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T8 Data Sheet

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Contents

Introduction

The T8 FPGA features the high-density, low-power Elitestek® Quantum® architecture wrapped with an I/O interface in a small footprint package for easy integration. T8 FPGAs support mobile, consumer, and IoT edge markets that need low power, low cost, and a small form factor. With ultra-low power T8 FPGAs, designers can build products that are always on, providing enhanced capabilities for applications such as embedded vision, voice and gesture recognition, intelligent sensor hubs, and power management.

Features

- High-density, low-power Quantum® architecture
- Built on SMIC 40 nm process
- Less than 150 µA typical core leakage current at 1.1 V(1)
- Ultra-small footprint package options
- FPGA interface blocks
  - GPIO
  - PLL
  - LVDS 600 Mbps per lane with up to 6 TX pairs and 6 RX pairs(2)
  - Oscillator
- Programmable high-performance I/O
  - Supports 1.8, 2.5, and 3.3 V single-ended I/O standards and interfaces(3)
- Flexible on-chip clocking
  - 12 low-skew global clock signals can be driven from off-chip external clock signals or PLL synthesized clock signals
  - PLL support
- Flexible device configuration
  - Standard SPI interface (active, passive, and daisy chain)
  - JTAG interface
  - Optional Mask Programmable Memory (MPM) capability
- Fully supported by the Efinity® software, an RTL-to-bitstream compiler

Table 1: T8 FPGA Resources

LEs(4)	Dedicated Global Clocks	Dedicated Global Controls	Embedded Memory (kbits)	Embedded Memory Blocks (5 Kbits)	Embedded Multipliers
7,384	Up to 16	Up to 8	122.88	24	8

(1) F49 and F81 packages only.
(2) LVDS pins are only available in Q144 packages.
(3) LVDS pins used as GPIO only support 3.3 V.
(4) Logic capacity in equivalent LE counts.

Table 2: T8 FPGA Package-Dependent Resources

Resource	F49	F81	Q144
Available GPIO[5]	33	55	97
Global clocks from GPIO pins	4	8	6
Global controls from GPIO pins	5	8	8
PLL (simple)	1	1	–
PLL (advanced)	–	–	5
Oscillator	1	1	–
MPM	1 (optional)	1 (optional)	1 (optional)
LVDS	–	–	6 TX pairs 6 RX pairs

Learn more: Refer to the **Trion Packaging User Guide** for the package outlines and markings.

Available Package Options

Table 3: Available Packages

Package	Dimensions (mm x mm)	Pitch (mm)
49-ball FBGA[6]	3 x 3	0.4
81-ball FBGA	5 x 5	0.5
144-pin LQFP	20 x 20	0.5

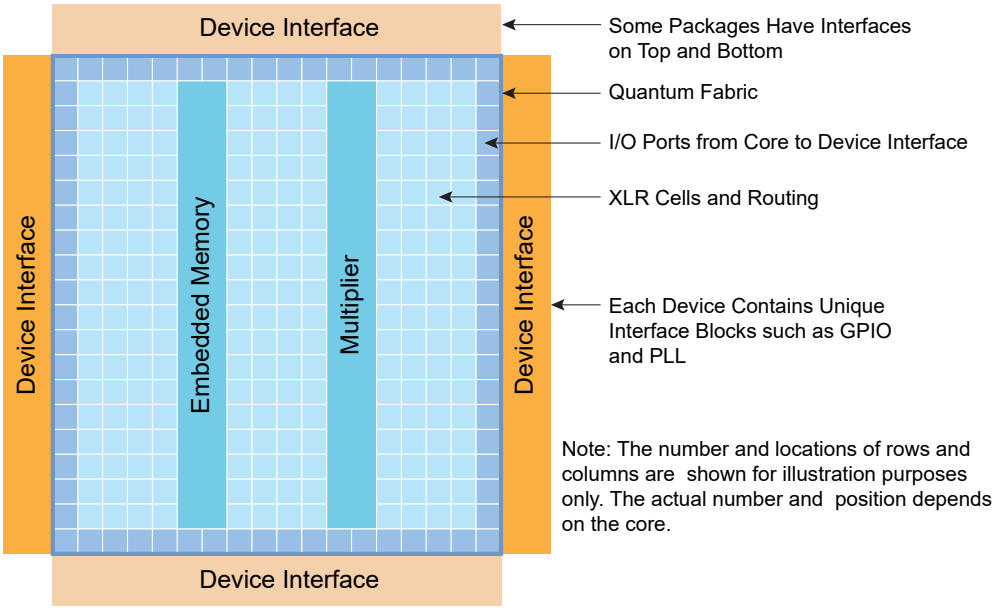
[5] The LVDS I/O pins are dual-purpose. The full number of GPIO are available when all LVDS I/O pins are in GPIO mode. GPIO and LVDS as GPIO supports different features. See **Table 9: Supported Features for GPIO and LVDS as GPIO** on page 12.

[6] This package does not have dedicated JTAG pins (TDI, TDO, TCK, TMS).

Device Core Functional Description

T8 FPGAs feature an eXchangeable Logic and Routing (XLR) cell that Elitestek has optimized for a variety of applications. Trion® FPGAs contain three building blocks constructed from XLR cells: logic elements, embedded memory blocks, and multipliers. Each FPGA in the Trion® family has a custom number of building blocks to fit specific application needs. As shown in the following figure, the FPGA includes I/O ports on all four sides, as well as columns of XLR cells, memory, and multipliers. A control block within the FPGA handles configuration.

Figure 1: T8 FPGA Block Diagram



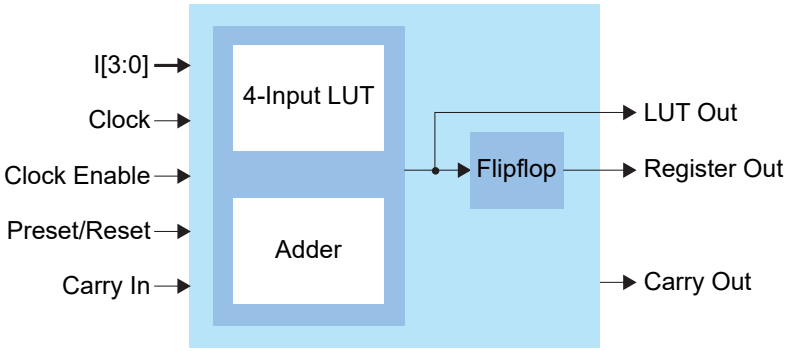
XLR Cell

The eXchangeable Logic and Routing (XLR) cell is the basic building block of the Quantum® architecture. The Elitestek XLR cell combines logic and routing and supports both functions interchangeably. This unique innovation greatly enhances the transistor flexibility and utilization rate, thereby reducing transistor counts and silicon area significantly.

Logic Cell

The logic cell comprises a 4-input LUT or a full adder plus a register (flipflop). You can program each LUT as any combinational logic function with four inputs. You can configure multiple logic cells to implement arithmetic functions such as adders, subtractors, and counters.

Figure 2: Logic Cell Block Diagram



Embedded Memory

The core has 5-kbit high-speed, synchronous, embedded SRAM memory blocks. Memory blocks can operate as single-port RAM, simple dual-port RAM, true dual-port RAM, FIFOs, or ROM. You can initialize the memory content during configuration. The Efinity® software includes a memory cascading feature to connect multiple blocks automatically to form a larger array. This feature enables you to instantiate deeper or wider memory modules.

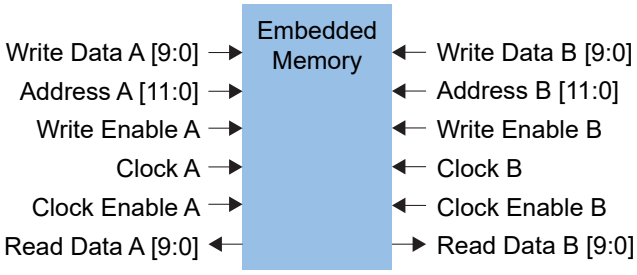
Note: The block RAM content is random and undefined if it is not initialized.

The memory read and write ports have the following modes for addressing the memory (depth x width):

256 x 16	1024 x 4	4096 x 1	512 x 10
512 x 8	2048 x 2	256 x 20	1024 x 5

The read and write ports support independently configured data widths.

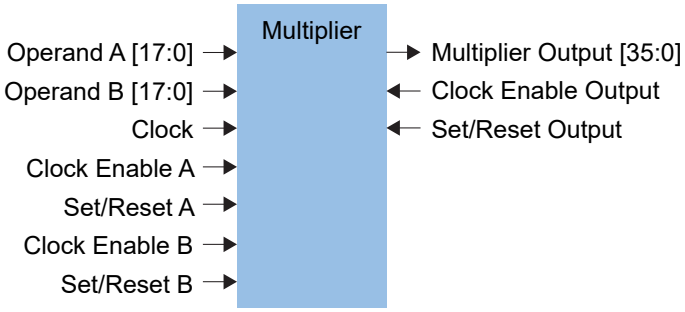
Figure 3: Embedded Memory Block Diagram (True Dual-Port Mode)



Multipliers

The FPGA has high-performance multipliers that support 18 x 18 fixed-point multiplication. Each multiplier takes two signed 18-bit input operands and generates a signed 36-bit output product. The multiplier has optional registers on the input and output ports.

Figure 4: Multiplier Block Diagram

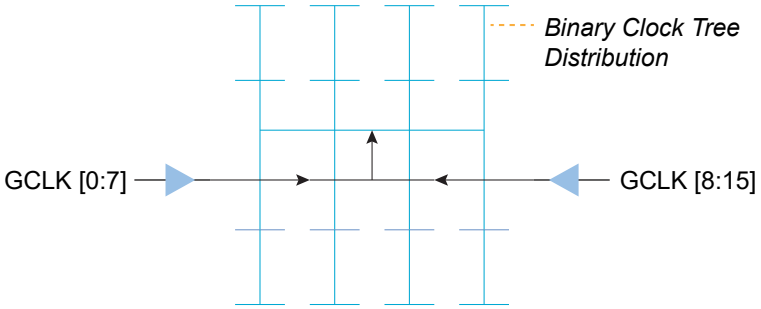


Global Clock Network

The Quantum® core fabric supports up to 16 global clock (GCLK) signals feeding 16 pre-built global clock networks. Global clock pins (GPIO), PLL outputs, oscillator output, and core-generated clocks can drive the global clock network.

The global clock networks are balanced clock trees that feed all FPGA modules. Each network has dedicated clock-enable logic to save power by disabling the clock tree at the root. The logic dynamically enables/disables the network and guarantees no glitches at the output.

Figure 5: Global Clock Network



Clock and Control Distribution Network

The global clock network is distributed through the device to provide clocking for the core's LEs, memory, multipliers, and I/O blocks. Designers can access the T8 global clock network using the global clock GPIO pins, PLL outputs, oscillator output, and core-generated clocks. Similarly, the T8 has GPIO pins (the number varies by package) that the designer can configure as control inputs to access the high-fanout network connected to the LE's set, reset, and clock enable signals.

Learn more: Refer to the **T8 Pinout** for information on the location and names of these pins.

Global Clock Location (Q144)

Table 4: Left Clock Input from GPIO Pins

Function Name	Resource Name	GCLK[0]	GCLK[1]	GCLK[2]	GCLK[3]	GCLK[4]	GCLK[5]	GCLK[6]	GCLK[7]
CLK0	GPIOL_24	✓	–	–	–	✓	–	–	–
CLK1	GPIOL_25	–	✓	–	–	–	✓	–	–
CLK2	GPIOL_26	–	–	✓	–	–	–	✓	–
CLK3	GPIOL_27	–	–	–	✓	–	–	–	✓
CLK4	GPIOL_28	✓	–	–	–	✓	–	–	–
CLK5	GPIOL_29	–	✓	–	–	–	✓	–	–
CLK6	GPIOL_30	–	–	✓	–	–	–	✓	–
CLK7	GPIOL_31	–	–	–	✓	–	–	–	✓

Table 5: Left Clock from PLL OUTCLK Signal

PLL Reference	CLKOUT	GCLK[0]	GCLK[1]	GCLK[2]	GCLK[3]	GCLK[4]	GCLK[5]	GCLK[6]	GCLK[7]
PLL_TL0	CLKOUT0	✓	–	–	–	–	–	✓	–
	CLKOUT1	–	✓	✓	–	–	–	–	–
	CLKOUT2	–	✓	✓	–	–	–	–	–
PLL_TL1	CLKOUT0	–	–	–	✓	–	–	–	✓
	CLKOUT1	–	–	–	–	✓	✓	–	–
	CLKOUT2	–	–	–	–	✓	✓	–	–

Table 6: Right Clock Input from GPIO Pins

Function Name	Resource Name	GCLK[8]	GCLK[9]	GCLK[10]	GCLK[11]	GCLK[12]	GCLK[13]	GCLK[14]	GCLK[15]
CLK0	GPIOR_127	✓	–	–	–	✓	–	–	–
CLK1	GPIOR_126	–	✓	–	–	–	✓	–	–
CLK2	GPIOR_125	–	–	✓	–	–	–	✓	–
CLK3	GPIOR_124	–	–	–	✓	–	–	–	✓
CLK4	GPIOR_123	✓	–	–	–	✓	–	–	–
CLK5	GPIOR_122	–	✓	–	–	–	✓	–	–
CLK6	GPIOR_121	–	–	✓	–	–	–	✓	–
CLK7	GPIOR_120	–	–	–	✓	–	–	–	✓

Table 7: Right Clock from PLL OUTCLK Signal

PLL Reference	CLKOUT	GCLK[8]	GCLK[9]	GCLK[10]	GCLK[11]	GCLK[12]	GCLK[13]	GCLK[14]	GCLK[15]
PLL_TR0	CLKOUT0	✓	–	–	–	–	–	✓	–
	CLKOUT1	–	✓	✓	–	–	–	–	–
	CLKOUT2	–	✓	✓	–	–	–	–	–
PLL_TR1	CLKOUT0	–	–	–	✓	–	–	–	✓
	CLKOUT1	–	–	–	–	✓	✓	–	–
	CLKOUT2	–	–	–	–	✓	✓	–	–
PLL_BR0	CLKOUT0	✓	–	–	–	–	–	–	✓
	CLKOUT1	–	✓	✓	–	–	–	–	–
	CLKOUT2	–	✓	✓	–	–	–	–	–

Device Interface Functional Description

The device interface wraps the core and routes signals between the core and the device I/O pads through a signal interface. Because they use the flexible Quantum® architecture, devices in the Trion® family support a variety of interfaces to meet the needs of different applications.

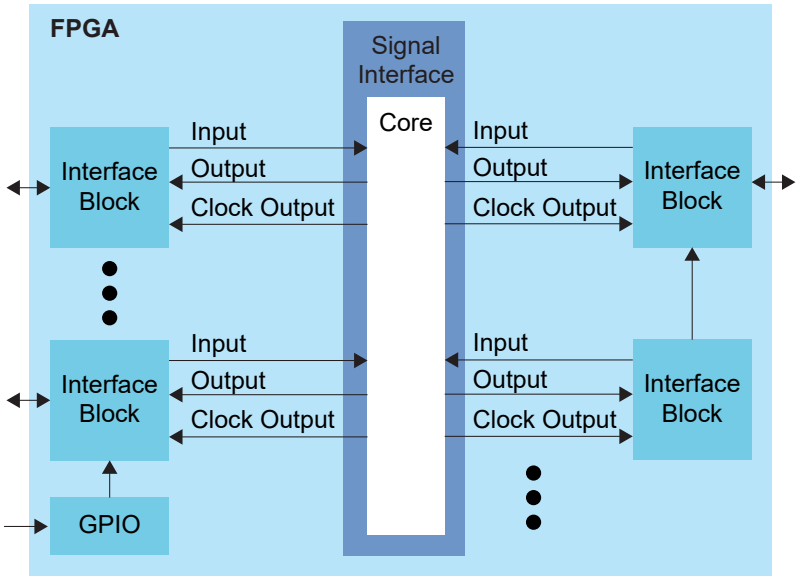
Learn more: The following sections describe the available device interface features in T8 FPGAs. Refer to the **Trion Interfaces User Guide** for details on the Efinity® Interface Designer settings.

Interface Block Connectivity

The FPGA core fabric connects to the interface blocks through a signal interface. The interface blocks then connect to the package pins. The core connects to the interface blocks using three types of signals:

- *Input*—Input data or clock to the FPGA core
- *Output*—Output from the FPGA core
- *Clock output*—Clock signal from the core clock tree

Figure 6: Interface Block and Core Connectivity



GPIO blocks are a special case because they can operate in several modes. For example, in alternate mode the GPIO signal can bypass the signal interface and directly feed another interface block. So a GPIO configured as an alternate input can be used as a PLL reference clock without going through the signal interface to the core.

When designing for Trion® FPGAs, you create an RTL design for the core and also configure the interface blocks. From the perspective of the core, outputs from the core are inputs to the interface block and inputs to the core are outputs from the interface block.

The Efinity netlist always shows signals from the perspective of the core, so some signals do not appear in the netlist:

- GPIO used as reference clocks are not present in the RTL design, they are only visible in the interface block configuration of the Efinity® Interface Designer.
- The FPGA clock tree is connected to the interface blocks directly. Therefore, clock outputs from the core to the interface are not present in the RTL design, they are only part of the interface configuration (this includes GPIO configured as output clocks).

The following sections describe the different types of interface blocks. Signals and block diagrams are shown from the perspective of the interface, not the core.

General-Purpose I/O Logic and Buffer

The GPIO support the 3.3 V LVTTL and 1.8 V, 2.5 V, and 3.3 V LVCMOS I/O standards. The GPIOs are grouped into banks. Each bank has its own VCCIO that sets the bank voltage for the I/O standard.

Each GPIO consists of I/O logic and an I/O buffer. I/O logic connects the core logic to the I/O buffers. I/O buffers are located at the periphery of the device.

The I/O logic comprises three register types:

- *Input*—Capture interface signals from the I/O before being transferred to the core logic
- *Output*—Register signals from the core logic before being transferred to the I/O buffers
- *Output enable*—Enable and disable the I/O buffers when I/O used as output

Table 8: GPIO Modes

GPIO Mode	Description
Input	Only the input path is enabled; optionally registered. If registered, the input path uses the input clock to control the registers (positively or negatively triggered). Select the alternate input path to drive the alternate function of the GPIO. The alternate path cannot be registered. **Q144 packages:** In DDIO mode, two registers sample the data on the positive and negative edges of the input clock, creating two data streams.
Output	Only the output path is enabled; optionally registered. If registered, the output path uses the output clock to control the registers (positively or negatively triggered). The output register can be inverted. **Q144 packages:** In DDIO mode, two registers capture the data on the positive and negative edges of the output clock, multiplexing them into one data stream.
Bidirectional	The input, output, and OE paths are enabled; optionally registered. If registered, the input clock controls the input register, the output clock controls the output and OE registers. All registers can be positively or negatively triggered. Additionally, the input and output paths can be registered independently. The output register can be inverted.
Clock output	Clock output path is enabled.

Table 9: Supported Features for GPIO and LVDS as GPIO

LVDS as GPIO are LVDS pins that act as GPIOs instead of the LVDS function.

Package	GPIO	LVDS as GPIO
F49 F81	Schmitt Trigger Variable Drive Strength Pull-up Pull-down Slew Rate	–
Q144	DDIO Schmitt Trigger Variable Drive Strength Pull-up Pull-down Slew Rate	Pull-up

Important: Elitestek® recommends that you limit the number of LVDS as GPIO set as output and bidirectional to 16 per bank to avoid switching noise. The Efinity software issues a warning if you exceed the recommended limit.

I/O Banks

Elitestek FPGAs have input/output (I/O) banks for general-purpose usage. Each I/O bank has independent power pins. The number and voltages supported vary by FPGA and package.

The number of banks and the voltages they support vary by package.

Some I/O banks are merged at the package level by sharing VCCIO pins. Merged banks have underscores (_) between banks in the name (e.g., 1B_1C means 1B and 1C are connected).

Table 10: I/O Banks by Package

Package	I/O Banks	Voltage (V)	Banks with DDIO Support	Merged Banks
F49, F81	1A - 1C, 2A, 2B	1.8, 2.5, 3.3	–	–
Q144	1A - 1E, 3A - 3E	1.8, 2.5, 3.3	1B, 1C, 1D, 3B, 3C, 3D, 3E	1C_1D, 3B_3C
	4A, 4B	3.3	–	–

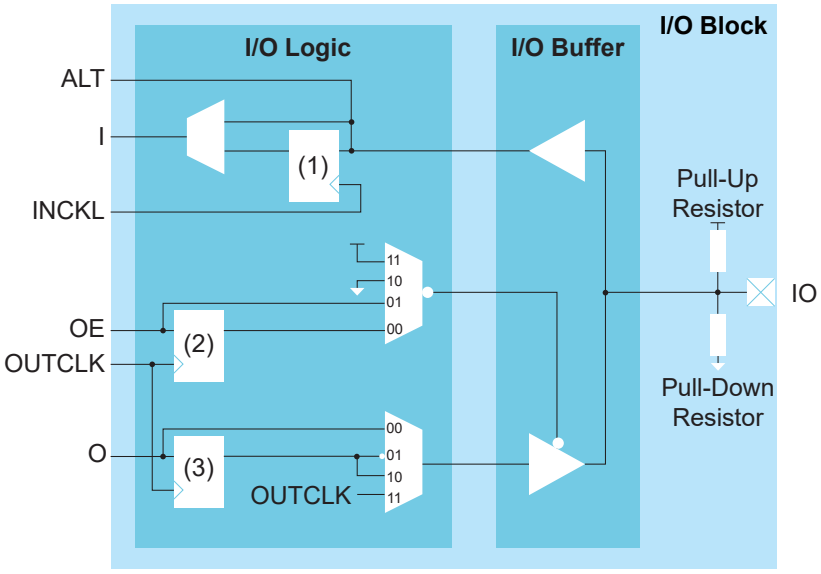
Learn more: Refer to the **T8 Pinout** for information on the I/O bank assignments.

T8 F49 and F81 Interface Description

T8 FPGAs in F49 and F81 packages have simple general-purpose I/O logic and buffers, I/O banks, a simple PLL, and an oscillator.

Simple I/O Buffer

Figure 7: I/O Interface Block



Notes:
1. Input Register
2. Output Enable Register
3. Output Register

Table 11: GPIO Signals

Signal	Direction	Description
I	Output	Input data from the GPIO pad to the core fabric.
ALT	Output	Alternative input connection (in the Interface Designer, the input **Register Option** is **none**). Alternative connections are GCLK, GCTRL, and PLL_CLKIN.
O	Input	Output data to GPIO pad from the core fabric.
OE	Input	Output enable from core fabric to the I/O block. Can be registered.
OUTCLK	Input	Core clock that controls the output and OE register. This clock is not visible in the user netlist.
INCLK	Input	Core clock that controls the input register. This clock is not visible in the user netlist.

Table 12: GPIO Pads

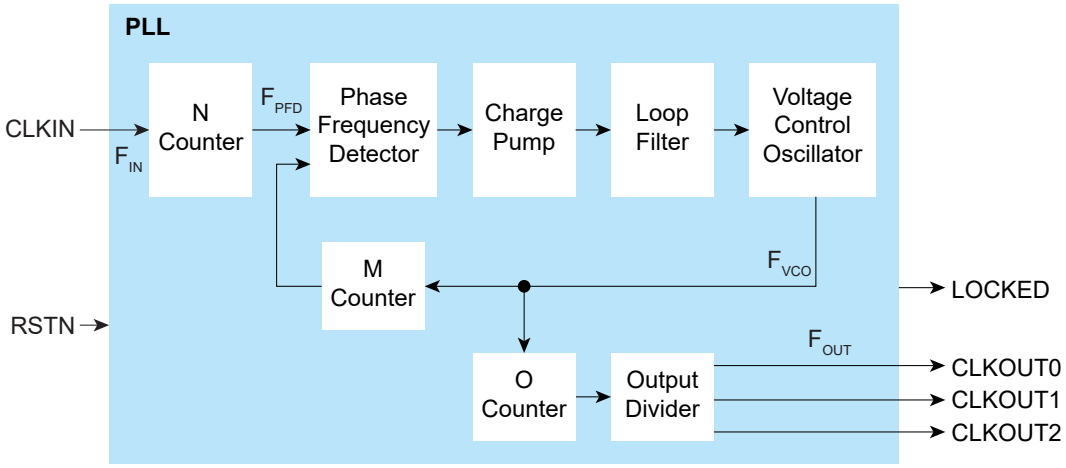
Signal	Direction	Description
IO	Bidirectional	GPIO pad.

Simple PLL

T8 FPGAs in F49 and F81 packages have a simple PLL.

The T8 has 1 PLL to synthesize clock frequencies. The PLL's reference clock input comes from a dedicated GPIO's alternate input pin. The PLL consists of a pre-divider counter (N counter), a feedback multiplier counter (M counter), post-divider counter (O counter), and an output divider per clock output.

Figure 8: T8 PLL Block Diagram



The counter settings define the PLL output frequency:	where:
$F_{PFD} = F_{IN} / N$ $F_{VCO} = F_{PFD} \times M$ $F_{OUT} = F_{VCO} / (O \times \text{Output divider})$	F_{VCO} is the voltage control oscillator frequency F_{OUT} is the output clock frequency F_{IN} is the reference clock frequency F_{PFD} is the phase frequency detector input frequency

Note: The reference clock must be between 10 and 50 MHz.
The PFD input must be between 10 and 50 MHz.
The VCO frequency must be between 500 and 1,200 MHz.

Unlike other Trion® FPGAs, the T8 simple PLL output locks on the *negative* clock edge (not the positive edge). When you are using two or more clock outputs, they are aligned on the falling edge. If the core register receiving the clock is positive edge triggered, Elitestek recommends inverting the clock outputs so they are correctly edge aligned.

Figure 9: Simple PLL Output Aligned with Negative Edge

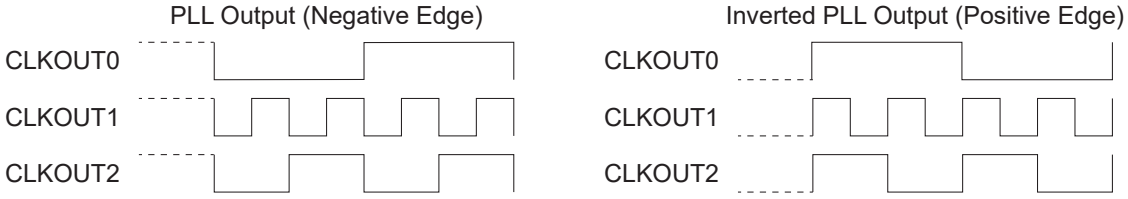


Table 13: PLL Pins

Port	Direction	Description
CLKIN	Input	Reference clock. This port is also a GPIO pin; the GPIO pins' alternate function is configured as a reference clock.
RSTN	Input	Active-low PLL reset signal. When asserted, this signal resets the PLL; when de-asserted, it enables the PLL. Connect this signal in your design to power up or reset the PLL. Assert the RSTN pin for a minimum pulse of 10 ns to reset the PLL.
CLKOUT0 CLKOUT1 CLKOUT2	Output	PLL output. The designer can route these signals as input clocks to the core's GCLK network.
LOCKED[7]	Output	Goes high when PLL achieves lock; goes low when a loss of lock is detected. Connect this signal in your design to monitor the lock status. This signal is analog asynchronous.

Table 14: PLL Settings

Configure these settings in the Efinity® Interface Designer.

Setting	Allowed Values	Notes
N counter	1 - 15 (integer)	Pre-divider
M counter	1 - 255 (integer)	Multiplier
O counter	1, 2, 4, 8	Post-divider
Output divider	2, 4, 8, 16, 32, 64, 128, 256	Output divider per output

Oscillator

T8 FPGAs in F49 and F81 packages have an oscillator.

The T8 has 1 low-frequency oscillator tailored for low-power operation. The oscillator runs at nominal frequency of 10 kHz. Designers can use the oscillator to perform always-on functions with the lowest power possible. Its output clock is available to the GCLK network.

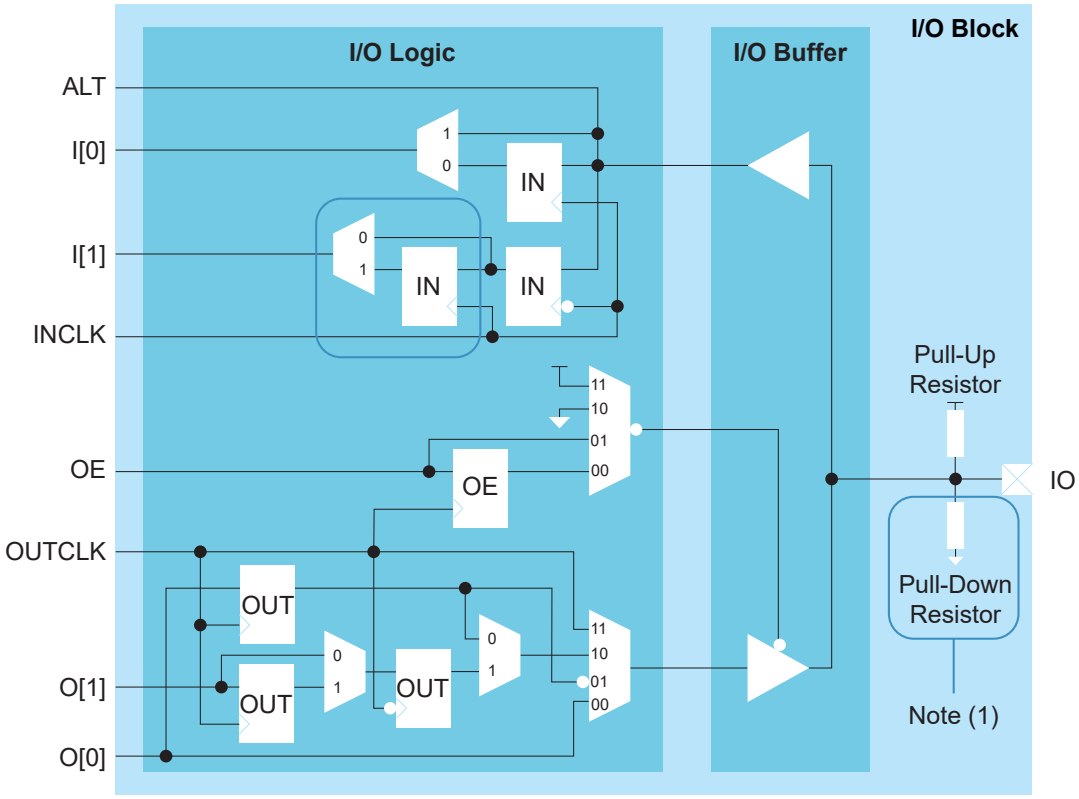
[7] The circuitry that generates the lock signal relies on a reference clock edge to transition the lock signal. A sudden removal of the reference clock will result in there being no positive clock edge with which to change the lock state from 1 back to 0. Therefore, the lock signal will remain on 1.

T8 Q144 Interface Description

T8 FPGAs in Q144 packages have advanced general-purpose I/O logic and buffers, I/O banks, advanced PLLs, and supports LVDS interface.

Complex I/O Buffer

Figure 10: I/O Interface Block



1. GPIO pins using LVDS resources do not have a pull-down resistor.

Note: LVDS as GPIO do not have double data I/O (DDIO).

Table 15: GPIO Signals (Interface to FPGA Fabric)

Signal	Direction	Description
I[1:0]	Output	Input data from the GPIO pad to the core fabric. I[0] is the normal input to the core. In DDIO mode, I[0] is the data captured on the positive clock edge (HI pin name in the Interface Designer) and I[1] is the data captured on the negative clock edge (LO pin name in the Interface Designer).
ALT	Output	Alternative input connection (in the Interface Designer, **Register Option** is **none**). Alternative connections are GCLK, GCTRL, PLL_CLKIN, and MIPI_CLKIN.
O[1:0]	Input	Output data to GPIO pad from the core fabric. O[0] is the normal output from the core. In DDIO mode, O[0] is the data output on the positive clock edge (HI pin name in the Interface Designer) and O[1] is the data output on the negative clock edge (LO pin name in the Interface Designer).
OE	Input	Output enable from core fabric to the I/O block. Can be registered.
OUTCLK	Input	Core clock that controls the output and OE registers. This clock is not visible in the user netlist unless you instantiate an EFX_GPIO_V2 primitive.
INCLK	Input	Core clock that controls the input registers. This clock is not visible in the user netlist unless you instantiate an EFX_GPIO_V2 primitive.

Table 16: GPIO Pads

Signal	Direction	Description
IO	Bidirectional	GPIO pad.

Double-Data I/O

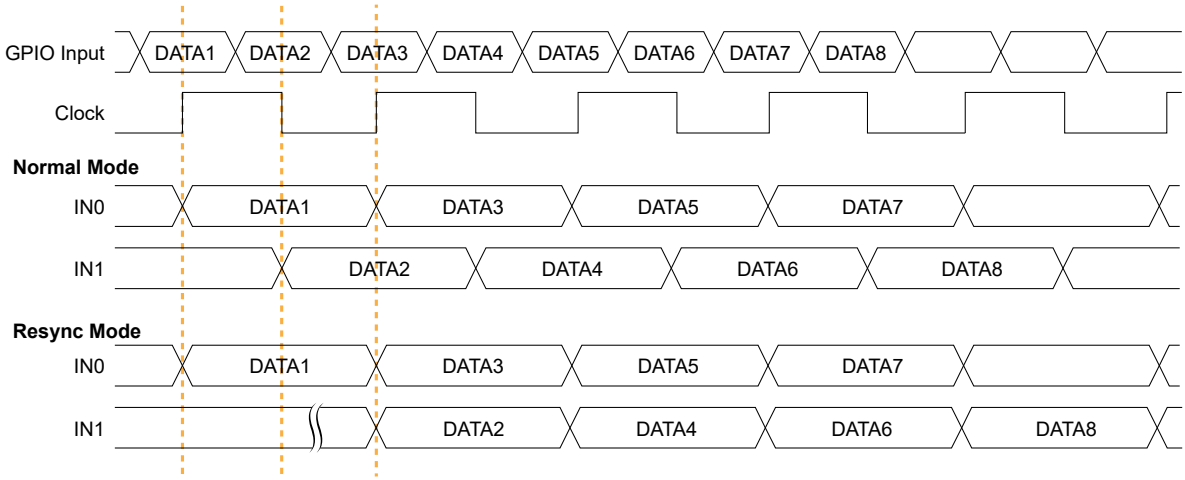
T8 FPGAs support double data I/O (DDIO) on input and output registers. In this mode, the DDIO register captures data on both positive and negative clock edges. The core receives 2 bit wide data from the interface.

In normal mode, the interface receives or sends data directly to or from the core on the positive and negative clock edges. In resync mode, the interface resynchronizes the data to pass both signals on the positive clock edge only.

Not all GPIO support DDIO; additionally, LVDS as GPIO (that is, single ended I/O) do not support DDIO functionality.

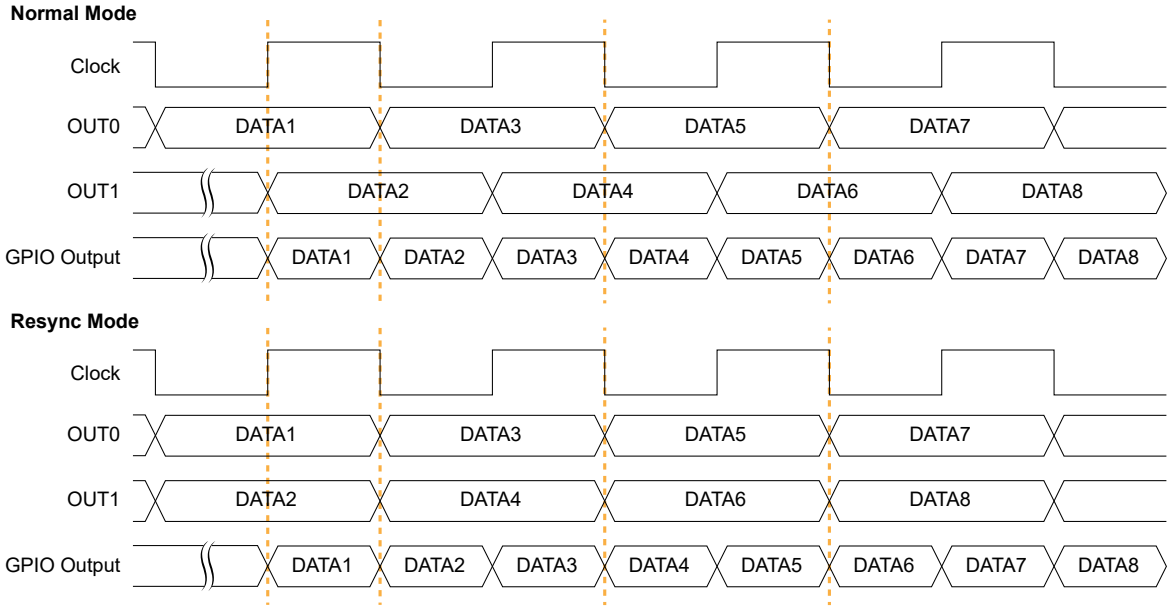
Note: The Resource Assigner in the Efinity® Interface Designer shows which GPIO support DDIO.

Figure 11: DDIO Input Timing Waveform



In resync mode, the IN1 data captured on the falling clock edge is delayed one half clock cycle.
In the Interface Designer, IN0 is the HI pin name and IN1 is the LO pin name.

Figure 12: DDIO Output Timing Waveform



In the Interface Designer, OUT0 is the HI pin name and OUT1 is the LO pin name.

Advanced PLL

T8 FPGAs in Q144 packages have 5 advanced PLLs.

Note: You can cascade the PLLs in T8 FPGAs. To avoid the PLL losing lock, Elitestek recommends that you do not cascade more than two PLLs.

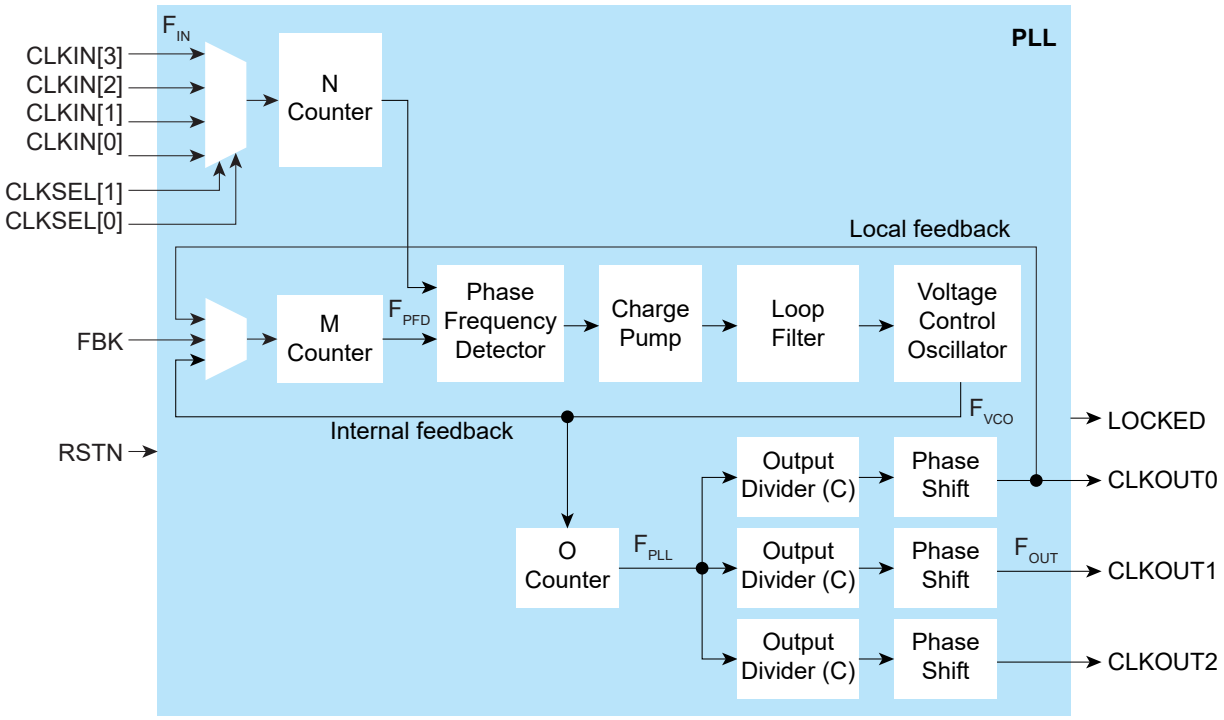
You can use the PLL to compensate for clock skew/delay via external or internal feedback to meet timing requirements in advanced application. The PLL reference clock has up to four sources. You can dynamically select the PLL reference clock with the `CLKSEL` port. (Hold the PLL in reset when dynamically selecting the reference clock source.)

One of the PLLs can use an LVDS RX buffer to input it's reference clock.

The PLL consists of a pre-divider counter (N counter), a feedback multiplier counter (M counter), a post-divider counter (O counter), and output divider.

Note: Refer to T8 Interface Floorplan for the location of the PLLs on the die. Refer to **Table 70: General Pinouts** on page 48 for the PLL reference clock resource assignment.

Figure 13: PLL Block Diagram



The counter settings define the PLL output frequency:

Internal Feedback Mode	Local and Core Feedback Mode	Where:
$F_{PFD} = F_{IN} / N$ $F_{VCO} = F_{PFD} \times M$ $F_{OUT} = (F_{IN} \times M) / (N \times O \times C)$ $F_{PLL} = F_{VCO} / O$	$F_{PFD} = F_{IN} / N$ $F_{VCO} = (F_{PFD} \times M \times O \times C_{FBK})$ [8] $F_{OUT} = (F_{IN} \times M \times C_{FBK}) / (N \times C)$ $F_{PLL} = F_{VCO} / O$	F_{VCO} is the voltage control oscillator frequency F_{OUT} is the output clock frequency F_{IN} is the reference clock frequency F_{PFD} is the phase frequency detector input frequency F_{PLL} is the post-divider PLL frequency C is the output divider O is the post-divider M is the multiplier N is the pre-divider C_{FBK} is the output divider for CLKOUT0

[8] $(M \times O \times C_{FBK})$ must be ≤ 255.

Note: F_{IN} must be within the values stated in **PLL Timing and AC Characteristics (Q144)** on page 41.

Figure 14: PLL Interface Block Diagram

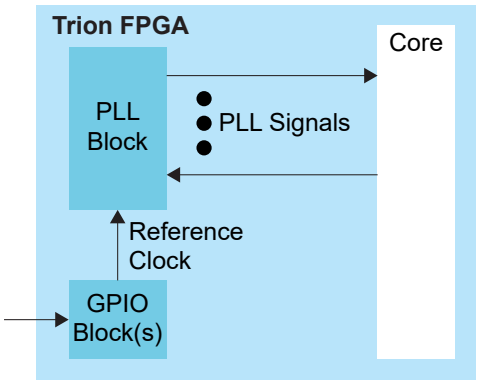


Table 17: PLL Signals (Interface to FPGA Fabric)

Signal	Direction	Description
CLKIN[3:0]	Input	Reference clocks driven by I/O pads or core clock tree.
CLKSEL[1:0]	Input	You can dynamically select the reference clock from one of the clock in pins.
RSTN	Input	Active-low PLL reset signal. When asserted, this signal resets the PLL; when de-asserted, it enables the PLL. De-assert only when the CLKIN signal is stable. Connect this signal in your design to power up or reset the PLL. Assert the RSTN pin for a minimum pulse of 10 ns to reset the PLL. Assert RSTN when dynamically changing the selected PLL reference clock.
FBK	Input	Connect to a clock out interface pin when the PLL feedback mode is not **internal**.
CLKOUT0 CLKOUT1 CLKOUT2	Output	PLL output. The designer can route these signals as input clocks to the core's GCLK network.
LOCKED[9]	Output	Goes high when PLL achieves lock; goes low when a loss of lock is detected; remains at previous state if the CLKIN goes discontinuous. Connect this signal in your design to monitor the lock status. This signal is not synchronized to any clock and the minimum high or low pulse width of the lock signal may be smaller than the CLKOUT's period.

Table 18: PLL Interface Designer Settings - Properties Tab

Parameter	Choices	Notes
Instance Name	User defined	
PLL Resource		The resource listing depends on the FPGA you choose.
Clock Source	External	PLL reference clock comes from external source through the REFCLK pin. Select the available external clock.
	Dynamic	PLL reference clock comes from up to four possible sources (external and core), and are controlled by the clock select bus. Specify the clock selector and core clock names.
	Core	PLL reference clock comes from the core. Specify the core clock pin name.
Automated Clock Calculation		Pressing this button launches the PLL Clock Caclulation window. The calculator helps you define PLL settings in an easy-to-use graphical interface.

[9] The circuitry that generates the lock signal relies on a reference clock edge to transition the lock signal. A sudden removal of the reference clock will result in there being no positive clock edge with which to change the lock state from 1 back to 0. Therefore, the lock signal will remain on 1.

Table 19: PLL Interface Designer Settings - Manual Configuration Tab

Parameter	Choices	Notes
Reset Pin Name	User defined	
Locked Pin Name	User defined	
Feedback Mode	Internal	PLL feedback is internal to the PLL resulting in no known phase relationship between clock in and clock out.
	Local	PLL feedback is local to the PLL. Aligns the clock out phase with clock in.
	Core	PLL feedback is from the core. The feedback clock is defined by the COREFBK connection, and must be one of the three PLL output clocks. Aligns the clock out phase with clock in and removes the core clock delay.
Reference clock Frequency (MHz)	User defined	
Multiplier (M)	1 - 255 (integer)	M counter.
Pre Divider (N)	1 - 15 (integer)	N counter.
Post Divider (O)	1, 2, 4, 8	O counter. The value must be 2 or higher if you enable more than 1 PLL output.
Clock 0, Clock 1, Clock 2	On, off	Use these checkboxes to enable or disable clock 0, 1, and 2.
Pin Name	User defined	Specify the pin name for clock 0, 1, or 2.
Divider (C)	1 to 256	Output divider.
Phase Shift (Degree)	0, 45, 90, 135, 180, or 270	Phase shift CLKOUT by 45°, 90°, 135°, 180°, or 270°. The phase shifts are supported with the following C divider settings: C divider = 2 : 90°, 180°, and 270° C divider = 4 : 45°, 90°, and 135° C divider = 6 : 90° To phase shift 225°, select 45° and invert the clock at the destination. To phase shift 315°, select 135° and invert the clock at the destination.
Use as Feedback	On, off	

Table 20: PLL Reference Clock Resource Assignments (Q144)

PLL	REFCLK1	REFCLK2
PLL_BR0	Differential: GPIOB_CLKP0, GPIOB_CLKN0 Single Ended: GPIOB_CLKP0	GPIOR_157_PLLIN
PLL_TR0	GPIOR_76_PLLIN0	GPIOR_77_PLLIN1
PLL_TR1	GPIOR_76_PLLIN0	GPIOR_77_PLLIN1
PLL_TL0	GPIOL_74_PLLIN0	GPIOL_75_PLLIN1
PLL_TL1	GPIOL_74_PLLIN0	GPIOL_75_PLLIN1

LVDS

T8 FPGAs in Q144 packages have an LVDS interface.

The LVDS hard IP transmitters and receivers operate independently.

- LVDS TX consists of LVDS transmitter and serializer logic.
- LVDS RX consists of LVDS receiver, on-die termination, and de-serializer logic.

The T8 has one PLL for use with the LVDS receiver.

Note: You can use the LVDS TX and LVDS RX channels as 3.3 V single-ended GPIO pins, which support a weak pull-up but do not support a Schmitt trigger or variable drive strength. When using LVDS as GPIO, make sure to leave at least 2 pairs of unassigned LVDS pins between any GPIO and LVDS pins. This rule applies for pins on each side of the device (top, bottom, left, right). This separation reduces noise. The Efinity software issues an error if you do not leave this separation.

The LVDS hard IP has these features:

- Up to 600 Mbps for LVDS data transmit or receive
- Supports serialization and deserialization factors: 8:1, 7:1, 6:1, 5:1, 4:1, 3:1, and 2:1
- Ability to disable serialization and deserialization
- Source synchronous clock output edge-aligned with data for LVDS transmitter and receiver
- 100 Ω on-die termination resistor for the LVDS receiver

Note: The LVDS RX supports the sub-lvds, slvs, HiVcm, RSDS and 3.3 V LVPECL differential I/O standards with a transfer rate of up to 800 Mbps.

LVDS TX

Figure 15: LVDS TX Interface Block Diagram

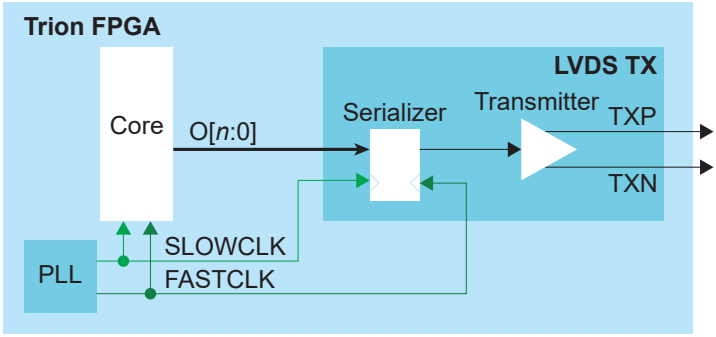


Table 21: LVDS TX Signals (Interface to FPGA Fabric)

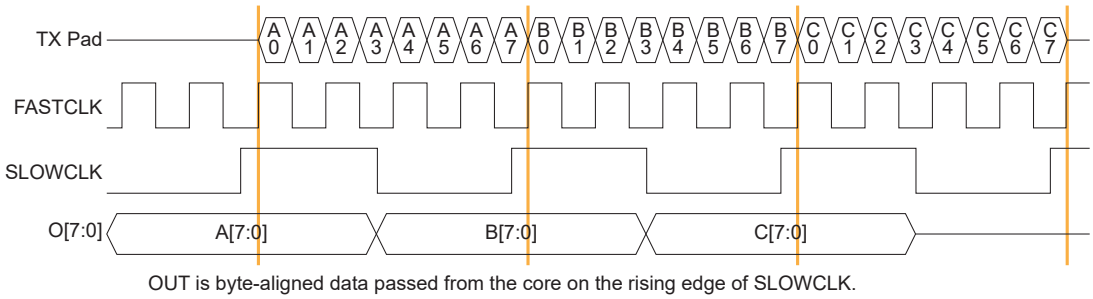
Signal	Direction	Notes
O[*n*-1:0]	Input	Parallel output data where *n* is the serialization factor. A width of 1 bypasses the serializer.
FASTCLK	Input	Fast clock to serialize the data to the LVDS pads.
SLOWCLK	Input	Slow clock to latch the incoming data from the core.

Table 22: LVDS TX Pads

Pad	Direction	Description
TXP	Output	Differential P pad.
TXN	Output	Differential N pad.

The following waveform shows the relationship between the fast clock, slow clock, TX data going to the pad, and byte-aligned data from the core.

Figure 16: LVDS Timing Example Serialization Width of 8



OUT is byte-aligned data passed from the core on the rising edge of SLOWCLK.

Figure 17: LVDS Timing Data and Clock Relationship Width of 8 (Parallel Clock Division=1)

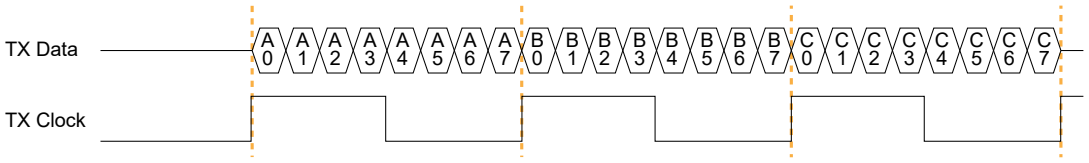
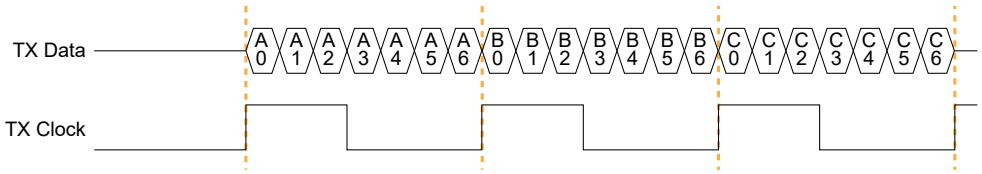


Figure 18: LVDS Timing Data and Clock Relationship Width of 7 (Parallel Clock Division=1)



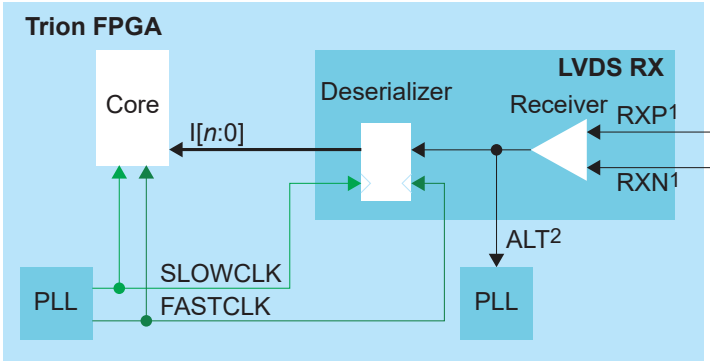
Note: For LVDS TX interfaces with multiple LVDS TX lanes and an LVDS TX reference clock output, use the LVDS TX blocks from the same side of the FPGA to minimize skew between data lanes and TX reference clock output.

Table 23: LVDS TX Settings in Efinity® Interface Designer

Parameters	Choices	Notes
Instance Name	User defined	
LVDS Resource	Resource list	Choose a resource.
Mode	serial data output or reference clock output	**serial data output**—Simple output buffer or serialized output. **reference clock output**—Use the transmitter as a clock output. When choosing this mode, the **Serialization Width** you choose should match the serialization for the rest of the LVDS bus.
Parallel Clock Division	1, 2	**1**—The output clock from the LVDS TX lane is parallel clock frequency. **2**—The output clock from the TX lane is half of the parallel clock frequency.
Enable Serialization	On or off	When off, the serializer is bypassed and the LVDS buffer is used as a normal output.
Serialization Width	2, 3, 4, 5, 6, 7, or 8	Supports 8:1, 7:1, 6:1, 5:1, 4:1, 3:1, and 2:1. Specify the serial clock and parallel clock.
Output Pin/Bus Name	User defined	Output pin or bus that feeds the LVDS transmitter parallel data. The width should match the serialization factor.
Output Enable Pin Name	User defined	Use with serial data output mode. Only available when serialization is disabled.
Reduce VOD Swing	On or off	When true, enables reduced output swing (similar to slow slew rate).
Output Load	5, 7, or 10	Output load in pF. Use an output load of 7 pF or higher to achieve the maximum supported toggle rate. See **Table 53: Maximum Toggle Rate** on page 37.

LVDS RX

Figure 19: LVDS RX Interface Block Diagram



1. There is a ~30k Ω internal weak pull-up to VCCIO (3.3V).
2. Only available for an LVDS RX resource in bypass mode (deserialization width is 1).

Table 24: LVDS RX Signals (Interface to FPGA Fabric)

Signal	Direction	Notes
I[*n*-1:0]	Output	Parallel input data where *n* is the de-serialization factor. A width of 1 bypasses the deserializer.
ALT	Output	Alternative input, only available for an LVDS RX resource in bypass mode (deserialization width is 1; alternate connection type). Alternative connections are PLL_CLKIN.
FASTCLK	Input	Fast clock to de-serialize the data from the LVDS pads.
SLOWCLK	Input	Slow clock to latch the incoming data to the core.

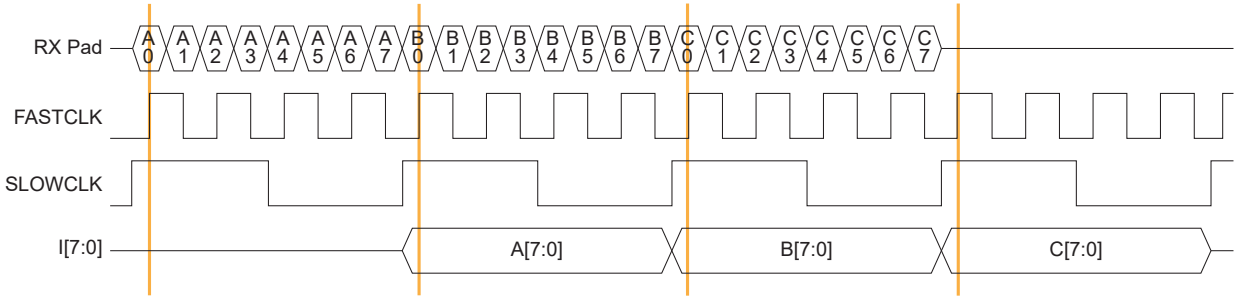
Table 25: LVDS RX Pads

Pad	Direction	Description
RXP	Input	Differential P pad.
RXN	Input	Differential N pad.

Note: You need an external DC-biased circuit if the incoming LVDS signals are AC-coupled. Refer to **Elitestek website** for more information.

The following waveform shows the relationship between the fast clock, slow clock, RX data coming in from the pad, and byte-aligned data to the core.

Figure 20: LVDS RX Timing Example Serialization Width of 8



I is byte-aligned data passed to the core on the rising edge of SLOWCLK.

Note: For LVDS RX interfaces with multiple LVDS RX lanes and an LVDS RX clock input, use the LVDS RX blocks from the same side of the FPGA to minimize skew between data lanes and RX clock input.

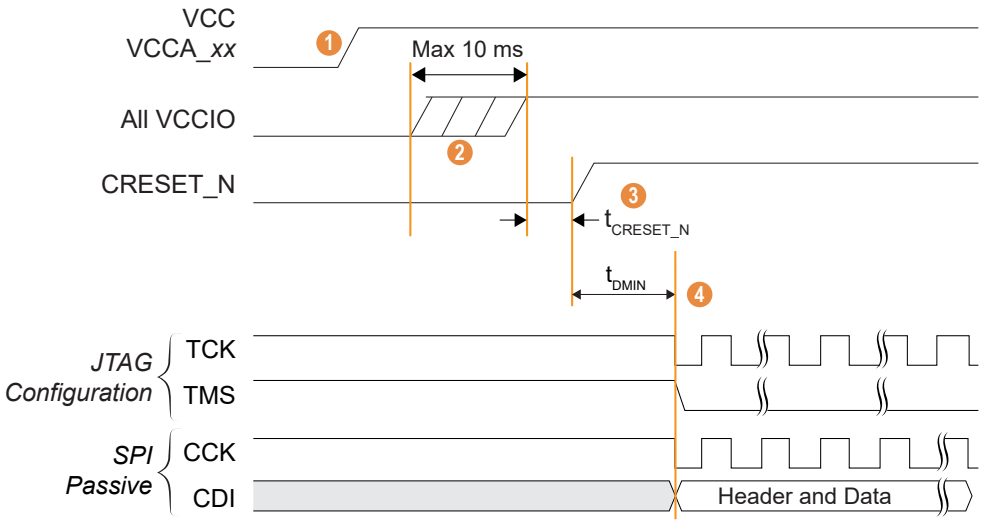
Table 26: LVDS RX Settings in Efinity® Interface Designer

Parameter	Choices	Notes
Instance Name	User defined	
LVDS Resource	Resource list	Choose a resource.
Connection Type	normal, pll_clkin	**normal**—Regular RX function. **pll_clkin**—Use the PLL CLKIN alternate function of the LVDS RX resource.
Input Pin/Bus Name	User defined	Input pin or bus that feeds the LVDS transmitter parallel data. The width should match the deserialization factor.
Enable Deserialization	On or off	When off, the de-serializer is bypassed and the LVDS buffer is used as a normal input. Specify the serial clock and parallel clock.
Deserialization Width	2, 3, 4, 5, 6, 7, or 8	Supports 8:1, 7:1, 6:1, 5:1, 4:1, 3:1, and 2:1.
Enable On-Die Termination	On or off	When on, enables an on-die 100-ohm resistor.
Static Mode Delay Setting	0 - 63	Choose the amount of static delay, each step adds approximately 25 ps of delay.

Power Up Sequence

Elitestek® recommends the following power up sequence when powering Trion® FPGAs:

Figure 21: Trion® FPGAs Power Up Sequence



1. Power up VCC and VCCA_xx first.
2. When VCC and VCCA_xx are stable, power up all VCCIO pins. There is no specific timing delay between the VCCIO pins.

   Important: Ensure the power ramp rate is within VCCIO/10 V/ms to 10 V/ms.
3. After all power supplies are stable, hold CRESET_N low for a duration of t_{CRESET_N} before asserting CRESET_N from low to high to trigger active SPI programming (the FPGA loads the configuration data from an external flash device).
4. FPGA configuration can begin after there has been a t_{DMIN} minimum delay after CRESET_N goes high (see **SPI Passive** on page 45 and **JTAG** on page 46 for the delay specification).

When you are not using the GPIO or PLL resources, connect the pins as shown in the following table.

Note: Refer to **Configuration Timing** on page 43 for timing information.

Power Supply Current Transient

You may observe an inrush current on the dedicated power rail during power-up. You must ensure that the power supplies selected in your board meets the current requirement during power-up and the estimated current during user mode. Use the Power Estimator to calculate the estimated current during user mode.

Table 27: Maximum Power Supply Current Transient

Power Supply	Device Package	Maximum Power Supply Current Transient[10][11]	Unit
VCC	F49, F81	18	mA
	Q144	35	mA

(10) Inrush current for other power rails are not significant in Trion® FPGAs.
(11) Measured at room temperature.

Unused Resources and Features

Table 28: Connection Requirements for Unused Resources

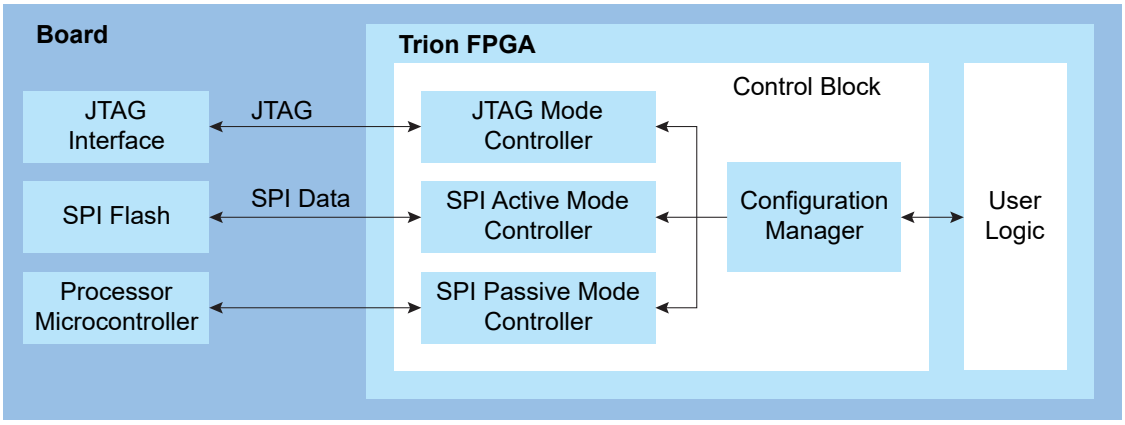
Unused Resource	Pin	Note
GPIO Bank	VCCIOxx	Connect to either 1.8 V, 2.5 V, or 3.3 V.
PLL	VCCA_PLL	Connect to VCC.

Configuration

The T8 FPGA contains volatile Configuration RAM (CRAM). The user must configure the CRAM for the desired logic function upon power-up and before the FPGA enters normal operation. The FPGA's control block manages the configuration process and uses a bitstream to program the CRAM. The Efinity® software generates the bitstream, which is design dependent. You can configure the T8 FPGA(s) in SPI active, SPI passive, or JTAG mode.

Learn more: Refer to **AN 006: Configuring Trion FPGAs** for details on the dedicated configuration pins and how to configure FPGA(s).

Figure 22: High-Level Configuration Options



In active mode, the FPGA controls the configuration process. An oscillator circuit within the FPGA provides the configuration clock. The bitstream is typically stored in an external serial flash device, which provides the bitstream when the FPGA requests it.

The control block sends out the instruction and address to read the configuration data. First, it issues a release from power-down instruction to wake up the external SPI flash. Then, it waits for at least 30 µs before issuing a fast read command to read the content of SPI flash from address 24h'000000.

In passive mode, the FPGA is the slave and relies on an external master to provide the control, bitstream, and clock for configuration. Typically the master is a microcontroller or another FPGA in active mode.

In JTAG mode, you configure the FPGA via the JTAG interface.

Supported Configuration Modes

Table 29: T8 Configuration Modes by Package

Configuration Mode	Width	F49	F81	F144
Active	X1	✓	✓	✓
	X2	✓	✓	✓
	X4	✓	✓	✓
Passive	X1	✓	✓	✓
	X2	✓	✓	✓
	X4	✓	✓	✓
	X8	✓	✓	✓
JTAG	X1		✓	✓

Mask-Programmable Memory Option

The T8 FPGA is equipped with one-time programmable MPM. With this feature, you use on-chip MPM instead of an external serial flash device to configure the FPGA. This option is for systems that require an ultra-small factor and the lowest cost structure such that an external serial flash device is undesirable and/or not required at volume production. MPM is a one-time factory programmable option that requires a Non-Recurring Engineering (NRE) payment. To enable MPM, submit your design to our factory; our Applications Engineers (AEs) convert your design into a single configuration mask to be specially fabricated.

DC and Switching Characteristics (F49 and F81)

Table 30: Absolute Maximum Ratings [12]

Conditions beyond those listed may cause permanent damage to the device. Device operation at the absolute maximum ratings for extended periods of time has adverse effects on the device.

Symbol	Description	Min	Max	Units
VCC	Core power supply	-0.5	1.42	V
VCCIO	I/O bank power supply	-0.5	4.6	V
VCCA_PLL	PLL analog power supply	-0.5	1.42	V
V_{IN}	I/O input voltage	-0.5	4.6	V
I_{IN}	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.[13]	–	10	mA
T_J	Operating junction temperature	-40	125	°C
T_{STG}	Storage temperature, ambient	-55	150	°C

Table 31: Recommended Operating Conditions [12]

Symbol	Description	Min	Typ	Max	Units
VCC	Core power supply	1.05	1.1	1.15	V
VCCIO	1.8 V I/O bank power supply	1.71	1.8	1.89	V
	2.5 V I/O bank power supply	2.38	2.5	2.63	V
	3.3 V I/O bank power supply	3.14	3.3	3.47	V
VCCA_PLL	PLL analog power supply	1.05	1.1	1.15	V
V_{IN}	I/O input voltage[14]	-0.3	–	VCCIO + 0.3	V
T_{JCOM}	Operating junction temperature, commercial	0	–	85	°C
T_{JIND}	Operating junction temperature, industrial	-40	–	100	°C

Table 32: Power Supply Ramp Rates

Symbol	Description	Min	Max	Units
t_{RAMP}	Power supply ramp rate for all supplies.	VCCIO/10	10	V/ms

(12) Supply voltage specification applied to the voltage taken at the device pins with respect to ground, not at the power supply.
(13) Should not exceed a total of 120 mA per bank.
(14) Values applicable to both input and tri-stated output configuration.

Table 33: Single-Ended I/O DC Electrical Characteristics

I/O Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)
	Min	Max	Min	Max	Max	Min
3.3 V LVCMOS	-0.3	0.8	2	VCCIO + 0.3	0.2	VCCIO - 0.2
3.3 V LVTTL	-0.3	0.8	2	VCCIO + 0.3	0.4	2.4
2.5 V LVCMOS	-0.3	0.7	1.7	VCCIO + 0.3	0.5	1.8
1.8 V LVCMOS	-0.3	0.35 * VCCIO	0.65 * VCCIO	VCCIO + 0.3	0.45	VCCIO - 0.45

Table 34: Single-Ended I/O and Dedicated Configuration Pins Schmitt Trigger Buffer Characteristic

Voltage	VT+ (V) Schmitt Trigger Low-to-High Threshold	VT- (V) Schmitt Trigger High-to-Low Threshold	Input Leakage Current (µA)	Tristate Output Leakage Current (µA)
3.3	1.73	1.32	±10	±10
2.5	1.37	1.01	±10	±10
1.8	1.05	0.71	±10	±10

Table 35: Single-Ended I/O Buffer Drive Strength Characteristics

Junction temperature at T_J = 25 °C, power supply at nominal voltage, device in nominal process (TT).

CDONE has a drive strength of 1.

I/O Standard	3.3 V		2.5 V		1.8 V	
Drive Strength	I_{OH} (mA)	I_{OL} (mA)	I_{OH} (mA)	I_{OL} (mA)	I_{OH} (mA)	I_{OL} (mA)
1	14.4	8.0	9.1	8.0	5.1	4.4
2	19.1	10.5	12.2	10.5	6.8	5.8
3	23.9	13.3	15.2	13.4	8.6	7.3
4	28.7	15.8	18.2	15.9	10.3	8.6

Table 36: Single-Ended I/O Internal Weak Pull-Up and Pull-Down Resistance

CDONE and CRESET_N also have an internal weak pull-up with these values.

I/O Standard	Internal Pull-Up			Internal Pull-Down			Units
	Min	Typ	Max	Min	Typ	Max	
3.3 V LVTTL/LVCMOS	27	40	65	30	47	83	kΩ
2.5 V LVCMOS	35	55	120	37	62	118	kΩ
1.8 V LVCMOS	70	90	200	80	99	300	kΩ

Table 37: Single-Ended I/O Rise and Fall Time

Data are based on the following IBIS simulation setup:

- Weakest drive strength model
- Typical simulation corner setting
- RLC circuit with 6.6 pF capacitance, 16.6 nH inductance, 0.095 ohm resistance, and 25 °C temperature

Note: For a more accurate data, you need to perform the simulation with your own circuit.

I/O Standard	Rise Time (T_R)		Fall Time (T_F)		Units
	Slow Slew Rate Enabled	Slow Slew Rate Disabled	Slow Slew Rate Enabled	Slow Slew Rate Disabled	
3.3 V LVTTL/LVCMOS	1.13	1.02	1.24	1.17	ns
2.5 V LVCMOS	1.4	1.3	1.44	1.31	ns
1.8 V LVCMOS	2.14	2.01	2.05	1.85	ns

Table 38: Maximum Toggle Rate

Elitestek recommends that you perform simulations using the IBIS model to determine the maximum toggle rate for your design.

I/O Standard	Max Toggle Rate	Units
3.3 V LVTTL/LVCMOS	400	Mbps
2.5 V LVCMOS	400	Mbps
1.8 V LVCMOS	400	Mbps

Table 39: Block RAM Characteristics

Symbol	Description	C2, I2 Speed Grade	Units
f_{MAX}	Block RAM maximum frequency.	275	MHz

Table 40: Multiplier Block Characteristics

Symbol	Description	C2, I2 Speed Grade	Units
f_{MAX}	Multiplier block maximum frequency.	275	MHz

DC and Switching Characteristics (Q144)

Table 41: Absolute Maximum Ratings

Conditions beyond those listed may cause permanent damage to the device. Device operation at the absolute maximum ratings for extended periods of time has adverse effects on the device.

Symbol	Description	Min	Max	Units
VCC	Core power supply	-0.5	1.42	V
VCCIO	I/O bank power supply	-0.5	4.6	V
VCCA_PLL	PLL analog power supply	-0.5	1.42	V
V_{IN}	I/O input voltage	-0.5	4.6	V
I_{IN}	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.(16)	–	10	mA
T_J	Operating junction temperature	-40	125	°C
T_{STG}	Storage temperature, ambient	-55	150	°C

Table 42: Recommended Operating Conditions (C3, C4, and I4 Speed Grades) (15)

Symbol	Description	Min	Typ	Max	Units
VCC	Core power supply	1.15	1.2	1.25	V
VCCIO	1.8 V I/O bank power supply	1.71	1.8	1.89	V
	2.5 V I/O bank power supply	2.38	2.5	2.63	V
	3.3 V I/O bank power supply	3.14	3.3	3.47	V
VCCA_PLL	PLL analog power supply	1.15	1.2	1.25	V
V_{IN}	I/O input voltage(17)	-0.3	–	VCCIO + 0.3	V
T_{JCOM}	Operating junction temperature, commercial	0	–	85	°C
T_{JIND}	Operating junction temperature, industrial	-40	–	100	°C

(15) Supply voltage specification applied to the voltage taken at the device pins with respect to ground, not at the power supply.
(16) Should not exceed a total of 120 mA per bank.
(17) Values applicable to both input and tri-stated output configuration.

Table 43: Recommended Operating Conditions (C4L and I4L Speed Grades) [15]

Symbol	Description	Min	Typ	Max	Units
VCC	Core power supply	1.05	1.1	1.15	V
VCCIO	1.8 V I/O bank power supply	1.71	1.8	1.89	V
	2.5 V I/O bank power supply	2.38	2.5	2.63	V
	3.3 V I/O bank power supply	3.14	3.3	3.47	V
VCCA_PLL	PLL analog power supply	1.05	1.1	1.15	V
V_{IN}	I/O input voltage[18]	-0.3	–	VCCIO + 0.3	V
T_{JCOM}	Operating junction temperature, commercial	0	–	85	°C
T_{JIND}	Operating junction temperature, industrial	-40	–	100	°C

Table 44: Power Supply Ramp Rates

Symbol	Description	Min	Max	Units
t_{RAMP}	Power supply ramp rate for all supplies.	VCCIO/10	10	V/ms

Table 45: Single-Ended I/O DC Electrical Characteristics

I/O Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)
	Min	Max	Min	Max	Max	Min
3.3 V LVCMOS	-0.3	0.8	2	VCCIO + 0.3	0.2	VCCIO - 0.2
3.3 V LVTTL	-0.3	0.8	2	VCCIO + 0.3	0.4	2.4
2.5 V LVCMOS	-0.3	0.7	1.7	VCCIO + 0.3	0.5	1.8
1.8 V LVCMOS	-0.3	0.35 * VCCIO	0.65 * VCCIO	VCCIO + 0.3	0.45	VCCIO - 0.45

Table 46: Single-Ended I/O and Dedicated Configuration Pins Schmitt Trigger Buffer Characteristic

Voltage (V)	VT+ (V) Schmitt Trigger Low-to-High Threshold	VT- (V) Schmitt Trigger High-to-Low Threshold	Input Leakage Current (µA)	Tri-State Output Leakage Current (µA)
3.3	1.73	1.32	±10	±10
2.5	1.37	1.01	±10	±10
1.8	1.05	0.71	±10	±10

[18] Values applicable to both input and tri-stated output configuration.

Table 47: Single-Ended I/O Buffer Drive Strength Characteristics

Junction temperature at T_J = 25 °C, power supply at nominal voltage.

CDONE has a drive strength of 1.

I/O Standard	3.3 V		2.5 V		1.8 V	
Drive Strength	I_{OH} (mA)	I_{OL} (mA)	I_{OH} (mA)	I_{OL} (mA)	I_{OH} (mA)	I_{OL} (mA)
1	14.4	8.0	9.1	8.0	5.1	4.4
2	19.1	10.5	12.2	10.5	6.8	5.8
3	23.9	13.3	15.2	13.4	8.6	7.3
4	28.7	15.8	18.2	15.9	10.3	8.6

Table 48: Single-Ended I/O Internal Weak Pull-Up and Pull-Down Resistance

CDONE and CRESET_N also have an internal weak pull-up with these values.

I/O Standard	Internal Pull-Up			Internal Pull-Down			Units
	Min	Typ	Max	Min	Typ	Max	
3.3 V LVTTL/LVCMOS	27	40	65	30	47	83	kΩ
2.5 V LVCMOS	35	55	120	37	62	118	kΩ
1.8 V LVCMOS	70	90	200	80	99	300	kΩ

Table 49: LVDS Pins Configured as Single-Ended I/O DC Electrical Characteristics

I/O Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)
	Min	Max	Min	Max	Max	Min
3.3 V LVCMOS	-0.3	0.8	2	VCCIO + 0.3	0.2	VCCIO - 0.2
3.3 V LVTTL	-0.3	0.8	2	VCCIO + 0.3	0.4	2.4

Table 50: LVDS Pins Configured as Single-Ended I/O Buffer Drive Strength Characteristics

Junction temperature at TJ = 25 °C, power supply at nominal voltage, device in nominal process (TT).

I/O Standard	Drive Strength	
	I_{OH}(mA)	I_{OL}(mA)
3.3 V	37.6	22

Table 51: LVDS Pins Configured as Single-Ended I/O DC Electrical Characteristics

Voltage (V)	Input Leakage Current (µA)	Tri-State Output Leakage Current (µA)
3.3	±10	±10

Table 52: LVDS Pins Configured as Single-Ended I/O Internal Weak Pull-Up Resistance

I/O Standard	Internal Pull-Up			Units
	Min	Typ	Max	
3.3 V LVTTL/LVCMOS	27	40	65	kΩ

Table 53: Maximum Toggle Rate

Elitestek recommends that you perform simulations using the IBIS model to determine the maximum toggle rate for your design.

I/O Standard	Max Toggle Rate	Units
3.3 V LVTTL/LVCMOS	400	Mbps
2.5 V LVCMOS	400	Mbps
1.8 V LVCMOS	400	Mbps
LVDS	600	Mbps

Table 54: Single-Ended I/O and LVDS Pins Configured as Single-Ended I/O Rise and Fall Time

Data are based on the following IBIS simulation setup:

- Weakest drive strength model
- Typical simulation corner setting
- RLC circuit with 6.6 pF capacitance, 16.6 nH inductance, 0.095 ohm resistance, and 25 °C temperature

Note: For a more accurate data, you need to perform the simulation with your own circuit.

I/O Standard	Rise Time (T_R)		Fall Time (T_F)		Units
	Slow Slew Rate Enabled	Slow Slew Rate Disabled	Slow Slew Rate Enabled	Slow Slew Rate Disabled	
3.3 V LVTTL/LVCMOS	1.13	1.02	1.24	1.17	ns
2.5 V LVCMOS	1.4	1.3	1.44	1.31	ns
1.8 V LVCMOS	2.14	2.01	2.05	1.85	ns
LVDS pins configured as 3.3 V LVTTL/ LVCMOS	0.45		0.44		ns

Table 55: Block RAM Characteristics

Symbol	Description	Speed Grade		Units
		C3, C4L, I4L	C4, I4	
f_{MAX}	Block RAM maximum frequency.	310	400	MHz

Table 56: Multiplier Block Characteristics

Symbol	Description	Speed Grade		Units
		C3, C4L, I4L	C4, I4	
f_{MAX}	Multiplier block maximum frequency.	310	400	MHz

LVDS I/O Electrical and Timing Specifications (Q144)

The LVDS pins comply with the EIA/TIA-644 electrical specifications.

Note: The LVDS RX supports the sub-lvds, slvs, HiVcm, RSDS and 3.3 V LVPECL differential I/O standards with a transfer rate of up to 800 Mbps.

Table 57: LVDS I/O Electrical Specifications

Parameter	Description	Test Conditions/ Options	Min	Typ	Max	Unit
V_{CCIO}	LVDS I/O Supply Voltage	–	2.97	3.3	3.63	V
LVDS TX						
V_{OD}	Output Differential Voltage	Reduce VOD Swing option disabled	250	350	450	mV
		Reduce VOD Swing option enabled	150	200	250	mV
ΔV_{OD}	Change in V_{OD}	–	–	–	50	mV
V_{OCM}	Output Common Mode Voltage	RT = 100 Ω	1,125	1,250	1,375	mV
ΔV_{OCM}	Change in V_{OCM}	–	–	–	50	mV
V_{OH}	Output High Voltage	RT = 100 Ω	–	–	1475	mV
V_{OL}	Output Low Voltage	RT = 100 Ω	925	–	–	mV
I_{SAB}	Output Short Circuit Current	–	–	–	24	mA
LVDS RX						
V_{ID}	Input Differential Voltage	–	100	–	600	mV
V_{ICM}	Input Common Mode Voltage	–	100	–	2,000	mV
V_{TH}	Differential Input Threshold	–	-100	–	100	mV
I_{IL}	Input Leakage Current	–	–	–	20	µA

Figure 23: LVDS RX I/O Electrical Specification Waveform

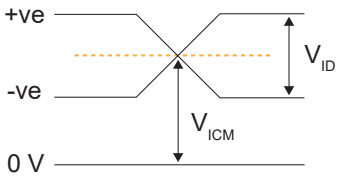


Table 58: LVDS Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t_{LVDS_CPA}	LVDS TX reference clock phase accuracy	-5	–	+5	%
t_{LVDS_skew}	LVDS TX lane-to-lane skew (edge-aligned)	–	–	200	ps
	LVDS TX lane-to-lane skew (center-aligned)	–	–	250	ps
t_{LVDS_SU}	LVDS RX Data to CLK setup time	344	–	–	ps
t_{LVDS_HD}	LVDS RX Data to CLK hold time	344	–	–	ps

Figure 24: LVDS RX Timing (Center-Aligned)

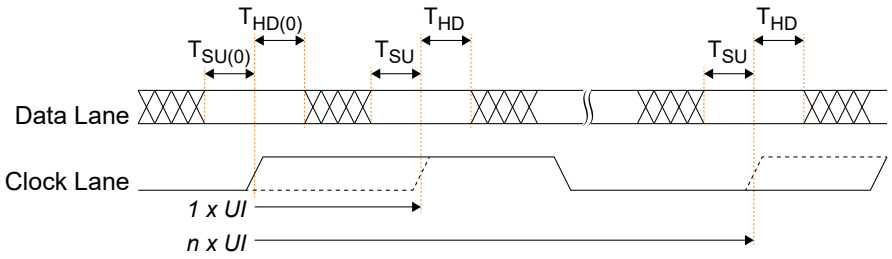
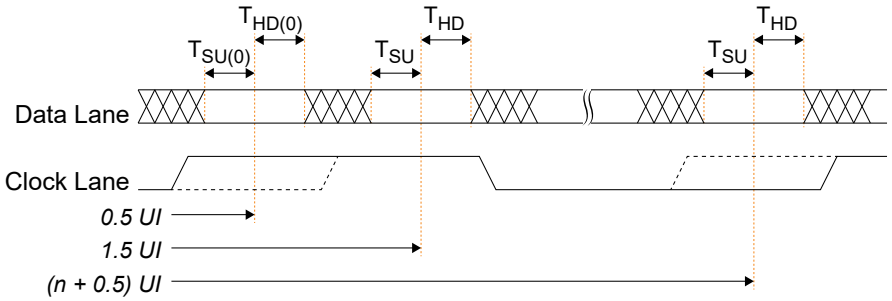


Figure 25: LVDS RX Timing (Edge-Aligned)



ESD Performance

Refer to the **Trion Reliability Report** for ESD performance data.

PLL Timing and AC Characteristics (F49 and F81)

The following tables describe the PLL timing and AC characteristics for the simple PLL in F49 and F81 packages.

Table 59: PLL Timing

Symbol	Parameter	Min	Typ	Max	Units
F_{PFD}	Phase frequency detector input frequency.	10	–	50	MHz
F_{OUT}	Output clock frequency.	0.25	–	400	MHz
F_{VCO}	PLL VCO frequency.	500	–	1200	MHz

Table 60: PLL AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{DT}	Output clock duty cycle.	40	50	60	%
t_{OPJIT} (PK - PK)	Output clock period jitter (PK-PK).	–	100	–	ps
t_{INDT}	Input clock duty cycle.	45	–	55	%
t_{ILJIT} (PK - PK)	Input clock long-term jitter (PK-PK)	–	–	800	ps
t_{LOCK}	PLL pull in plus lock-in time.	–	–	0.5	ms

PLL Timing and AC Characteristics (Q144)

The following tables describe the PLL timing and AC characteristics for the advanced PLL in Q144 packages.

Table 61: PLL Timing (C3, C4, and I4)

Symbol	Parameter	Min	Typ	Max	Units
F_{IN} [19]	Input clock frequency from core.	10	–	330	MHz
	Input clock frequency from GPIO.	10	–	200	MHz
	Input clock frequency from LVDS.	10	–	400	MHz
F_{OUT}	Output clock frequency.	0.24	–	500	MHz
F_{VCO}	PLL VCO frequency for internal feedback mode.	500	–	1,600	MHz
	PLL VCO frequency for local and core feedback mode	500	–	3,600	MHz
F_{PLL}	Post-divider PLL VCO frequency if all output divider values <= 64	62.5	–	1,800	MHz
	Post-divider PLL VCO frequency if any of the output divider value > 64	62.5	–	1,400	MHz
F_{PFD}	Phase frequency detector input frequency.	10	–	100	MHz

Table 62: PLL Timing (C4L and I4L)

Symbol	Parameter	Min	Typ	Max	Units
F_{IN} [19]	Input clock frequency from core.	10	–	330	MHz
	Input clock frequency from GPIO.	10	–	200	MHz
	Input clock frequency from LVDS.	10	–	400	MHz
F_{OUT}	Output clock frequency.	0.24	–	500	MHz
F_{VCO}	PLL VCO frequency for internal feedback mode.	500	–	1,600	MHz
	PLL VCO frequency for local and core feedback mode	500	–	3,200	MHz
F_{PLL}	Post-divider PLL VCO frequency if all output divider values <= 64	62.5	–	1,600	MHz
	Post-divider PLL VCO frequency if any of the output divider value > 64	62.5	–	1,200	MHz
F_{PFD}	Phase frequency detector input frequency.	10	–	100	MHz

[19] When using the Dynamic clock source mode, the maximum input clock frequency is limited by the slowest clock frequency of the assigned clock source. For example, the maximum input clock frequency of a Dynamic clock source mode from core and GPIO is 200 MHz.

Table 63: PLL AC Characteristics[20]

Symbol	Parameter	Min	Typ	Max	Units
t_{DT}	Output clock duty cycle.	40	50	60	%
t_{OPJIT} (PK - PK) [21]	Output clock period jitter (PK-PK).	–	–	200	ps
t_{PLL_HLW}	PLL input clock from GPIO, HIGH/LOW pulse width.	2.25	–	–	ns
	PLL input clock from LVDS, HIGH/LOW pulse width.	1.13	–	–	ns
t_{ILJIT} (PK - PK)	Input clock long-term jitter (PK-PK)	–	–	800	ps
t_{LOCK}	PLL lock-in time.	–	–	0.5	ms

Internal Oscillator (F49 and F81)

The internal oscillator has the following specifications.

Table 64: Internal Oscillator Specifications

Symbol	Parameter	Min	Typ	Max	Units
F_{CLKOSC}	Oscillator clock frequency.	–	10	–	kHz
D_{CHOSC}	Duty cycle.	45	50	55	%

[20] Test conditions at 3.3 V and room temperature.
[21] The output jitter specification applies to the PLL jitter when an input jitter of 20 ps is applied.

Configuration Timing

The T8 FPGA has the following configuration timing specifications. Refer to **AN 006: Configuring Trion FPGAs** for detailed configuration information.

Table 65: Timing Parameters for All Modes

Symbol	Parameter	Min	Typ	Max	Units
t_{CRESET_N}	Minimum creset_n low pulse width required to trigger re-configuration.	320	–	–	ns
t_{USER}	Minimum configuration duration after CDONE goes high before entering user mode.[22][23] Test condition at 10 kΩ pull-up resistance and 10 pF output loading on CDONE pin.	12	–	[24]	µs

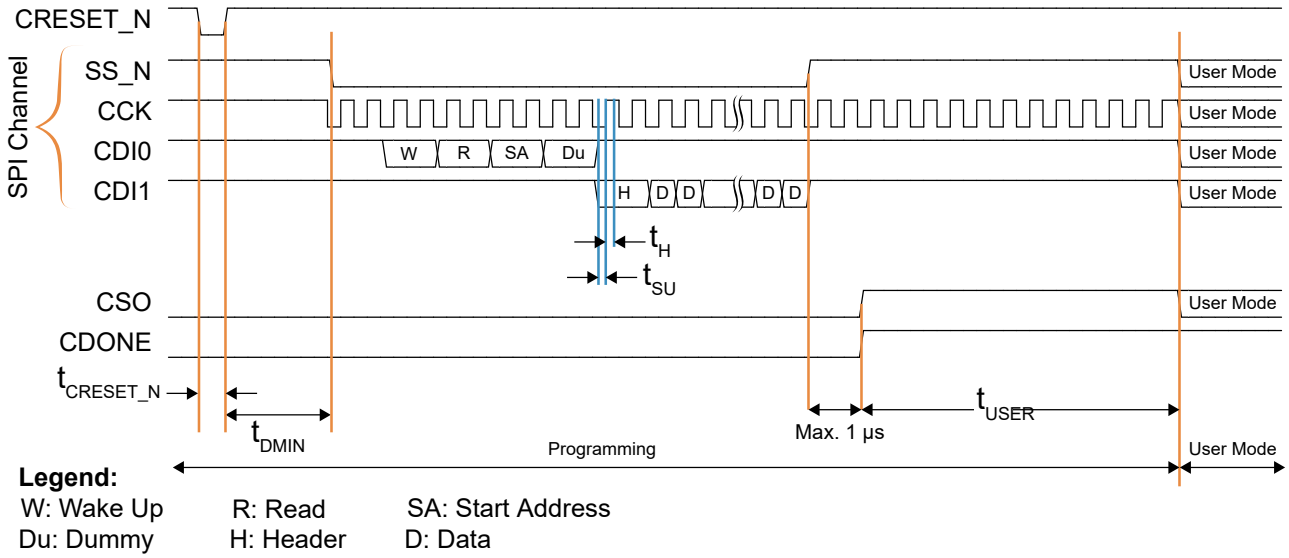
[22] The FPGA may go into user mode before t_{USER} has elapsed. However, Elitestek recommends that you keep the system interface to the FPGA in reset until t_{USER} has elapsed.

[23] For JTAG programming, the min t_{USER} configuration time is required after CDONE goes high and FPGA receives the ENTERUSER instruction from JTAG host (TAP controller in UPDATE_IR state).

[24] See **Maximum tUSER for SPI Active and Passive Modes** on page 47

SPI Active

Figure 26: SPI Active Mode (x1) Timing Sequence



The JTAG pins must be inactive during SPI active configuration.

Table 66: Active Mode Timing Parameters

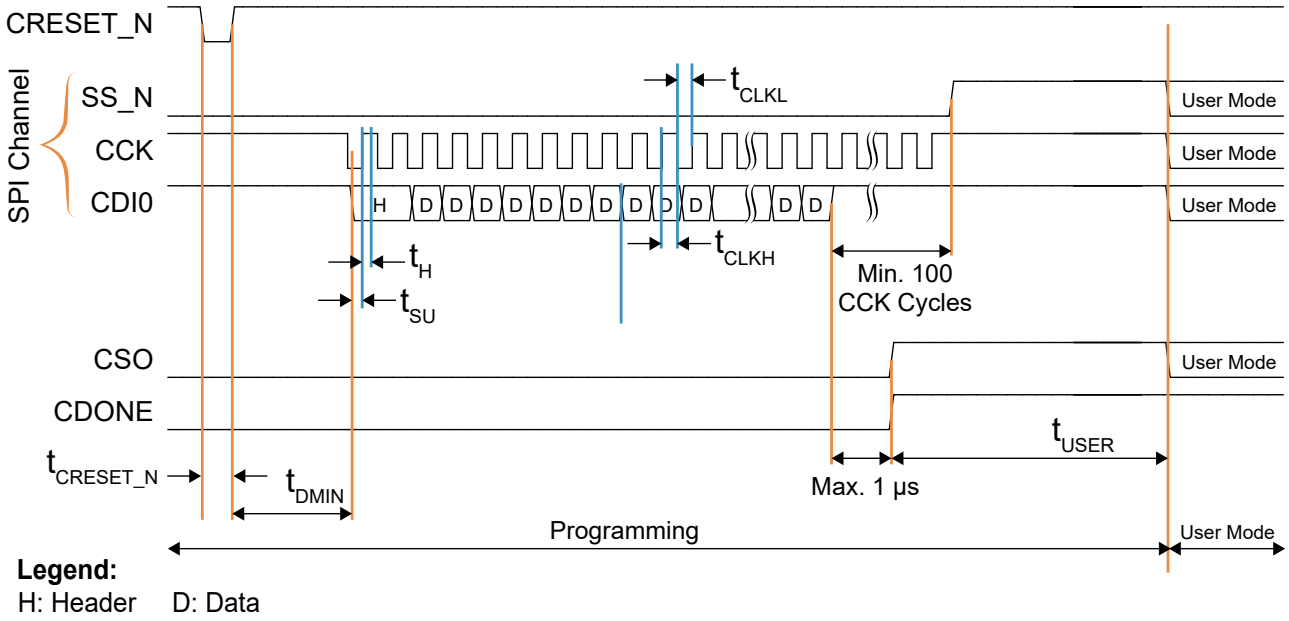
Symbol	Parameter	Frequency	Min	Typ	Max	Units
f_{MAX_M}	Active mode configuration clock frequency[25].	DIV4	14	20	26	MHz
		DIV8	7	10	13	MHz
t_{SU}	Setup time. Test condition at 3.3 V I/O standard and 0 pF output loading.	–	7.5	–	–	ns
t_H	Hold time. Test condition at 3.3 V I/O standard and 0 pF output loading.	–	1	–	–	ns
t_{DMIN}	Minimum time between deassertion of CRESET_N to first valid configuration data.	–	1.2	–	–	µs

Note: Refer to **Power Up Sequence** on page 27 for details on the power-up requirements.

[25] For parallel daisy chain x2 and x4, the active configuration clock frequency, fMAX_M, must be set to DIV4.

SPI Passive

Figure 27: SPI Passive Mode (x1) Timing Sequence



The JTAG pins must be inactive during SPI passive configuration.

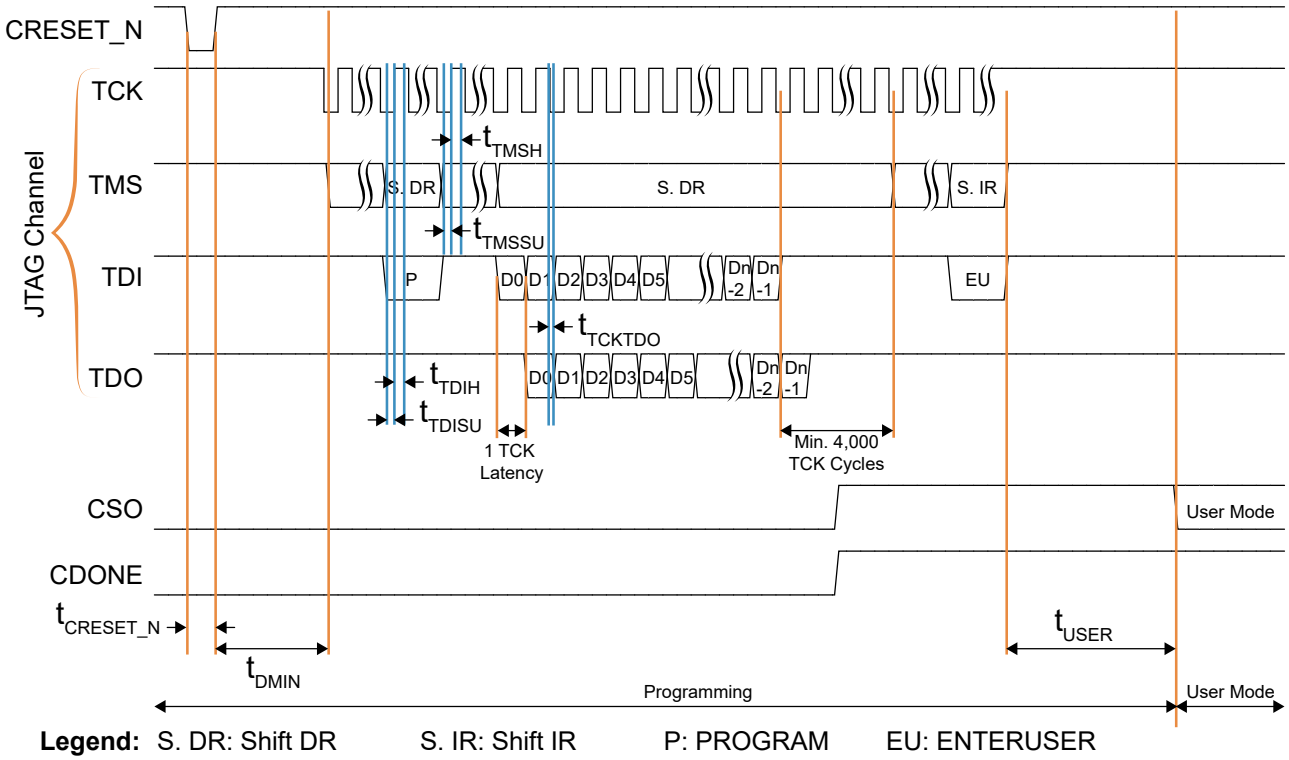
Table 67: Passive Mode Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
f_{MAX_S}	Passive mode X1 configuration clock frequency.	–	–	25	MHz
	Passive mode X2, X4 or X8 configuration clock frequency.	–	–	50	MHz
t_{CLKH}	Configuration clock pulse width high.	0.48*1/ f_{MAX_S}	–	–	ns
t_{CLKL}	Configuration clock pulse width low.	0.48*1/ f_{MAX_S}	–	–	ns
t_{SU}	Setup time. (F49 and F81)	4	–	–	ns
t_{SU}	Setup time. (Q144 packages)	6	–	–	ns
t_H	Hold time.	1	–	–	ns
t_{DMIN}	Minimum time between deassertion of CRESET_N to first valid configuration data.	1.2	–	–	µs

Note: Refer to **Power Up Sequence** on page 27 for details on the power-up requirements.

JTAG

Figure 28: JTAG Programming Waveform



Legend: S. DR: Shift DR S. IR: Shift IR P: PROGRAM EU: ENTERUSER

The SPI bus must be inactive during JTAG configuration.

Important: Refer to **Power Up Sequence** on page 27 for power-up details.

Table 68: JTAG Mode Timing Parameters

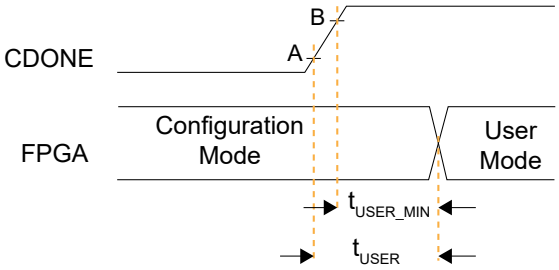
Symbol	Parameter	Min	Typ	Max	Units
f_{TCK}	TCK frequency.	–	–	25	MHz
t_{TDISU}	TDI setup time.	3.5	–	–	ns
t_{TDIH}	TDI hold time.	1	–	–	ns
t_{TMSSU}	TMS setup time.	3	–	–	ns
t_{TMSH}	TMS hold time.	1	–	–	ns
t_{TCKTDO}	TCK falling edge to TDO output.	–	–	10.5[26]	ns
t_{DMIN}	Minimum time between deassertion of CRESET_N to first valid configuration data.	1.2	–	–	µs

Note: Refer to **Power Up Sequence** on page 27 for details on the power-up requirements.

[26] 0 pf output loading.

Maximum t_{USER} for SPI Active and Passive Modes

The following waveform illustrates the minimum and maximum values for t_{USER}.



- *Point A*—User-defined trigger point to start counter on t_{USER}
- *Point B*—V_{IH} (with Schmitt Trigger) of Trion I/Os

The maximum t_{USER} value can be derived based on the following formula:

Table 69: t_{USER} Maximum

Configuration Setup	t_{USER} Maximum
Single Trion FPGA	$t_{USER} = t_{(from\ A\ to\ B)} + t_{USER\_MIN}$
Slave FPGA in a dual-Trion FPGA SPI chain	
Master FPGA in a dual-Trion FPGA SPI chain	t_{USER} = (1344 / SPI_WIDTH) * CCK period + t_{USER_MIN} + $t_{(from\ A\ to\ B)}$

Pinout Description

The following tables describe the pinouts for power, ground, configuration, and interfaces.

Table 70: General Pinouts

Function	Group	Direction	Description
VCC	Power	–	Core power supply.
VCCA_*xx*	Power	–	PLL analog power supply. *xx* indicates location: TL: Top left, TR: Top right, BR: bottom right
VCCA_PLL	Power	–	PLL analog power supply.
VCCIO	Power	–	I/O pin power supply.
VCCIO*xx*	Power	–	I/O pin power supply. *xx* indicates the bank location: 1A: Bank 1A, 3E: Bank 3E 4A: Bank 4A (only for 3.3 V) , 4B: Bank 4B (only for 3.3 V)
VCCIO*xx_yy_zz*	Power	–	Power for I/O banks that are shorted together. *xx*, *yy*, and *zz* are the bank locations. For example: VCCIO1B_1C shorts banks 1B and 1C VCCIO3C_TR_BR shorts banks 3C, TR, and BR
GND	Ground	–	Ground.
GNDA_PLL	Ground	–	PLL ground pin.
CLK*n*	Alternate	Input	Global clock network input. *n* is the number. The number of inputs is package dependent.
CTRL*n*	Alternate	Input	Global network input used for high fanout and global reset. *n* is the number. The number of inputs is package dependent.
PLLIN	Alternate	Input	PLL reference clock resource. There are 5 PLL reference clock resource assignments (depending on the package). Assign the reference clock resource based on the PLL you are using.
MREFCLK	Alternate	Input	MIPI TX PLL reference clock source.
GPIO*x_n*	GPIO	I/O	General-purpose I/O for user function. User I/O pins are single-ended. *x*: Indicates the bank (L or R) *n*: Indicates the GPIO number.
GPIO*x_n_yyy* GPIO*x_n_yyy_zzz* GPIO*x_zzzn*	GPIO Multi-Function	I/O	Multi-function, general-purpose I/O. These pins are single ended. If these pins are not used for their alternate function, you can use them as user I/O pins. *x*: Indicates the bank; left (L), right (R), or bottom (B). *n*: Indicates the GPIO number. *yyy, yyy_zzz*: Indicates the alternate function. *zzzn*: Indicates LVDS TX or RX and number.
TXN*n*, TXP*n*	LVDS	I/O	LVDS transmitter (TX). *n*: Indicates the number.
RXN*n*, RXP*n*	LVDS	I/O	LVDS receiver (RX). *n*: Indicates the number.
CLKN*n*, CLKP*n*	LVDS	I/O	Dedicated LVDS receiver clock input. *n*: Indicates the number.
RXN*n*_EXTFB*n* RXP*n*_EXTFB*n*	LVDS	I/O	LVDS PLL external feedback. *n*: Indicates the number.
REF_RES	–	–	REF_RES is a reference resistor to generate constant current for LVDS TX. Connect a 12 kΩ resistor with a tolerance of ±1% to the REF_RES pin with respect to ground. If none of the pins in a bank are used for LVDS, leave this pin floating.

Table 71: Dedicated Configuration Pins

These pins cannot be used as general-purpose I/O after configuration.

All the pins are in internal weak pull-up during configuration except for `TCK` and `TDO`.

Pins	Direction	Description	External Weak Pull- Up/ Pull Down Requirement
CDONE	I/O	Configuration done status pin. CDONE is an open drain output; connect it to an external pull-up resistor to VCCIO. When CDONE = 1, the configuration is complete and the FPGA enters user mode. You can hold CDONE low and release it to synchronize the FPGAs entering user mode.	Pull up
CRESET_N	Input	Active-low FPGA reset and re-configuration trigger. Pulse CRESET_N low for a duration of t_{creset_N} before releasing CRESET_N from low to high to initiate FPGA re-configuration. This pin does not perform a system reset.	Pull up
TCK	Input	JTAG test clock input (TCK). The rising edge loads signals applied at the TAP input pins (TMS and TDI). The falling edge clocks out signals through the TAP TDO pin.	Pull up
TMS	Input	JTAG test mode select input (TMS). The I/O sequence on this input controls the test logic operation . The signal value typically changes on the falling edge of TCK. TMS has an internal weak pull-up; when it is not driven by an external source, the test logic perceives a logic 1.	Pull up
TDI	Input	JTAG test data input (TDI). Data applied at this serial input is fed into the instruction register or into a test data register depending on the sequence previously applied at TMS. Typically, the signal applied at TDI changes state following the falling edge of TCK while the registers shift in the value received on the rising edge. Like TMS, TDI has an internal weak pull-up; when it is not driven from an external source, the test logic perceives a logic 1.	Pull up
TDO	Output	JTAG test data output (TDO). This serial output from the test logic is fed from the instruction register or a test data register depending on the sequence previously applied at TMS. The shift out content is based on the issued instruction. The signal driven through TDO changes state following the falling edge of TCK. When data is not being shifted through the device, TDO is set to an inactive drive state (e.g., high-impedance).	Pull up

Note: All dedicated configuration pins have Schmitt Trigger buffer. See **Table 34: Single-Ended I/O and Dedicated Configuration Pins Schmitt Trigger Buffer Characteristic** on page 32 for the Schmitt Trigger buffer specifications.

Table 72: Dual-Purpose Configuration Pins

In user mode (after configuration), you can use these dual-purpose pins as general I/O.

Pins	Direction	Description	Use External Weak Pull-Up
CBUS[2:0]	Input	Configuration bus width select. CBUS has an internal weak pull-up. However, Elitestek recommends that you use an external pull-up accordingly. See *Selecting the Configuration Mode* in **AN 006: Configuring Trion FPGAs**.	Pull up or pull down[27]
CBSEL[1:0]	Input	Multi-image configuration selection pin. This function is not applicable to single-image bitstream configuration or internal reconfiguration (remote update). Connect CBSEL[1:0] to the external resistors for the image you want to use: 00 for image 1 01 for image 2 10 for image 3 11 for image 4 0: Connect to an external weak pull down. 1: Connect to an external weak pull up.	Pull up or pull down [28]
CCK	I/O	Passive SPI input configuration clock or active SPI output configuration clock (active low). Includes an internal weak pull-up.	Optional[29]
CDI*n*	I/O	*n* is a number from 0 to 31 depending on the SPI configuration. 0: Passive serial data input or active serial output. 1: Passive serial data output or active serial input. *n*: Parallel I/O. In multi-bit daisy chain connection, the CDI (31:0) connects to the data bus in parallel.	Optional[29]
CSI	Input	Chip select. 0: The FPGA is not selected or enabled and will not be configured. 1: Selects the FPGA for all configuration modes. CSI must remain high throughout all configuration modes.	Pull up
CSO	Output	Chip select output. Selects the next device for cascading configuration.	N/A
NSTATUS	Output	Status (active low). Indicates a configuration error. When the FPGA drives this pin low, it indicates either a device mismatch or a failed bitstream CRC check. Refer to **Table 73: I/O Pin States** on page 51. For F49, and T8 F81 packages, logic low indicates a configuration error due to ID mismatch.	N/A
SS_N	Input	SPI configuration mode select. The FPGA senses the value of SS_N when it comes out of reset (i.e., CRESET_N transitions from low to high). 0: SPI Passive mode; connect to external weak pull down. 1: SPI Active mode; connect to external weak pull up. In active configuration mode, SS_N is an active-low chip select to the flash device (CDI0 - CDI3).	Optional[29]
TEST_N	Input	Active-low test mode enable signal. Set to 1 to disable test mode. During all configuration modes, rely on the external weak pull-up or drive this pin high.	Pull up
RESERVED_OUT	Output	Reserved pin during user configuration. This pin drives high during user configuration. F49 and F81 packages only.	N/A

(27) Optional for x1 mode.
(28) Not applicable to single-image or remote update.
(29) Optional unless pull-up is required by external load.

Pin States

GPIO pins have as internal pull up/down (see **Figure 7: I/O Interface Block** on page 14 and **Figure 10: I/O Interface Block** on page 17), and LVDS pins used as GPIO have a weak pull up. The following table shows the pin state during reset, configuration, and when unused in user mode.

Table 73: I/O Pin States

Pin Type	During Reset (CRESET_N Low)	During Configuration (CRESET_N High, CDONE Low)	When Unused in User Mode (Default)
User Pins			
GPIO	Input tri-state with weak pull up.	Input tri-state with weak pull up.	Input tri-state with weak pull up.(30)
LVDS used as GPIO	Input tri-state with no weak pull up or pull down.	Input tri-state with no weak pull up or pull down.	Input tri-state with weak pull up.
Dual-Purpose Configuration Pins			
CSO	0	0(31)	Input tri-state with weak pull up.
NSTATUS	1	1(32)	Input tri-state with weak pull up.
CCK	Input tri-state with weak pull up.	SPI active output clock. SPI passive input with weak pull up.	Input tri-state with weak pull up.
CDI0	Input tri-state with weak pull up.	SPI active output. SPI passive input with weak pull up.	Input tri-state with weak pull up.

As shown in **Power Up Sequence** on page 27, `CRESET_N` must be kept low during power up.

Note: Refer to the following tables for details:
Table 36: Single-Ended I/O Internal Weak Pull-Up and Pull-Down Resistance on page 32
Table 48: Single-Ended I/O Internal Weak Pull-Up and Pull-Down Resistance on page 36

Efinity Software Support

The Efinity® software provides a complete tool flow from RTL design to bitstream generation, including synthesis, place-and-route, and timing analysis. The software has a graphical user interface (GUI) that provides a visual way to set up projects, run the tool flow, and view results. The software also has a command-line flow and Tcl command console. The Efinity® software supports simulation flows using the ModelSim, NCSim, or free iVerilog simulators. An integrated hardware Debugger with Logic Analyzer and Virtual I/O debug cores helps you probe signals in your design. The software-generated bitstream file configures the T8 FPGA. The software supports the Verilog HDL, SystemVerilog, and VHDL languages.

T8 Interface Floorplan

Note: The numbers in the floorplan figures indicate the GPIO and LVDS number ranges. Some packages may not have all GPIO or LVDS pins in the range bonded out. Refer to the **T8 Pinout** for information on which pins are available in each package.

(30) You can change it to weak pull-down in the Interface Designer.
(31) CSO is driven to 1 when the bitstream is done transmitting (CDONE = 1).
(32) NSTATUS is driven to 0 if the FPGA detects an invalid bitstream (e.g., CRC error).

Figure 29: Floorplan Diagram for F49 and F81 Packages

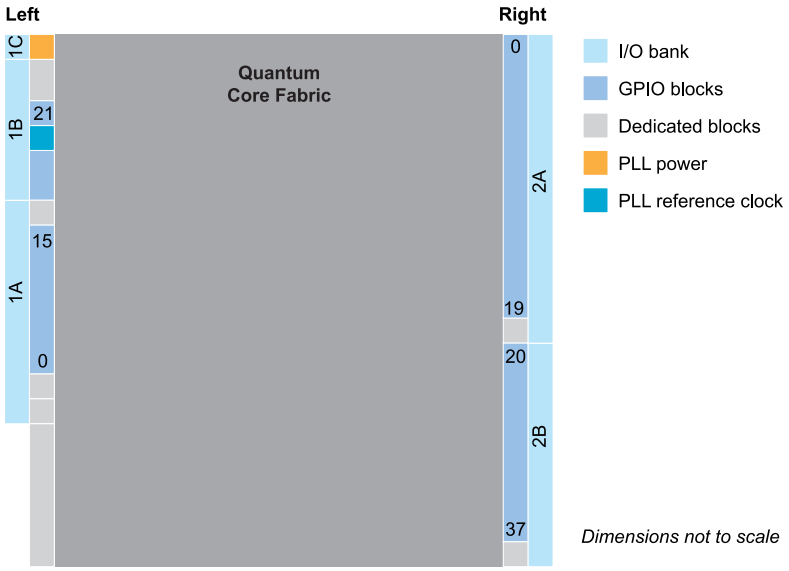
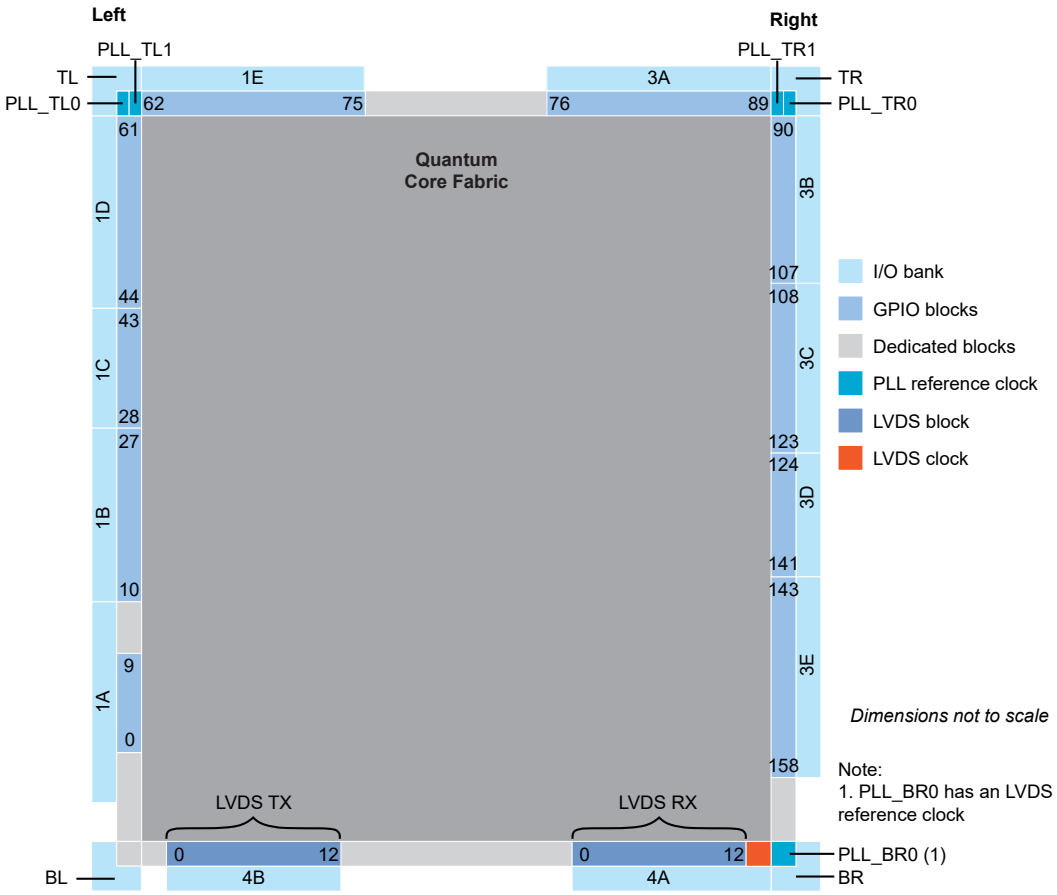


Figure 30: Floorplan Diagram for Q144 Packages



Ordering Codes

Refer to the **Trion Selector Guide** for the full listing of T8 ordering codes.

Revision History

Table 74: Revision History

Date	Version	Description
November 2025	5.5	Update **Unused Resources and Features** on page 28. (DOC-2610) Updated CBSEL[1:0] in **Table 72: Dual-Purpose Configuration Pins** on page 50.
April 2025	5.4	Fixed typo in **Table 66: Active Mode Timing Parameters** on page 44. (DOC-2500)
April 2025	5.3	Updated LVDS used as GPIO state in Pin States topic. Updated configuration timing waveforms. (DOC-2325) Moved information about unused resources to **Unused Resources and Features** on page 28.
November 2024	5.2	Updated GPIO interface pin names (IN to I and OUT to O). (DOC-2086) Fixed typo in **Table 72: Dual-Purpose Configuration Pins** on page 50. (DOC-2038) Footnote added to **Table 17: PLL Signals (Interface to FPGA Fabric)** on page 21 and **Table 13: PLL Pins** on page 16. (DOC-1939) Removed Dynamic Enable Pin Name from **Table 26: LVDS RX Settings in Efinity Interface Designer** on page 26. Pin does not exist in Trion family. (PT-2355) Added Pin States topic. (DOC-2087) SPI and JTAG pins should not be active at the same time for configuration. (DOC-2046) Renamed package prefix to match Efinity software (e.g., BGA changesd to F).
February 2024	5.1	Updated SPI passive timing waveform. Added note about external DC-biased circuit is required if the incoming LVDS signals are AC-coupled and link to Trion Hardware Design Checklist and Guidelines. (DOC-1532)
October 2023	5.0	Added LVDS RX Static Mode Delay Setting. (DOC-1473) Updated Maximum Toggle Rate table by adding recommendation to run simulation for actual toggle rate. (DOC-1468) Updated 2.5 V and 1.8 LVCMOS Single-Ended I/O Internal Weak Pull-Up and Pull-Down Resistance. (DOC-1476)
September 2022	4.9	Updated maximum LVDS toggle rate for Q144 package. (DOC-1441)
June 2023	4.8	Removed t_{LVDS_DT} and t_{INDT} specs, and replaced with t_{PLL_HLW} and t_{LVDS_CPA} for Q144 packages. (DOC-1189) Updated PLL LOCKED signal description. (DOC-1208)
April 2023	4.7	Corrected t_{LVDS_SU} and t_{LVDS_HD} specs (DOC-1070) Updated Advanced PLL RSTN signal description about de-asserting only when CLKIN is stable. (DOC-1226)
February 2023	4.6	Updated t_{LVDS_skew} specs. (DOC-1111) Updated t_{LVDS_SU} specs (DOC-1070) Updated power up sequence diagram. (DOC-954) Added note to use LVDS blocks from the same side to minimize skew. (DOC-1150) Updated Advanced PLL Settings table descriptions. (DOC-945)
November 2022	4.5	Added note recommending up to only 2 cascading advanced PLLs. (DOC-931) Corrected I_{OH} and I_{OL} in buffer drive strength characteristic specifications. (DOC-933) Updated F_{VCO}, F_{PLL}, and F_{PFD} Advanced PLL Timing parameter specifications and PLL Interface Designer Settings - Manual Configuration Tab notes. (DOC-1019) Added tLVDS_SU, tLVDS_HD specs and LVDS RX timing waveforms.
September 2022	4.4	Removed PLL_EXTFB from alternative input. (DOC-849) Updated Advanced PLL LOCKED signal description. (DOC-763)
April 2022	4.3	Updated test condition load to maximum load in Maximum Toggle Rate Table. (DOC-781) Updated note about leaving at least 2 pairs of unassigned LVDS pins between any GPIO and LVDS in the same device side. (DOC-769)

Date	Version	Description
March 2022	4.2	Updated supported maximum VCO frequency to 1,200 MHz for F49 and F81 packages. (DOC-722) Updated behaviour description for GPIO and LVDS as GPIO pins during configuration, and unused GPIO pins during user mode. (DOC-720) Added note about the block RAM content is random and undefined if it is not initialized. (DOC-729) Updated power supply ramp rate and power up sequence diagram. (DOC-631)
January 2022	4.1	Added LVDS Pins Configured as Single-Ended I/O Buffer Drive Strength Characteristics for Q144 packages.
January 2022	4.0	Corrected power supply ramp rate. (DOC-699)
January 2022	3.9	Removed LVDS Pins Configured as Single-Ended I/O Buffer Drive Strength Characteristics for Q144 packages. (DOC-679) Added Output Differential Voltage with Reduce VOD Swing option enabled specs. (DOC-648) Added maximum I/O pin input current, I_{IN}, and maximum per bank specs. (DOC-652) Added PLL input clock duty cycle, t_{INDT}, specs. (DOC-661) Updated CDONE pin direction as bidirectional. (DOC-672)
November 2021	3.8	Added storage temperature, T_{STG} spec. (DOC-560) Updated maximum JTAG mode TCK frequency, f_{TCK}. (DOC-574) Updated CSI pin description. (DOC-546) Updated LVDS Pins Configured as Single-Ended I/O Buffer Drive Strength specifications. (DOC-578) Update LVDS standard compliance which is TIA/EIA-644. (DOC-592) Updated t_{CLKH} and t_{CLKL}, and corrected SPI Passive Mode (x1) Timing Sequence waveform. (DOC-590) Updated REF_RES_*xx* description. (DOC-602, DOC-605) Updated Maximum Toggle Rate table. (DOC-630) Updated minimum Power Supply Ramp Rates. (DOC-631)
September 2021	3.7	Added Single-Ended I/O and LVDS Pins Configured as Single-Ended I/O Rise and Fall Time specs. (DOC-522) Added note to Active mode configuration clock frequency stating that for parallel daisy chain x2 and x4 configuration, f_{MAX_M}, must be set to DIV4. (DOC-528) Added Global Clock Location topic. (DOC-532) Added Maximum t_{USER} for SPI Active and Passive Modes topic. (DOC-535)
August 2021	3.6	Removed Static Supply Current parameter. (DOC-456) Added internal weak pull-up and pull-down resistor specs. (DOC-485) Updated table title for Single-Ended I/O Schmitt Trigger Buffer Characteristic. (DOC-507) Added note in Pinout Description stating all dedicated configuration pins have Schmitt Trigger buffer. (DOC-507)
June 2021	3.5	Updated CRESET_N pin description. (DOC-450)
April 2021	3.4	Updated PLL specs; t_{ILJIT} (PK - PK) and t_{DT}. (DOC-403) Added note about limiting number of LVDS as GPIO output and bidirectional per I/O bank to avoid switching noise. (DOC-411)
March 2021	3.3	Added LVDS TX reference clock output duty cycle and lane-to-lane skew specs. (DOC-416)
March 2021	3.2	The simple PLL output is negative edge aligned. (DOC-400)
February 2021	3.1	Added I/O input voltage, V_{IN} specification. (DOC-389) Added LVDS TX data and timing relationship waveform. (DOC-359) Added LVDS RX I/O electrical specification waveform. (DOC-346)

Date	Version	Description
December 2020	3.0	Updated NSTATUS pin description. (DOC-335) Added data for C4L and I4L DC speed grades. (DOC-268) Updated Advanced PLL reference clock input note by asking reader to refer to PLL Timing and AC Characteristics (Q144). (DOC-336) Added other PLL input clock frequency sources in PLL Timing and AC Characteristics (Q144). (DOC-336) Removed OE and RST from LVDS block as they are not supported in software. (DOC-328) Added a table to Power Up Sequence topic describing pin connection when PLL or GPIO is not used. (DOC-325) Updated f_{MAX_S} for passive configuration modes. (DOC-350)
September 2020	2.9	Updated pinout links.
August 2020	2.8	Removed typical standby (low power [LP] option) from static supply current table and updated typical standby value for F49 and F81 packages. Updated t_{USER} timing parameter values and added a note about the conditions for the values. Updated description for GPIO pins state during configuration to exclude LVDS as GPIO. Added operating junction temperature for industrial speed grade for F49 and F81 packages. Updated block RAM and multiplier block maximum frequencies to include I2 speed grade. Added f_{MAX} for single-ended I/O and LVDS configured as single-ended I/O. Added maximum power supply current transient during power-up.
July 2020	2.7	Removed preliminary note from F_{OUT}, F_{VCO}, t_{DT}, and t_{OPJIT}. These specifications are final. Updated timing parameter symbols in boundary scan timing waveform to reflect JTAG mode parameter symbols. Added supported GPIO features. Updated the maximum F_{VCO} for advanced PLL to 1,600 MHz. Updated the C divider requirement for the 90 degrees phase shift in the Advanced PLL Interface Designer Settings - Manual Configuration Tab. Removed LVDS electrical specifications note about RX differential I/O standard support. Added as a note in LVDS functional description topic. Added note to LVDS RX interface block diagram. Updated I/O bank names from TL_CORNER, BL_CORNER, TR_CORNER, and BR_CORNER to TL, BL, TR, and BR respectively. Updated the term DSP to multiplier. Updated power up sequence description about holding CRESET_N low. Updated PLLCLK pin name to PLL_CLKIN. Added PLL_EXTFB as an alternative input in GPIO signals table for complex I/O buffer. Updated PLL names in PLL reference clock resource assignments.
April 2020	2.6	Removed preliminary note from LVDS I/O electrical specification. These specifications are final.
February 2020	2.5	Added f_{MAX} for DSP blocks and RAM blocks. Added Trion power-up sequence. Updated number of global clocks and controls that can come from GPIO pins in package resources table.
December 2019	2.4	Updated PLL settings in the Interface Designer. Removed DIV1 and DIV2 active mode configuration frequencies; they are not supported. Added note to LVDS electrical specifications about RX differential I/O standard support.
October 2019	2.3	Added explanation that 2 unassigned pairs of LVDS pins should be located between and GPIO and LVDS pins in the same bank. Updated the reference clock pin assignments for TL_PLL0 and TL_PLL1. Added waveforms for configuration timing. Clarified I/O bank information.
September 2019	2.2	Minor clarifications.
August 2019	2.1	Updated formatting for I/O bank information.
August 2019	2.0	Added information about T8 FPGAs in 144-pin Q packages.

Date	Version	Description
February 2019	1.7	Removed incorrect footnote about LVDS under Available Package Options.
November 2018	1.6	Updated PLL interface description. Added packaging and floorplan information. Updated configuration timing and PLL timing information.
August 2018	1.5	Updated configuration pin table. Renamed RST PLL pin as RSTN.
August 2018	1.4	Updated standby current specifications. Updated ordering codes.
July 2018	1.3	Updated the PLL timing specification to add F_{PFD}. Clarified the slew rate description.
May 2018	1.2	Added ordering code information.
April 2018	1.1	Minor changes throughout.
December 2017	1.0	Initial release.