



# Trion<sup>®</sup> Packaging User Guide

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UG-TRION-PKG-v4.0  
December 2021  
[www.elitestek.com](http://www.elitestek.com)



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# Introduction

易灵思 offers Trion® FPGAs in packages that are designed for the device's maximum number of user I/O pins. This document describes Trion® FPGA pin and package specifications as well as solder reflow guidelines.



**Learn more:** Refer to the following documents for more information:

FPGA pinout specification

FPGA data sheet for pin definitions

## Available Package Options

*Table 1: Available Packages*

| Package                     | Dimensions (mm x mm) | Pitch (mm) |
|-----------------------------|----------------------|------------|
| <b>T4/T8 FPGAs</b>          |                      |            |
| 49-ball FBGA <sup>(1)</sup> | 3 x 3                | 0.4        |
| 81-ball FBGA                | 5 x 5                | 0.5        |
| <b>T20 FPGAs</b>            |                      |            |
| 80-ball WLCSP               | 4.5 x 3.6            | 0.4        |
| <b>T8/T20 FPGAs</b>         |                      |            |
| 144-pin QFP                 | 20 x 20              | 0.5        |
| <b>T13/T20 FPGAs</b>        |                      |            |
| 169-ball FBGA               | 9 x 9                | 0.65       |
| 256-ball FBGA               | 13 x 13              | 0.8        |
| <b>T20/T35 FPGAs</b>        |                      |            |
| 324-ball FBGA               | 12 x 12              | 0.65       |
| 400-ball FBGA               | 16 x 16              | 0.8        |
| <b>T55/T85/T120 FPGAs</b>   |                      |            |
| 324-ball FBGA               | 12 x 12              | 0.65       |
| 484-ball FBGA               | 18 x 18              | 0.80       |
| 576-ball FBGA               | 16 x 16              | 0.65       |

Refer to the FPGA data sheet for information on the number of GPIO and other resources in each FPGA/package combination.

<sup>(1)</sup> This package does not have dedicated JTAG pins (TDI, TDO, TCK, TMS).

## Device Pinout File

易灵思 provides pinout files for Trion® FPGAs. For each device/package combination, these files contain the pin name, I/O bank number for each pin, configuration function, and pin location.



**Download:** Download the pinout files from the Documentation page in the Support section of the 易灵思® web site ([www.elitestek.com/support](http://www.elitestek.com/support))

# Pinout Description

The following tables describe the pinouts for power, ground, configuration, and interfaces.

**Table 2: General Pinouts**

| Function                                         | Group     | Direction | Description                                                                                                                                                                                                 |
|--------------------------------------------------|-----------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VCC                                              | Power     | –         | Core power supply.                                                                                                                                                                                          |
| VCCIO <sub>xx</sub><br>VCCIO <sub>xx_yy_zz</sub> | Power     | –         | I/O pin power supply.<br>Power for I/O banks that are shorted together. <i>xx</i> , <i>yy</i> , and <i>zz</i> are the bank locations.                                                                       |
| VCCA <sub>xx</sub><br>VCCA_PLL                   | Power     | –         | PLL analog power supply.<br><i>xx</i> indicates the location.                                                                                                                                               |
| VCCIO                                            | Power     | –         | I/O pin power supply.                                                                                                                                                                                       |
| VCCA_PLL                                         | Power     | –         | PLL analog power supply.                                                                                                                                                                                    |
| VCCA <sub>xx</sub>                               | Power     | –         | PLL analog power supply. <i>xx</i> indicates location:<br>TL: Top left, TR: Top right, BR: bottom right                                                                                                     |
| VCCA <sub>xx</sub>                               | Power     | –         | PLL analog power supply. <i>xx</i> indicates the location.                                                                                                                                                  |
| VCCIO <sub>xx</sub>                              | Power     | –         | I/O pin power supply. <i>xx</i> indicates the bank location:<br>1A: Bank 1A, 3E: Bank 3E<br>4A: Bank 4A (only for 3.3 V) , 4B: Bank 4B (only for 3.3 V)                                                     |
| VCCIO <sub>xx</sub>                              | Power     | –         | I/O pin power supply. <i>xx</i> indicates the bank location.                                                                                                                                                |
| VCCIO <sub>xx_yy_zz</sub>                        | Power     | –         | Power for I/O banks that are shorted together. <i>xx</i> , <i>yy</i> , and <i>zz</i> are the bank locations. For example:<br>VCCIO1B_1C shorts banks 1B and 1C<br>VCCIO3C_TR_BR shorts banks 3C, TR, and BR |
| GND                                              | Ground    | –         | Ground.                                                                                                                                                                                                     |
| GNDA_PLL                                         | Ground    | –         | (T4/T8) PLL ground pin.                                                                                                                                                                                     |
| GNDA_PLL                                         | Ground    | –         | PLL ground pin.                                                                                                                                                                                             |
| CLK <sub>n</sub>                                 | Alternate | Input     | Global clock network input. <i>n</i> is the number. The number of inputs is package dependent.                                                                                                              |
| CTRL <sub>n</sub>                                | Alternate | Input     | Global network input used for high fanout and global reset. <i>n</i> is the number. The number of inputs is package dependent.                                                                              |
| PLLIN                                            | Alternate | Input     | PLL reference clock.                                                                                                                                                                                        |
| PLLIN                                            | Alternate | Input     | (T4) PLL reference clock.                                                                                                                                                                                   |
| PLLIN                                            | Alternate | Input     | (T8) PLL reference clock resource. There are 5 PLL reference clock resource assignments (depending on the package). Assign the reference clock resource based on the PLL you are using.                     |
| PLLIN                                            | Alternate | Input     | (T13/T20) PLL reference clock resource. There are 5 PLL reference clock resource assignments. Assign the reference clock resource based on the PLL you are using.                                           |
| PLLIN                                            | Alternate | Input     | (T35) PLL reference clock resource. There are 7 PLL reference clock resource assignments. Assign the reference clock resource based on the PLL you are using.                                               |

| Function                                     | Group                     | Direction | Description                                                                                                                                                                                                                                                                                                                                                                                                                  |
|----------------------------------------------|---------------------------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PLLIN                                        | Alternate                 | Input     | (T55/T85/T120) PLL reference clock resource. There are 7 (BGA324) or 8 (BGA484 and BGA576) PLL reference clock resource assignments. Assign the reference clock resource based on the PLL you are using.                                                                                                                                                                                                                     |
| MREFCLK                                      | Alternate                 | Input     | MIPI PLL reference clock source.                                                                                                                                                                                                                                                                                                                                                                                             |
| GPIOx_n                                      | GPIO                      | I/O       | General-purpose I/O for user function. User I/O pins are single-ended.<br>x: Indicates the bank (L or R)<br>n: Indicates the GPIO number.                                                                                                                                                                                                                                                                                    |
| GPIOx_n_yyy<br>GPIOx_n_yyy_zzz<br>GPIOx_zzzn | GPIO<br>Multi<br>Function | I/O       | Multi-function, general-purpose I/O. These pins are single ended. If these pins are not used for their alternate function, you can use them as user I/O pins.<br>x: (T4) Indicates the bank; left (L) or right (R).<br>x: (T13/T20) Indicates the bank; left (L), right (R), or bottom (B).<br>n: Indicates the GPIO number.<br>yyy, yyy_zzz: Indicates the alternate function.<br>zzzn: Indicates LVDS TX or RX and number. |
| TXNn, TXPn                                   | LVDS                      | I/O       | LVDS transmitter (TX). n: Indicates the number.                                                                                                                                                                                                                                                                                                                                                                              |
| RXNn, RXPn                                   | LVDS                      | I/O       | LVDS receiver (RX). n: Indicates the number.                                                                                                                                                                                                                                                                                                                                                                                 |
| CLKNn, CLKPn                                 | LVDS                      | I/O       | Dedicated LVDS receiver clock input. n: Indicates the number.                                                                                                                                                                                                                                                                                                                                                                |
| RXNn_EXTFBn<br>RXPn_EXTFBn                   | LVDS                      | I/O       | LVDS PLL external feedback. n: Indicates the number.                                                                                                                                                                                                                                                                                                                                                                         |
| REF_RES                                      | -                         | -         | REF_RES is a reference resistor to generate constant current for LVDS TX. Connect a 12 k $\Omega$ resistor with a tolerance of $\pm 1\%$ to the REF_RES pin with respect to ground. If none of the pins in a bank are used for LVDS, leave this pin floating.                                                                                                                                                                |

**Table 3: Dedicated Configuration Pins**

These pins cannot be used as general-purpose I/O after configuration.

| Pins     | Direction | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Use External Weak Pull-Up |
|----------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|
| CDONE    | Output    | Configuration done status pin. CDONE is an open drain output; connect it to an external pull-up resistor to VCCIO. When CDONE = 1, configuration is complete. If you hold CDONE low, the device will not enter user mode.                                                                                                                                                                                                                                                                                                                            | ✓                         |
| CRESET_N | Input     | Initiates FPGA re-configuration (active low). Pulse CRESET_N low for a duration of $t_{\text{creset\_N}}$ before asserting CRESET_N from low to high to initiate FPGA re-configuration. This pin does not perform a system reset.                                                                                                                                                                                                                                                                                                                    | ✓                         |
| TCK      | Input     | JTAG test clock input (TCK). The rising edge loads signals applied at the TAP input pins (TMS and TDI). The falling edge clocks out signals through the TAP TDO pin.                                                                                                                                                                                                                                                                                                                                                                                 | ✓                         |
| TMS      | Input     | JTAG test mode select input (TMS). The I/O sequence on this input controls the test logic operation. The signal value typically changes on the falling edge of TCK. TMS is typically a weak pull-up; when it is not driven by an external source, the test logic perceives a logic 1.                                                                                                                                                                                                                                                                | ✓                         |
| TDI      | Input     | JTAG test data input (TDI). Data applied at this serial input is fed into the instruction register or into a test data register depending on the sequence previously applied at TMS. Typically, the signal applied at TDI changes state following the falling edge of TCK while the registers shift in the value received on the rising edge. Like TMS, TDI is typically a weak pull-up; when it is not driven from an external source, the test logic perceives a logic 1.                                                                          | ✓                         |
| TDO      | Output    | JTAG test data output (TDO). This serial output from the test logic is fed from the instruction register or from a test data register depending on the sequence previously applied at TMS. During shifting, data applied at TDI appears at TDO after a number of cycles of TCK determined by the length of the register included in the serial path. The signal driven through TDO changes state following the falling edge of TCK. When data is not being shifted through the device, TDO is set to an inactive drive state (e.g., high-impedance). | ✓                         |



**Note:** All dedicated configuration pins have Schmitt Trigger buffer. See [Table 5](#)[Table 6](#)[Table 6](#)[Table 6](#) for the Schmitt Trigger buffer specifications.

**Table 4: Dual-Purpose Configuration Pins**

In user mode (after configuration), you can use these dual-purpose pins as general I/O.

| Pins         | Direction | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Use External Weak Pull-Up |
|--------------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|
| CBUS[2:0]    | Input     | Configuration bus width select. Connect to weak pull-up resistors if using default mode (x1).                                                                                                                                                                                                                                                                                                                                                                          | ✓                         |
| CBSEL[1:0]   | Input     | Optional multi-image selection input (if external multi-image configuration mode is enabled).                                                                                                                                                                                                                                                                                                                                                                          | N/A                       |
| CCK          | I/O       | Passive SPI input configuration clock or active SPI output configuration clock (active low). Includes an internal weak pull-up.                                                                                                                                                                                                                                                                                                                                        | N/A                       |
| CDIn         | I/O       | $n$ is a number from 0 to 31 depending on the SPI configuration.<br>0: Passive serial data input or active serial output.<br>1: Passive serial data output or active serial input.<br>$n$ : Parallel I/O.<br>In multi-bit daisy chain connection, the CDIn (31:0) connects to the data bus in parallel.                                                                                                                                                                | N/A                       |
| CSI          | Input     | Chip select.<br>0: The FPGA is not selected or enabled and will not be configured.<br>1: Selects the FPGA for configuration (SPI and JTAG configuration).                                                                                                                                                                                                                                                                                                              | ✓                         |
| CSO          | Output    | Chip select output. Selects the next device for cascading configuration.                                                                                                                                                                                                                                                                                                                                                                                               | N/A                       |
| NSTATUS      | Output    | T8 BGA49 and T8 BGA81:<br>Status (active low). Indicates a configuration error. When the FPGA drives this pin low, it indicates an ID mismatch.<br>T8 QFP144:<br>Status (active low). Indicates a configuration error. When the FPGA drives this pin low, it indicates an ID mismatch, the bitstream CRC check has failed, or remote update has failed.                                                                                                                | N/A                       |
| SS_N         | Input     | SPI slave select (active low). Includes an internal weak pull-up resistor to VCCIO during configuration. During configuration, the logic level samples on this pin determine the configuration mode. This pin is an input when sampled at the start of configuration (SS is low); an output in active SPI flash configuration mode.<br>The FPGA senses the value of SS_N when it comes out of reset (pulse CRESET_N low to high).<br>0: Passive mode<br>1: Active mode | ✓                         |
| TEST_N       | Input     | Active-low test mode enable signal. Set to 1 to disable test mode.<br>During configuration, rely on the external weak pull-up or drive this pin high.                                                                                                                                                                                                                                                                                                                  | ✓                         |
| RESERVED_OUT | Output    | Reserved pin during user configuration. This pin drives high during user configuration.<br>BGA49 and BGA81 packages only.                                                                                                                                                                                                                                                                                                                                              | N/A                       |



**Table 5: MIPI Pinouts (Dedicated)***n* Indicates the number. *L* indicates the lane

| Function                                             | Group  | Direction | Description                           |
|------------------------------------------------------|--------|-----------|---------------------------------------|
| VCC25A_MIPI0<br>VCC25A_MIPI1                         | Power  | -         | MIPI 2.5 V analog power supply.       |
| VCC12A_MIPI0_TX<br>VCC12A_MIPI1_TX                   | Power  | -         | MIPI 1.2 V TX analog power supply.    |
| VCC12A_MIPI0_RX<br>VCC12A_MIPI1_RX                   | Power  | -         | MIPI 1.2 V RX analog power supply.    |
| GNDA_MIPI                                            | Ground | -         | Ground for MIPI analog power supply.  |
| MIPI <sub>n</sub> _TXDPL<br>MIPI <sub>n</sub> _TXDNL | MIPI   | I/O       | MIPI differential transmit data lane. |
| MIPI <sub>n</sub> _RXDPL<br>MIPI <sub>n</sub> _RXDNL | MIPI   | I/O       | MIPI differential receive data lane.  |
| MREFCLK                                              | Clock  | Input     | MIPI PLL reference clock source.      |

**Table 6: DDR Pinouts (Dedicated)***n* indicates the number.

| Function              | Direction | Description                                              |
|-----------------------|-----------|----------------------------------------------------------|
| VCCIO_DDR             | -         | DDR power supply.                                        |
| DDR_A[ <i>n</i> ]     | Output    | Address signals to the memories.                         |
| DDR_BA[ <i>n</i> ]    | Output    | Bank signals to the memories.                            |
| DDR_CAS_N             | Output    | Active-low column address strobe signal to the memories. |
| DDR_CKE               | Output    | Active-high clock enable signals to the memories.        |
| DDR_CK<br>DDR_CK_N    | Output    | Differential clock output pins to the memories.          |
| DDR_CS_N              | Output    | Active-low chip select signals to the memories.          |
| DDR_DQ[ <i>n</i> ]    | I/O       | Data bus to/from the memories.                           |
| DDR_DM[ <i>n</i> ]    | Output    | Active-high data-mask signals to the memories.           |
| DDR_DQS_N[ <i>n</i> ] | I/O       | Differential data strobes to/from the memories.          |
| DDR_DQS[ <i>n</i> ]   | I/O       | Differential data strobes to/from the memories.          |
| DDR_ODT               | Output    | ODT signal to the memories.                              |
| DDR_RAS_N             | Output    | Active-low row address strobe signal to the memories.    |
| DDR_RST_N             | Output    | Active-low reset signals to the memories.                |
| DDR_WE_N              | Output    | Active-low write enable strobe signal to the memories.   |
| DDR_VREF              | I/O       | Reference voltage.                                       |
| DDR_ZQ                | I/O       | ZQ calibration pin.                                      |

# 49-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

**Figure 1: 49-Ball FBGA Pinout Diagram**

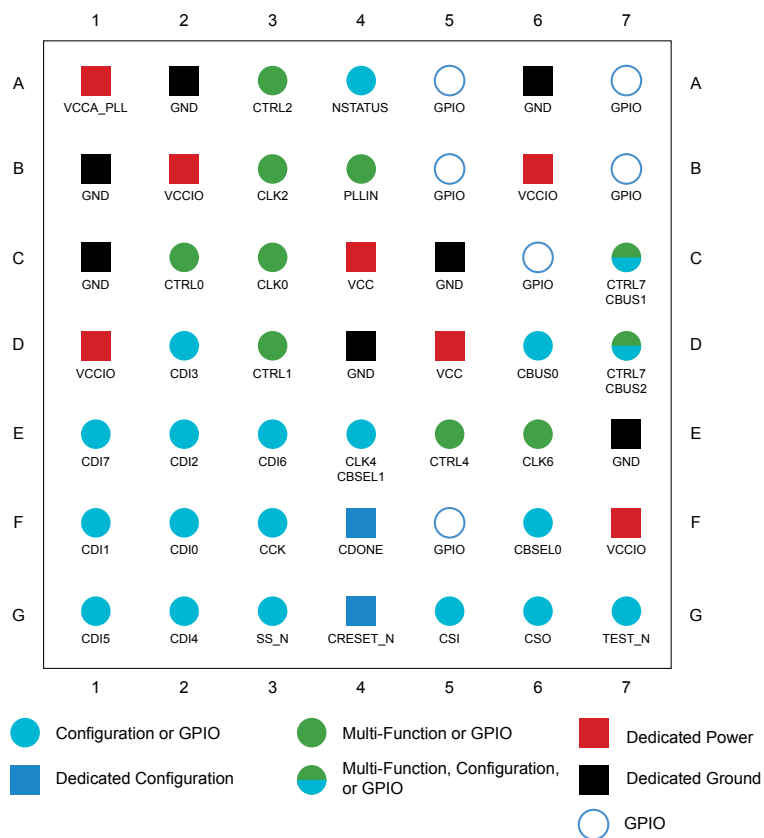


Figure 2: 49-Ball FBGA I/O Bank Diagram

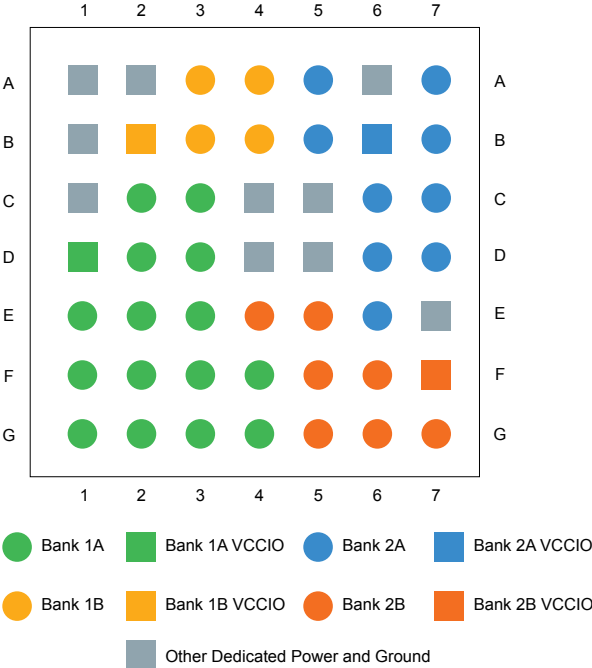


Figure 3: 49-Ball FPGA Package Marking

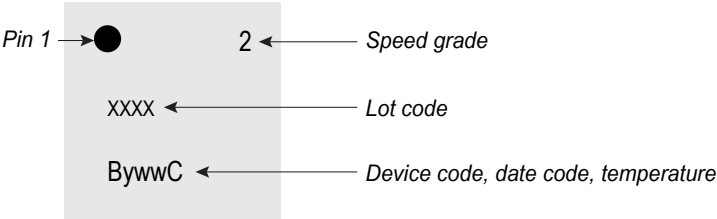
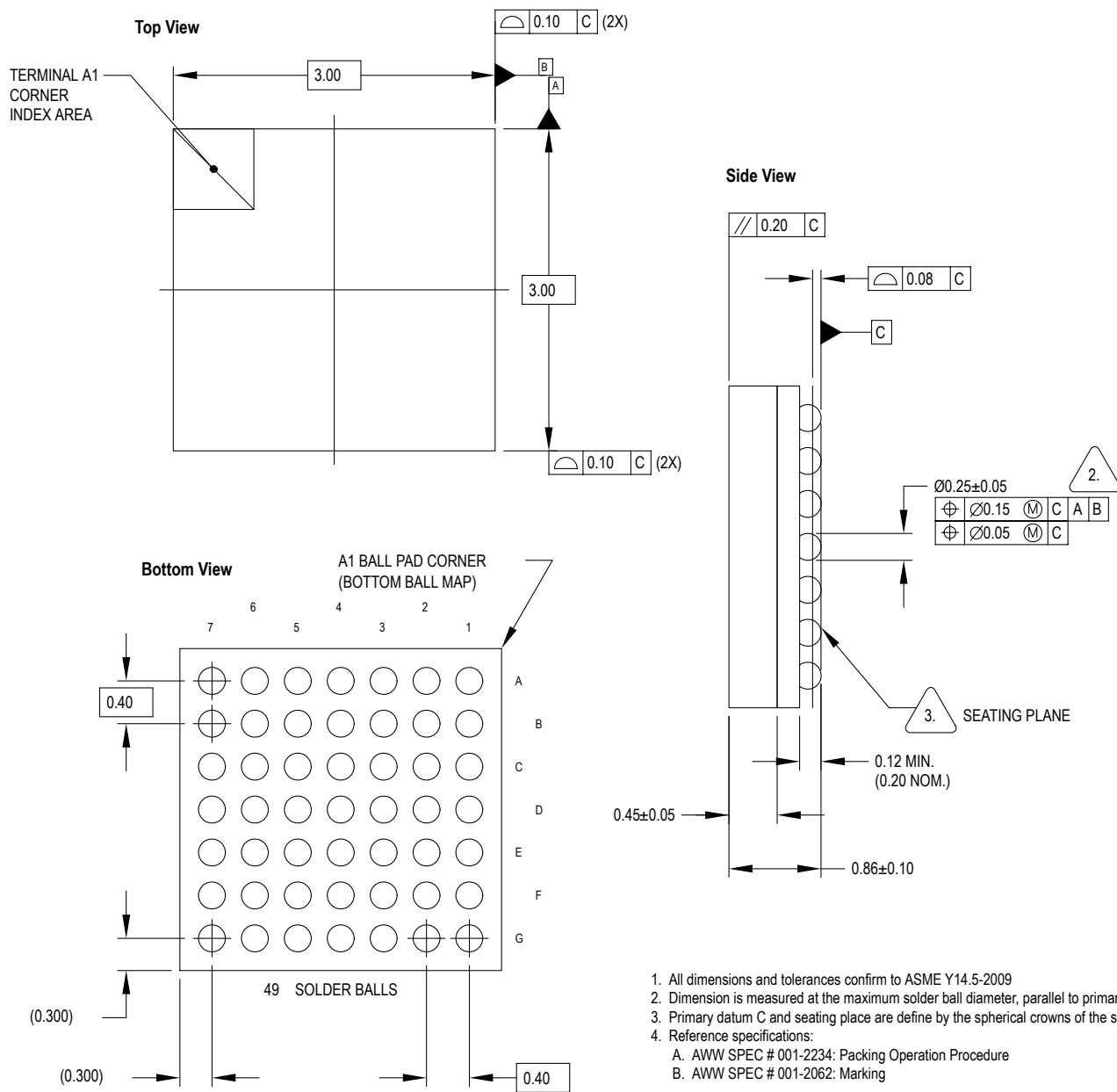


Figure 4: 49-Ball FBGA Package Outline



# 80-Ball WLCSP Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

**Figure 5: 80-Ball WLCSP Pinout Diagram**

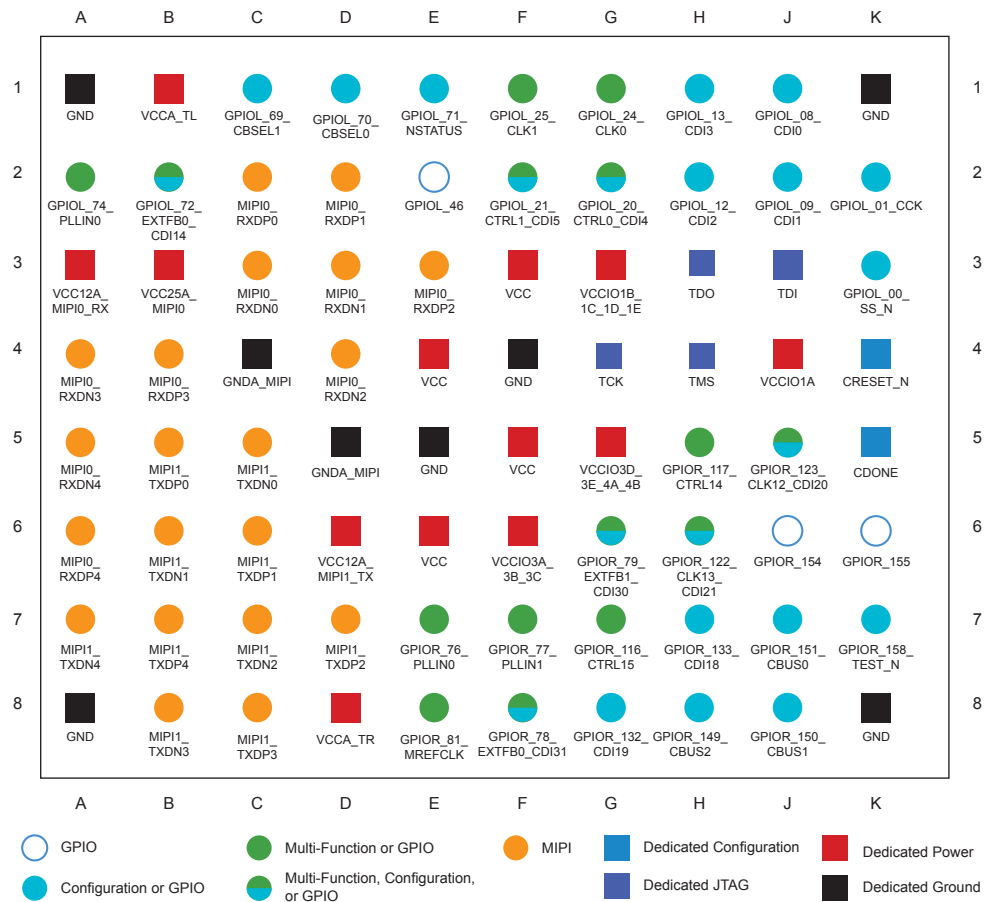


Figure 6: 80-Ball WLCSP I/O Bank Diagram

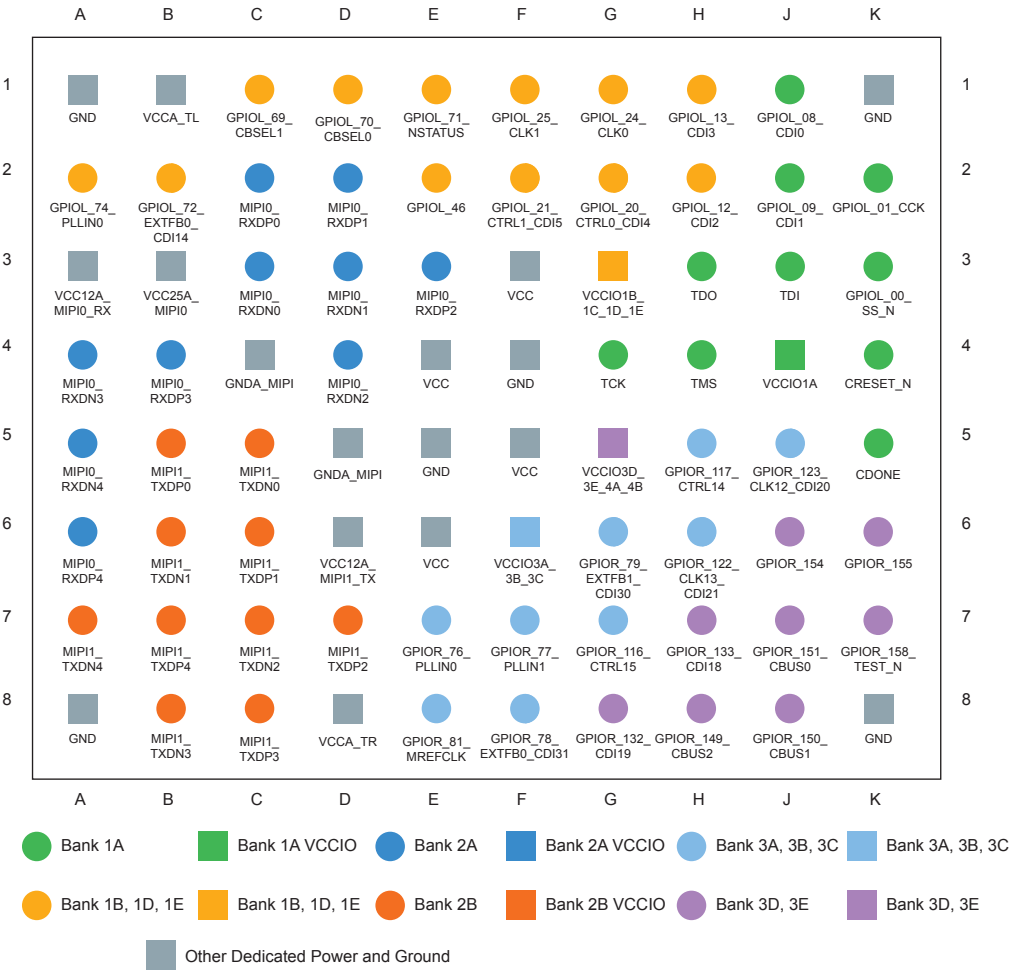


Figure 7: 80-Ball WLCSP Package Marking

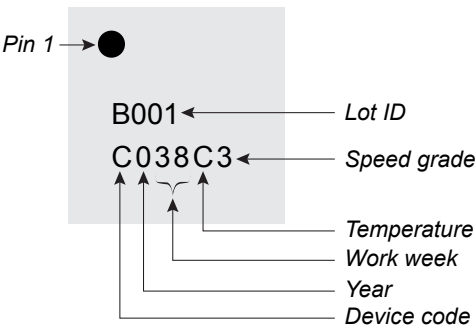
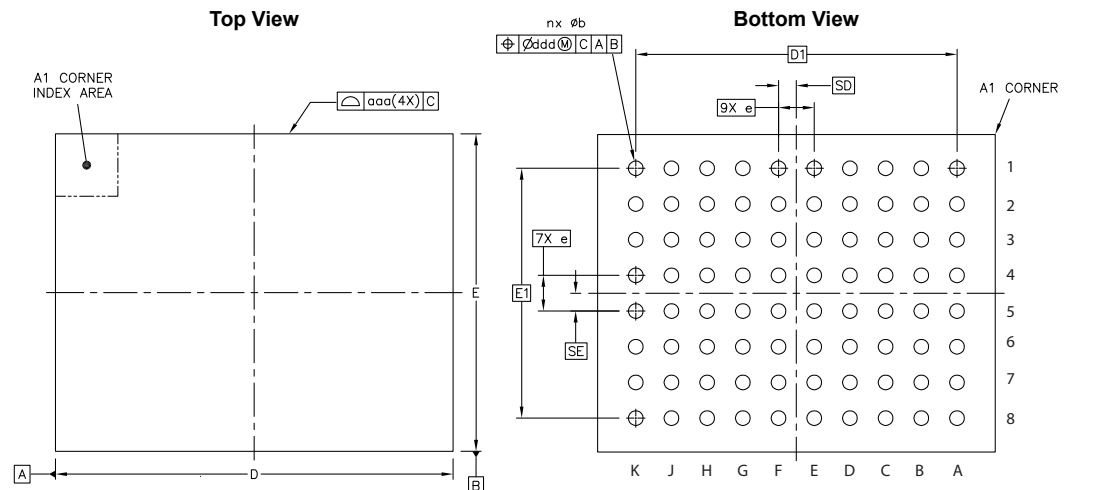
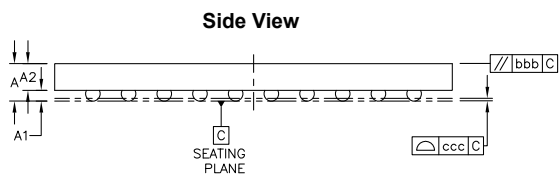


Figure 8: 80-Ball WLCSP Package Outline



|                            |   | SYMBOL | MIN    | NOM   | MAX   |
|----------------------------|---|--------|--------|-------|-------|
| TOTAL THICKNESS            |   | A      | 0.4    | 0.455 | 0.51  |
| STAND OFF                  |   | A1     | 0.125  | ---   | 0.185 |
| WAFER THICKNESS            |   | A2     | 0.275  | 0.3   | 0.325 |
| FILM THICKNESS             |   | A3     | ---    | ---   | ---   |
| BODY SIZE                  | Y | D      | 4.4567 |       |       |
|                            | X | E      | 3.5569 |       |       |
| BALL/BUMP PITCH            | Y | SD     | 0.2    | BSC   |       |
|                            | X | SE     | 0.2    | BSC   |       |
| EDGE BALL CENTER TO CENTER | Y | D1     | 3.6    | BSC   |       |
|                            | X | E1     | 2.8    | BSC   |       |
| PITCH                      |   | e      | 0.4    | BSC   |       |
| BALL DIAMETER (SIZE)       |   |        | 0.2    |       |       |
| BALL/BUMP WIDTH            |   | b      | 0.19   | ---   | 0.25  |
| BALL/BUMP COUNT            |   | n      | 80     |       |       |
| PACKAGE EDGE TOLERANCE     |   | aaa    | 0.03   |       |       |
| WAFER FLATNESS             |   | bbb    | 0.06   |       |       |
| COPLANARITY                |   | ccc    | 0.03   |       |       |
| BALL/BUMP OFFSET (PACKAGE) |   | ddd    | 0.015  |       |       |



# 81-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

**Figure 9: 81-Ball FBGA Pinout Diagram**

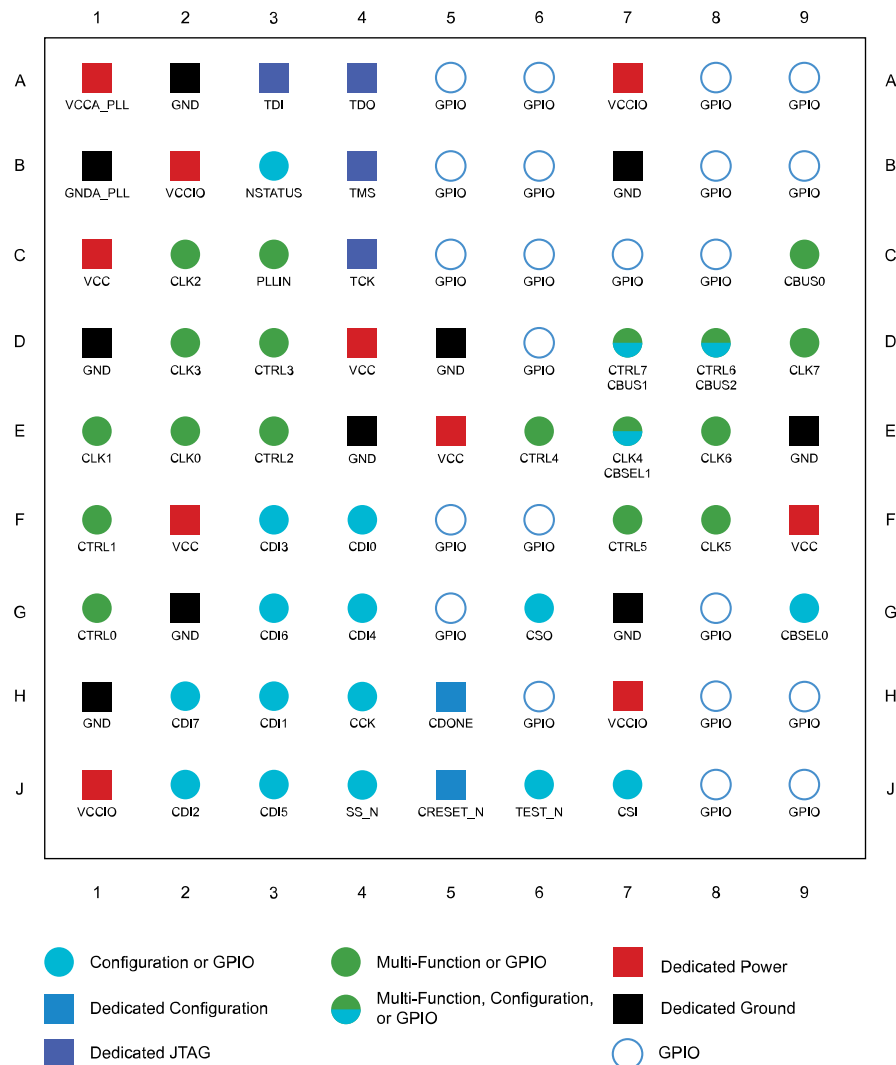




Figure 10: 81-Ball FBGA I/O Bank Diagram

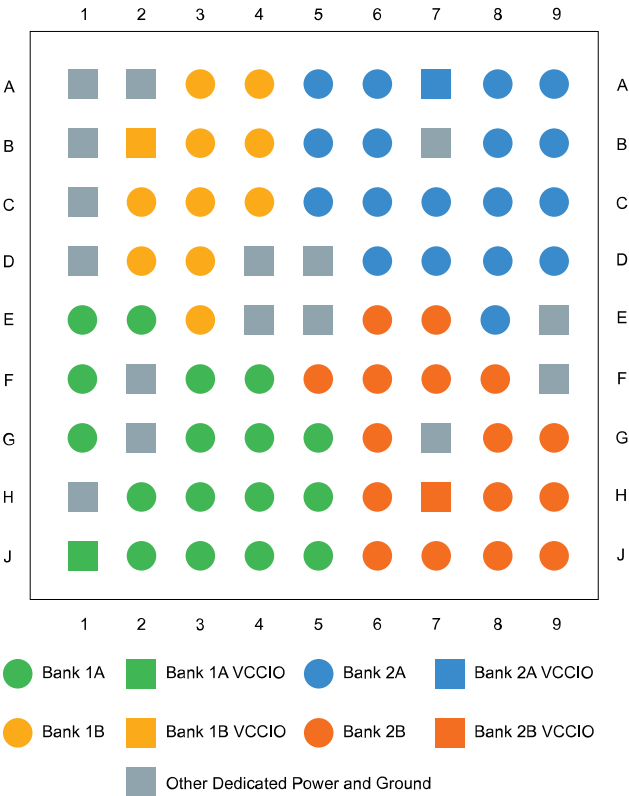


Figure 11: 81-Ball FPGA Package Marking

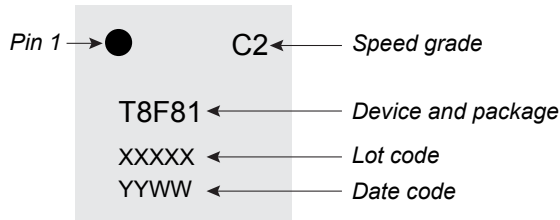
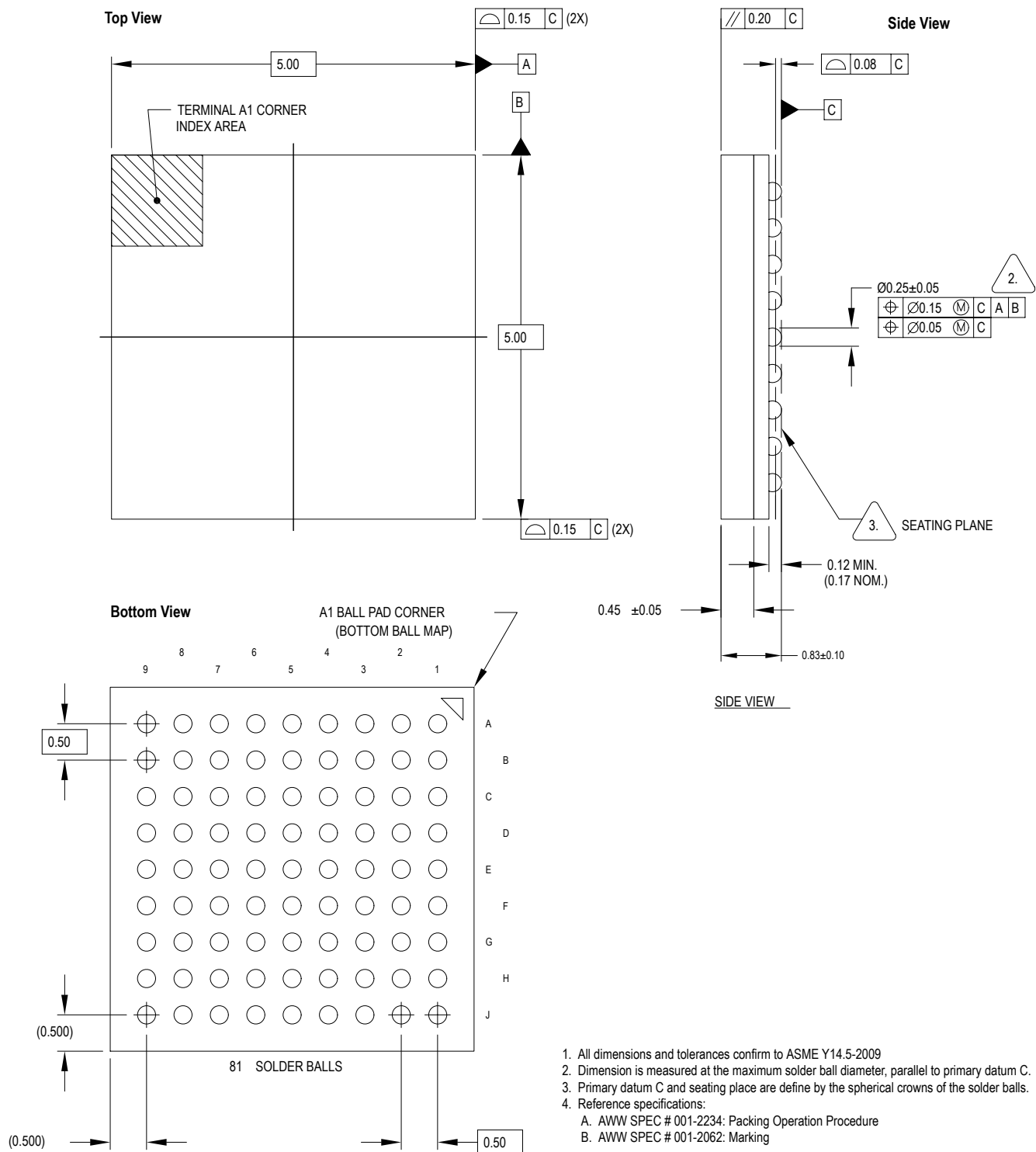


Figure 12: 81-Ball FBGA Package Outline



# 144-Lead LQFP Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package.

Figure 13: 144-Lead LQFP Pinout Diagram

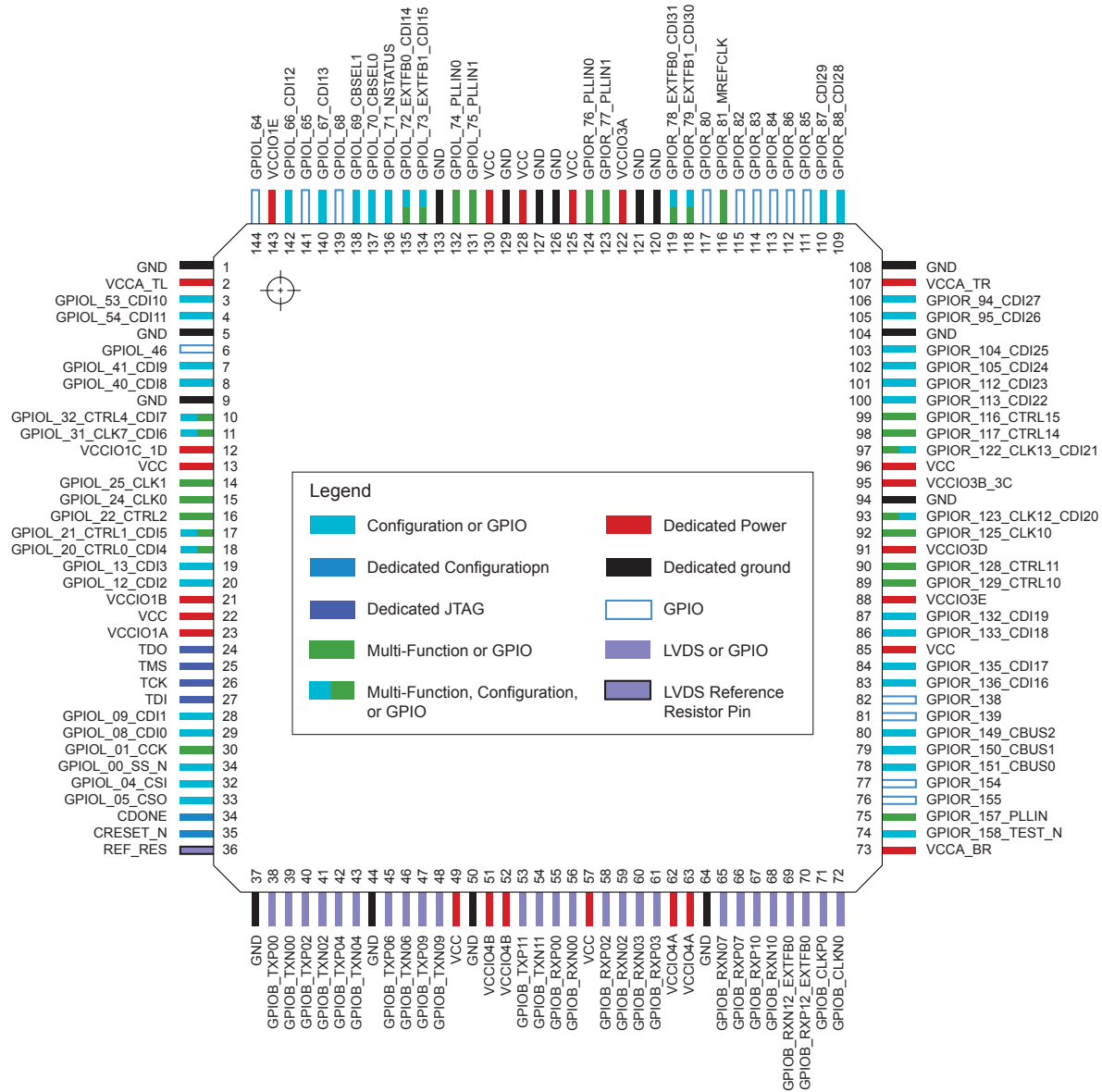


Figure 14: 144-Lead LQFP I/O Bank Diagram

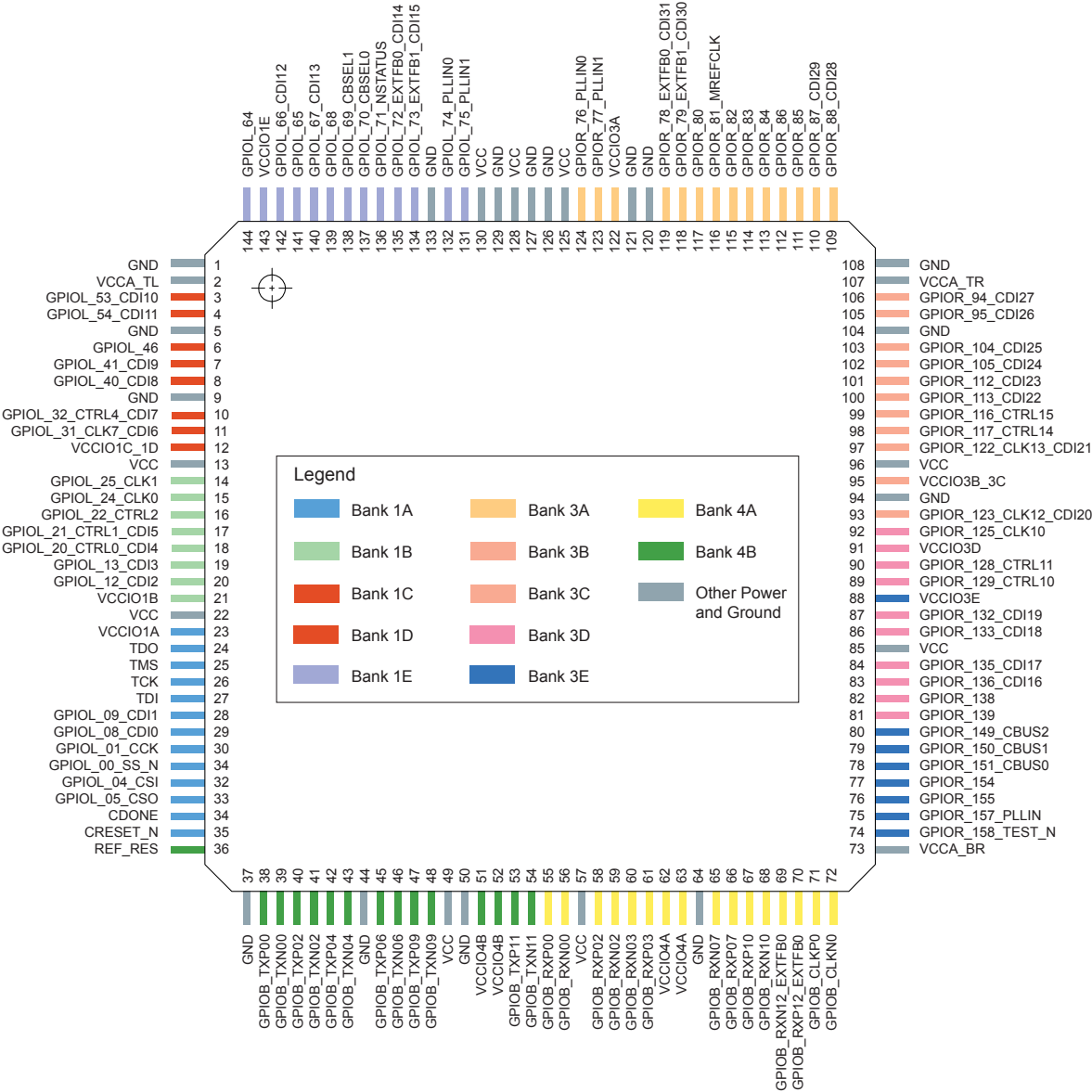
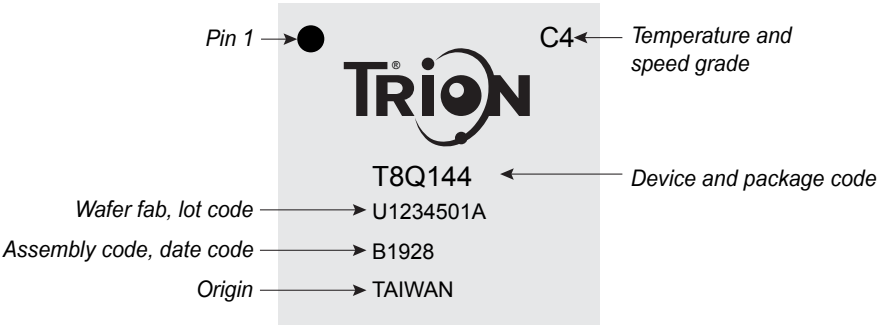
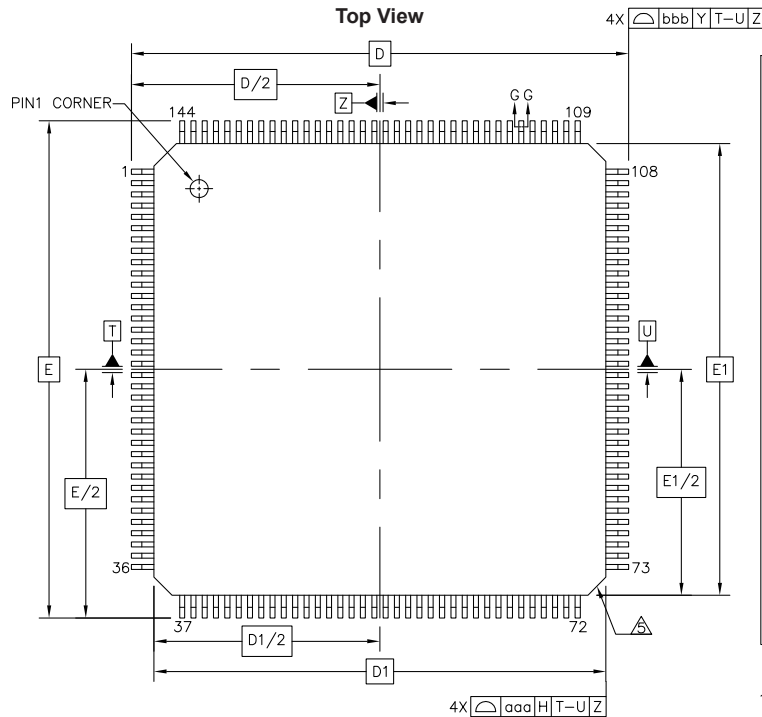


Figure 15: 144-Lead LQFP FPGA Package Marking



**Figure 16: 144-Lead LQFP FBGA Package Outline**

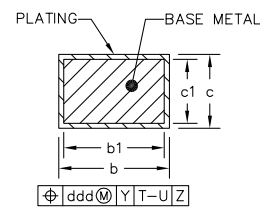
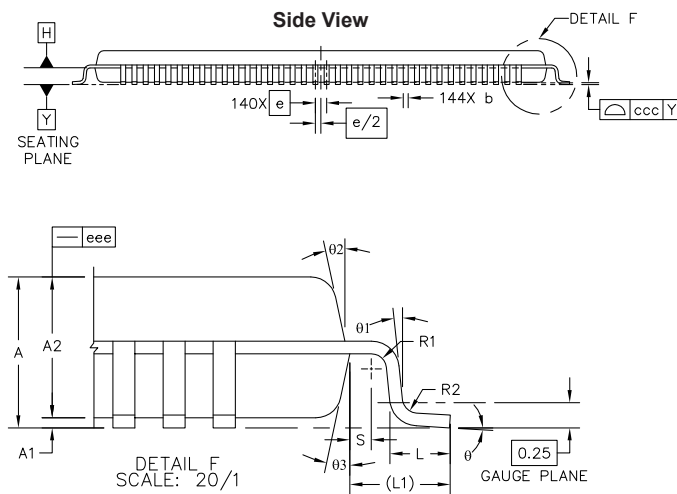


|                        |   | SYMBOL | MIN     | NOM  | MAX  |
|------------------------|---|--------|---------|------|------|
| TOTAL THICKNESS        |   | A      | ---     | ---  | 1.6  |
| STAND OFF              |   | A1     | 0.05    | ---  | 0.15 |
| MOLD THICKNESS         |   | A2     | 1.35    | 1.4  | 1.45 |
| LEAD WIDTH(PLATING)    |   | b      | 0.17    | 0.22 | 0.23 |
| LEAD WIDTH             |   | b1     | 0.17    | 0.2  | 0.23 |
| L/F THICKNESS(PLATING) |   | c      | 0.09    | ---  | 0.2  |
| L/F THICKNESS          |   | c1     | 0.09    | ---  | 0.16 |
| BODY SIZE              | X | D      | 22 BSC  |      |      |
|                        | Y | E      | 22 BSC  |      |      |
|                        | X | D1     | 20 BSC  |      |      |
|                        | Y | E1     | 20 BSC  |      |      |
| LEAD PITCH             |   | e      | 0.5 BSC |      |      |
|                        |   | L      | 0.45    | 0.6  | 0.75 |
| FOOTPRINT              |   | L1     | 1 REF   |      |      |
|                        |   | Ø      | 0*      | 3.5* | 7*   |
|                        |   | Ø1     | 0*      | ---  | ---  |
|                        |   | Ø2     | 11*     | 12*  | 13*  |
|                        |   | Ø3     | 11*     | 12*  | 13*  |
|                        |   | R1     | 0.08    | ---  | ---  |
|                        |   | R2     | 0.08    | ---  | 0.2  |
|                        |   | S      | 0.2     | ---  | ---  |
| PACKAGE EDGE TOLERANCE |   | aaa    | 0.1     |      |      |
| LEAD EDGE TOLERANCE    |   | bbb    | 0.2     |      |      |
| COPLANARITY            |   | ccc    | 0.08    |      |      |
| LEAD OFFSET            |   | ddd    | 0.08    |      |      |
| MOLD FLATNESS          |   | eee    | 0.05    |      |      |

## NOTES

1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLDDPROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUMb DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

5 EXACT SHAPE OF EACH CORNER IS OPTIONAL.

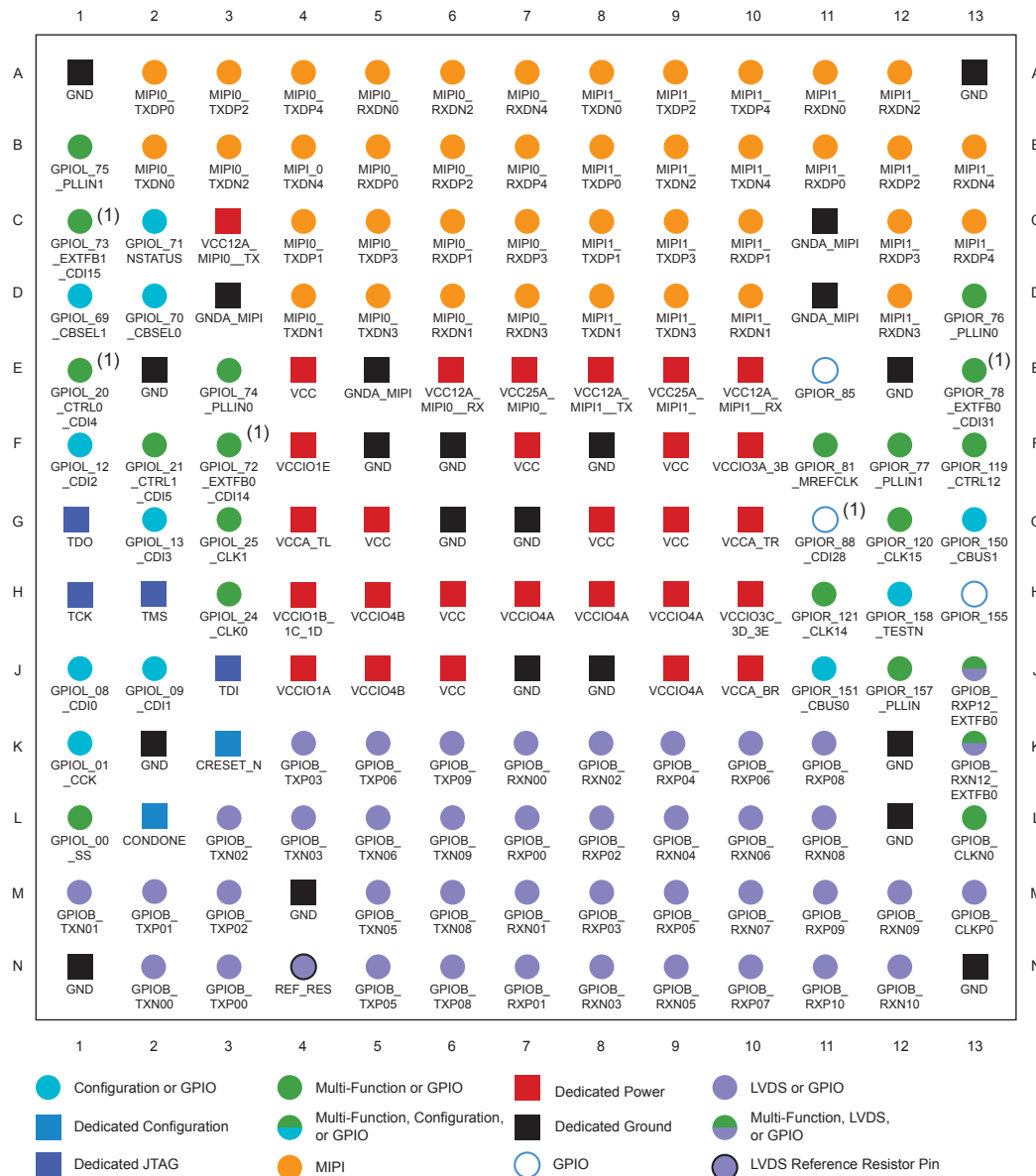


SECTION G-G  
SCALE: 100/1

# 169-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 17: 169-Ball FBGA Pinout Diagram



Note (1) In this package, this pin is not used for configuration functions.

Figure 18: 169-Ball FBGA I/O Bank Diagram

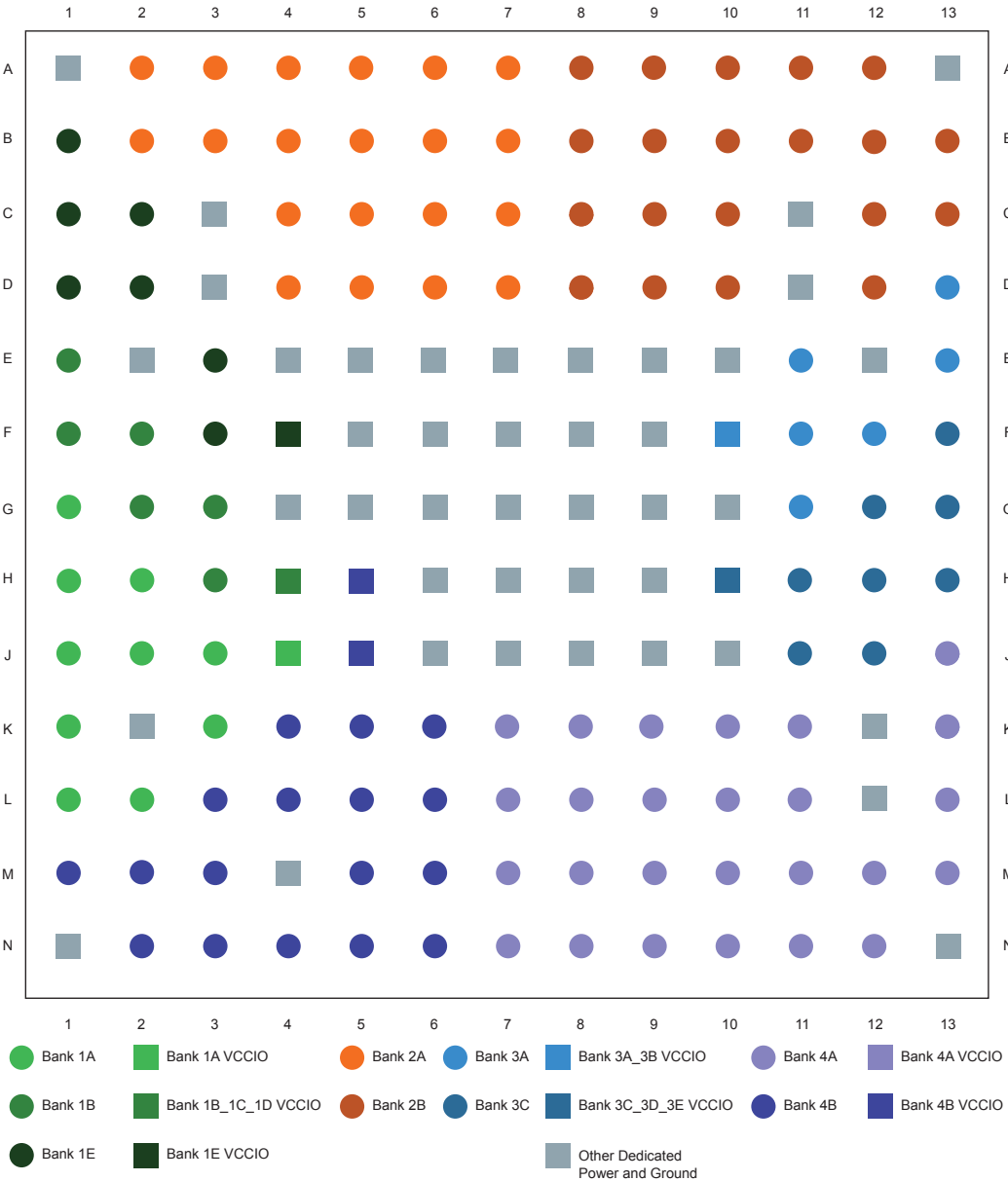


Figure 19: 169-Ball FPGA Package Marking

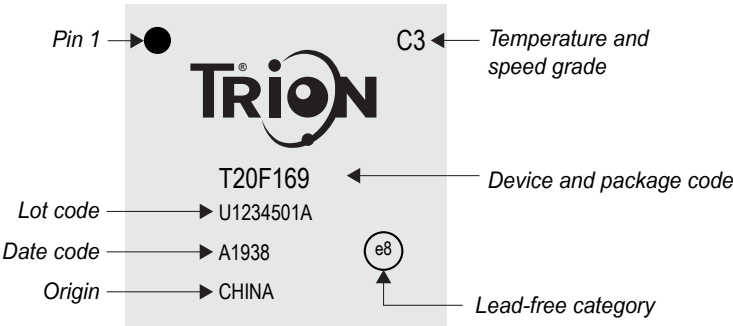
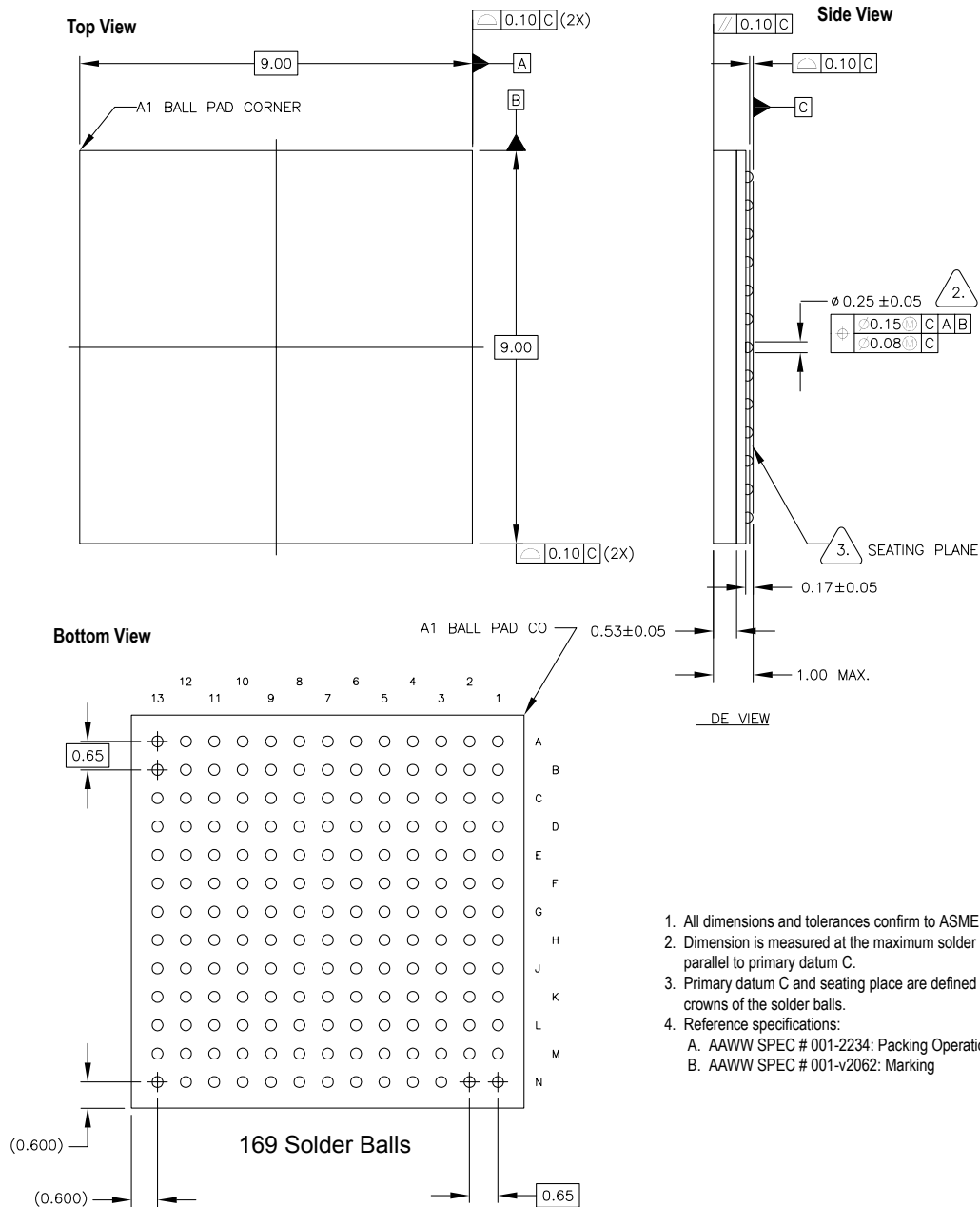


Figure 20: 169-Ball FBGA Package Outline



1. All dimensions and tolerances confirm to ASME Y14.5M-2009
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
3. Primary datum C and seating place are defined by the spherical crowns of the solder balls.
4. Reference specifications:
  - A. AAWW SPEC # 001-2234: Packing Operation Procedure
  - B. AAWW SPEC # 001-v2062: Marking



# 256-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 21: 256-Ball FBGA Pinout Diagram

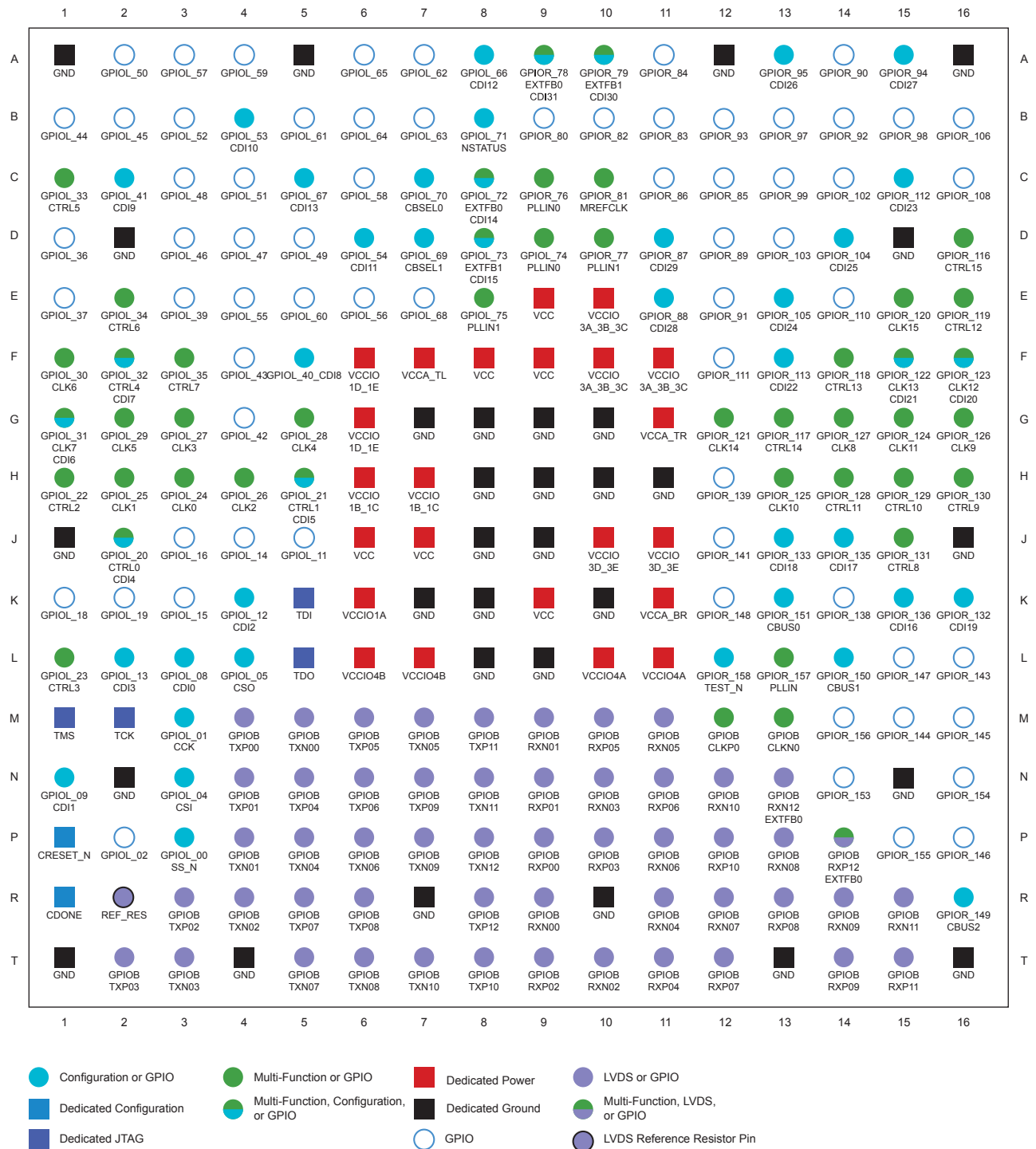


Figure 22: 256-Ball FBGA I/O Bank Diagram

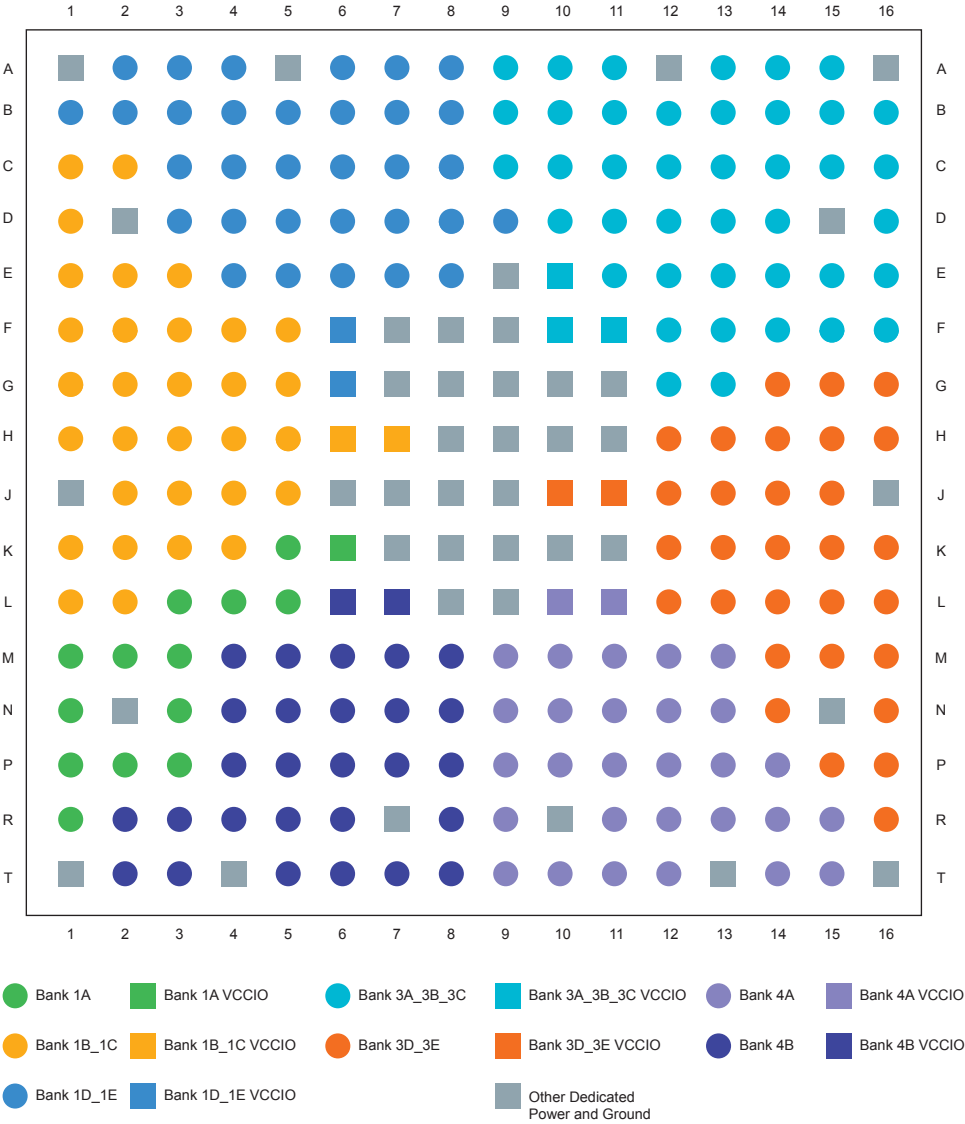


Figure 23: 256-Ball FPGA Package Marking

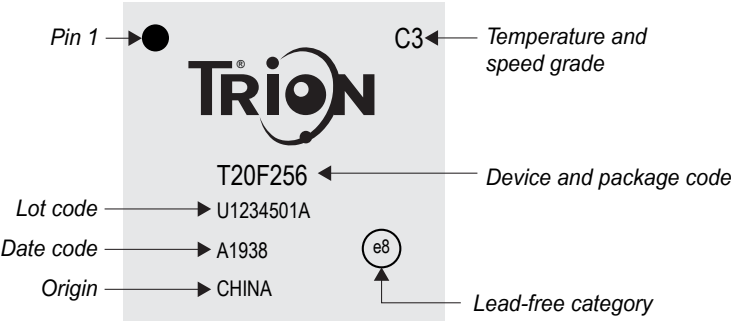
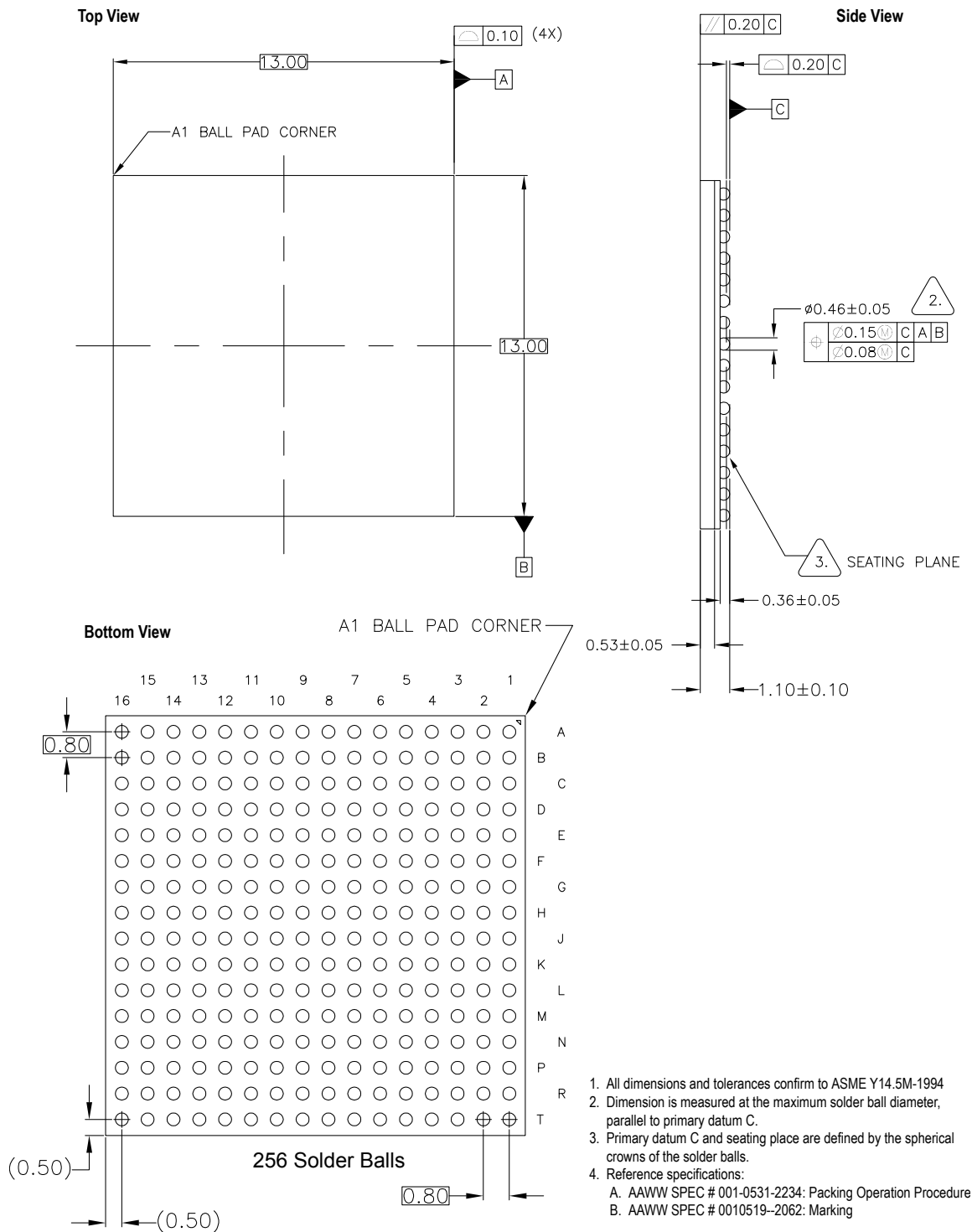


Figure 24: 256-Ball FBGA Package Outline



# 324-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package.



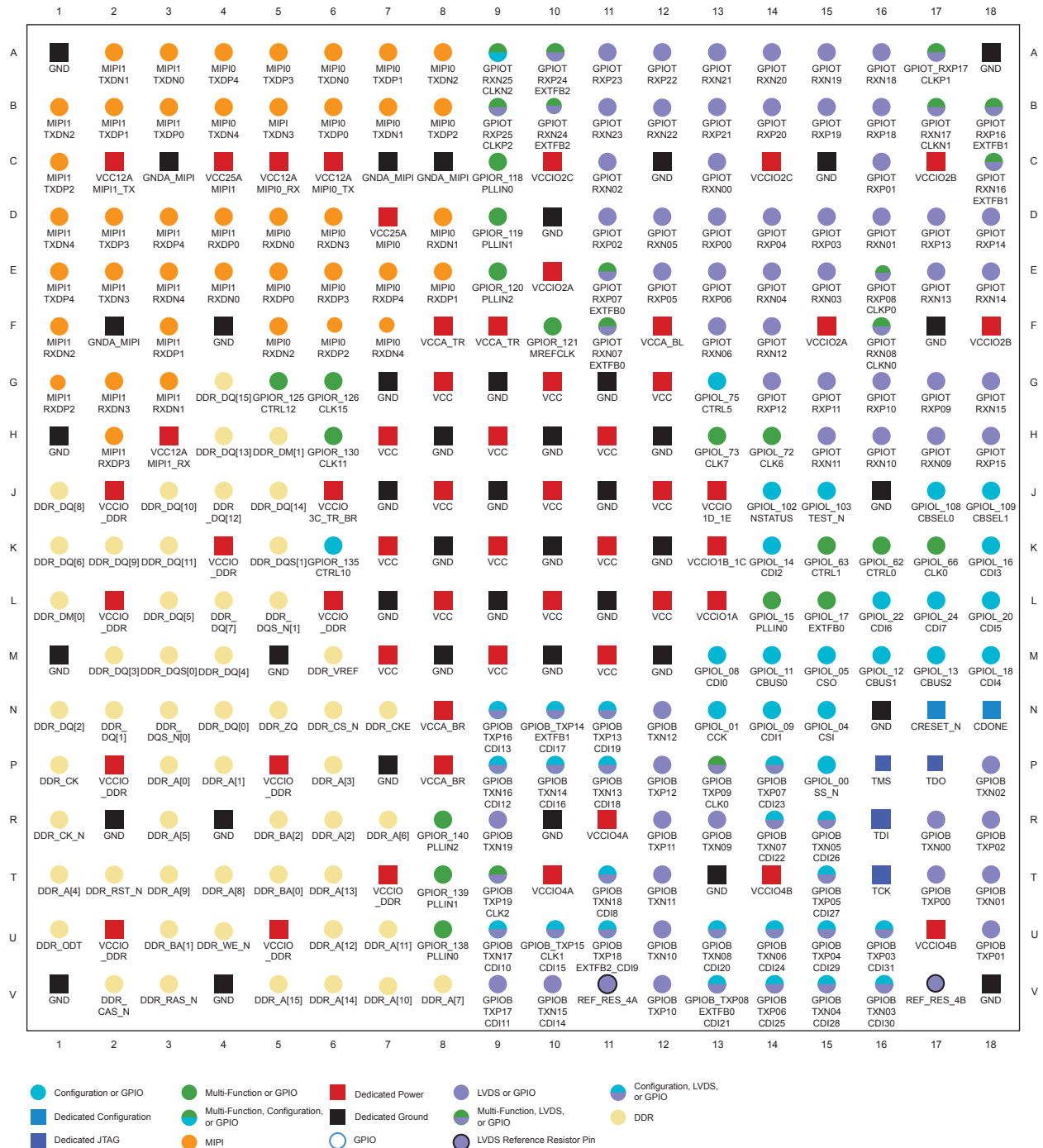
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**Note:** Some pin names and I/O banks differ between T20/T35 and T55/T85/T120 FPGAs; however, you can still migrate between FPGAs in this package.

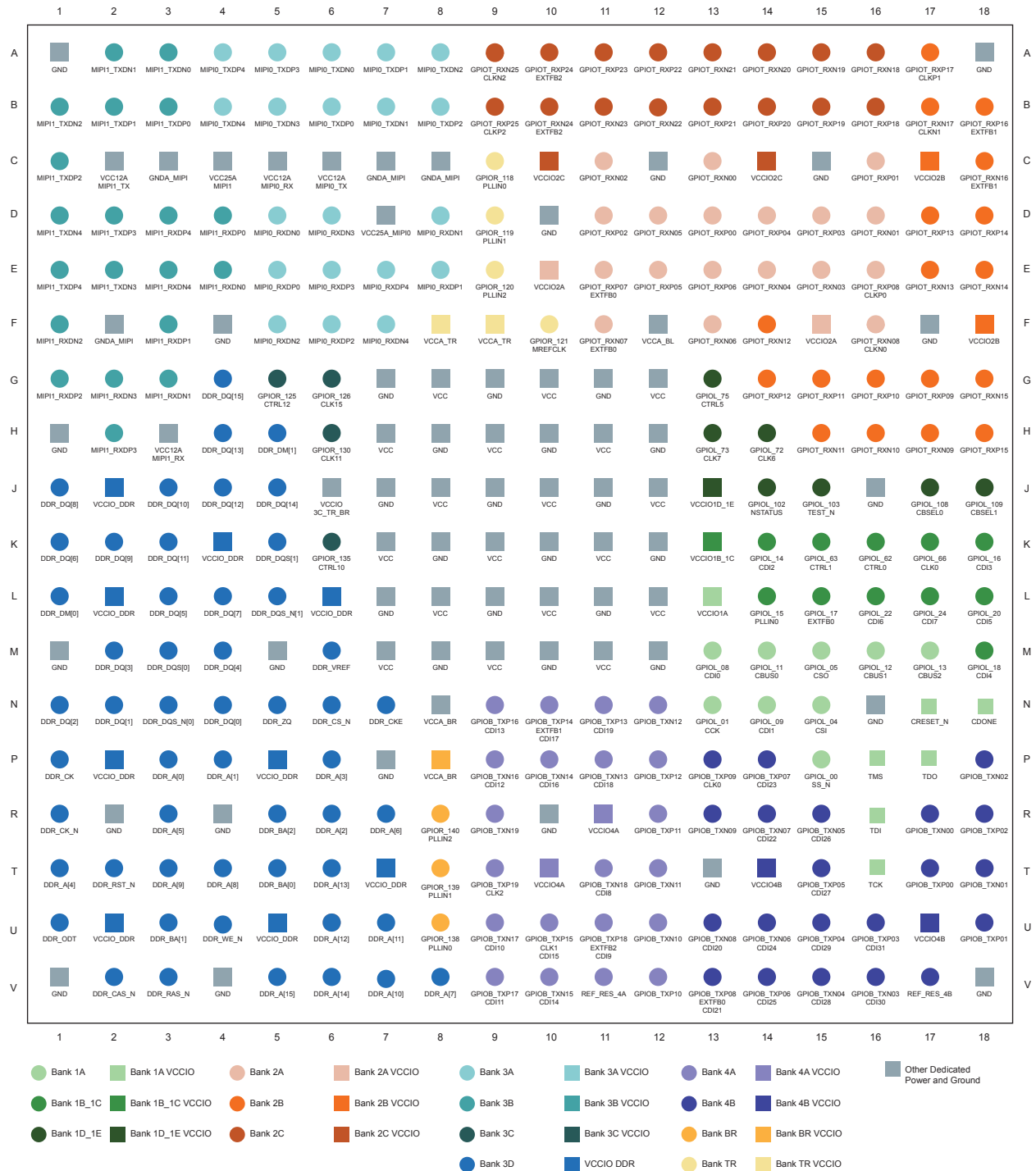
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## T20 and T35 FPGAs: Pinout and I/O Banks

Figure 25: 324-Ball FBGA Pinout Diagram (T20 and T35)



30



# T55, T85, and T120 FPGAs: Pinout and I/O Banks

Figure 27: 324-Ball FBGA Pinout Diagram (T55, T85, and T120)

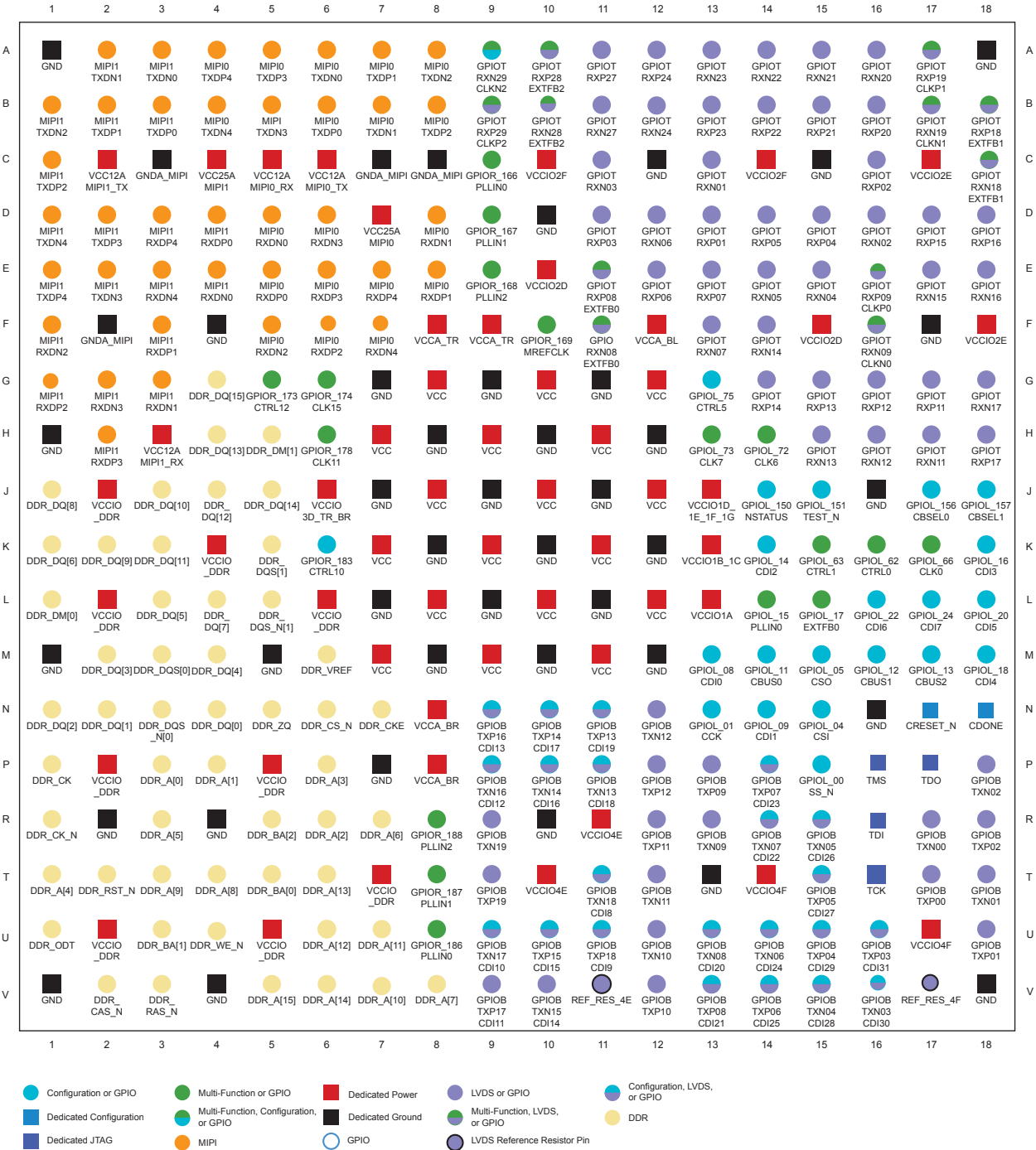
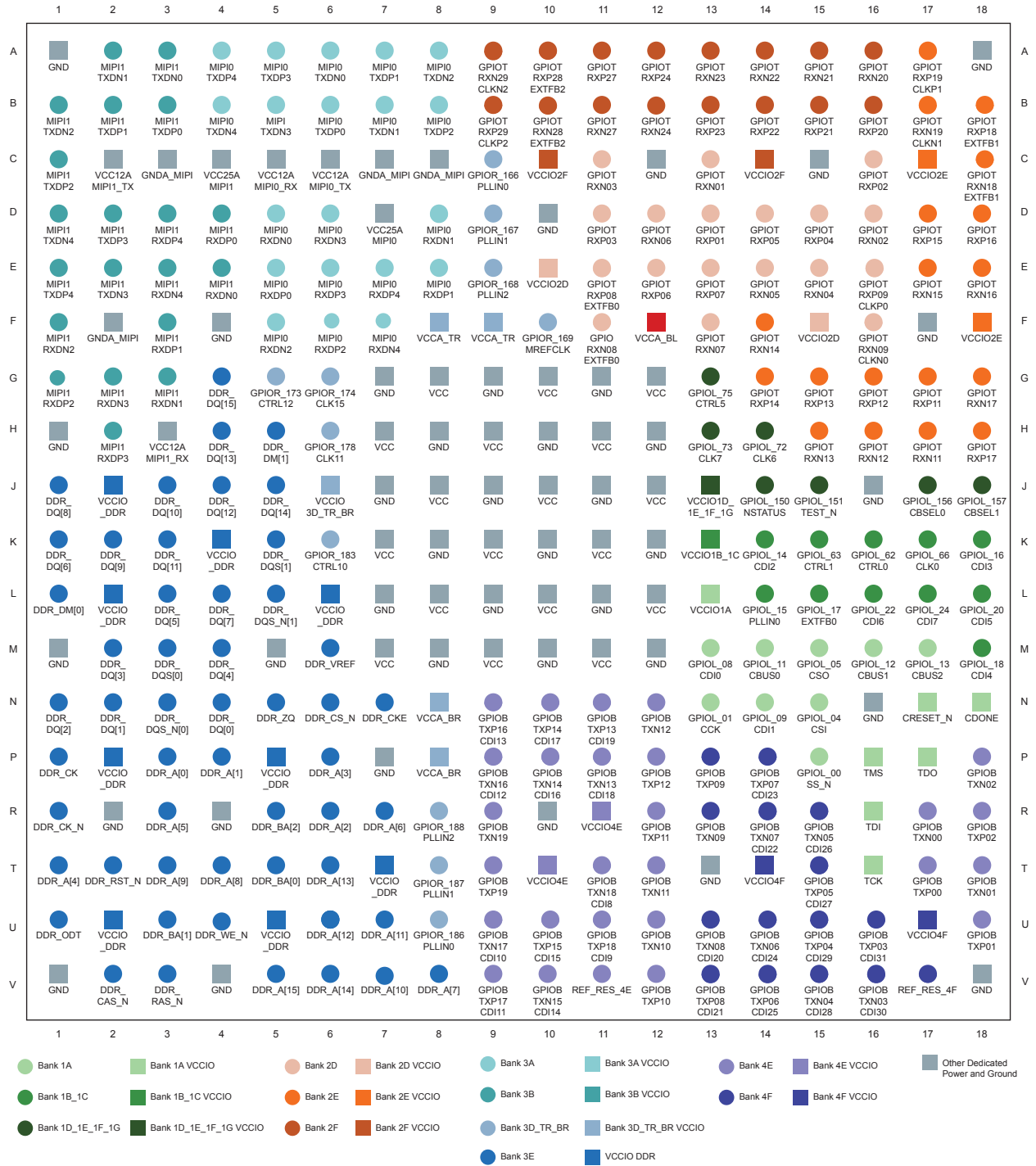


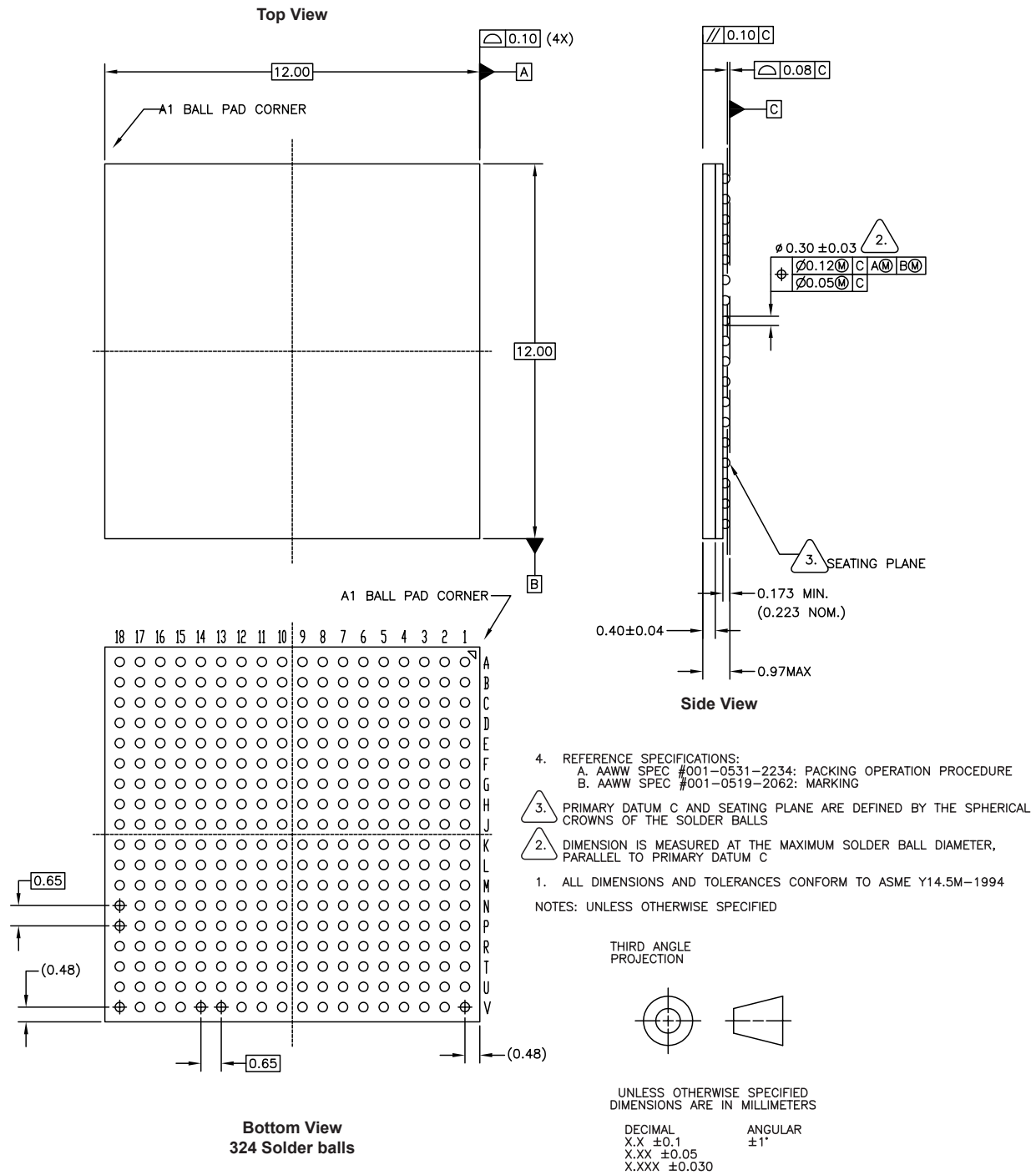
Figure 28: 324-Ball FBGA I/O Bank Diagram (T55, T85, and T120)



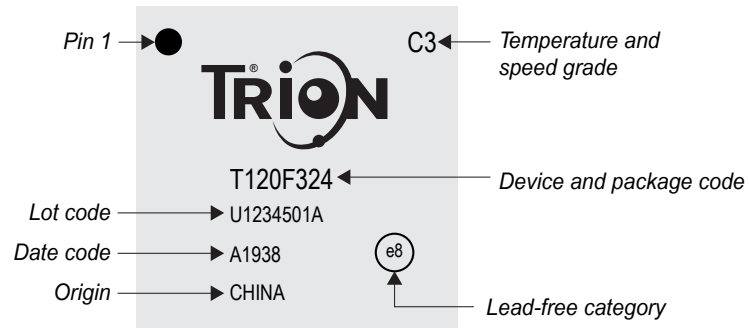


## Package Outline and Marking (All FPGAs in this Package)

Figure 29: 324-Ball FBGA Package Outline



**Figure 30: 324-Ball FPGA Package Marking**



# 400-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 31: 400-Ball FBGA Pinout Diagram

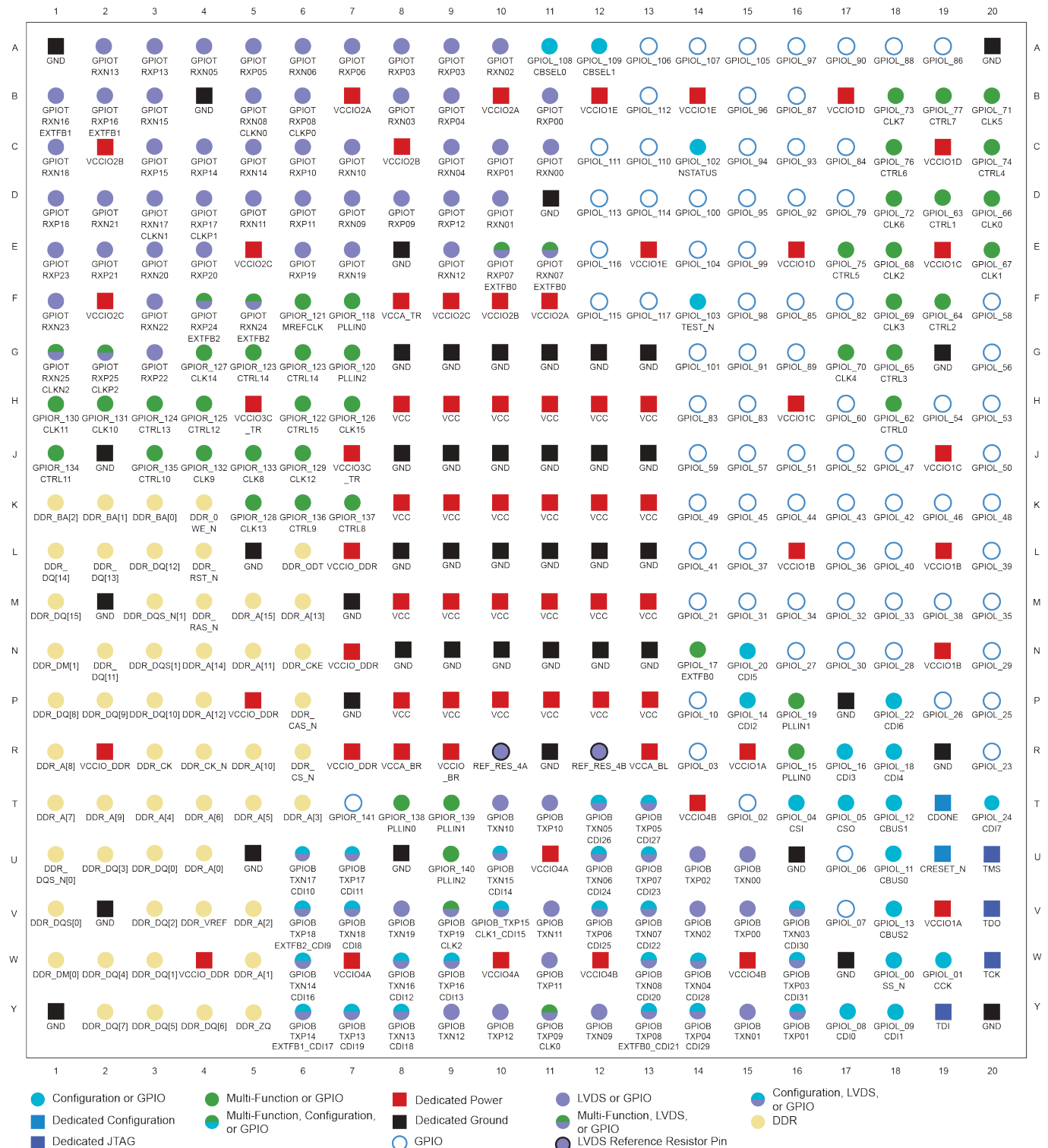


Figure 32: 400-Ball FBGA I/O Bank Diagram

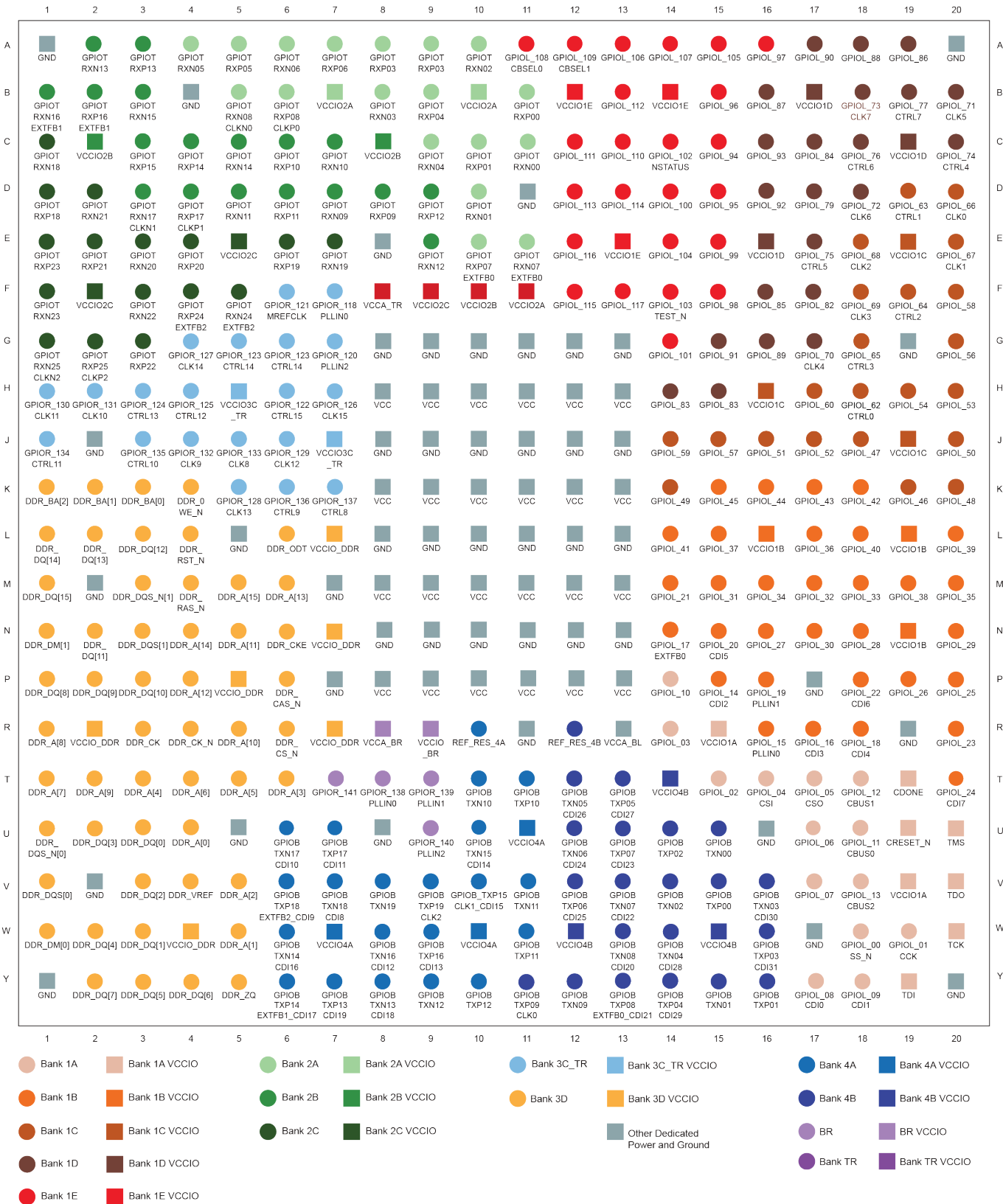


Figure 33: 400-Ball FBGA Package Outline

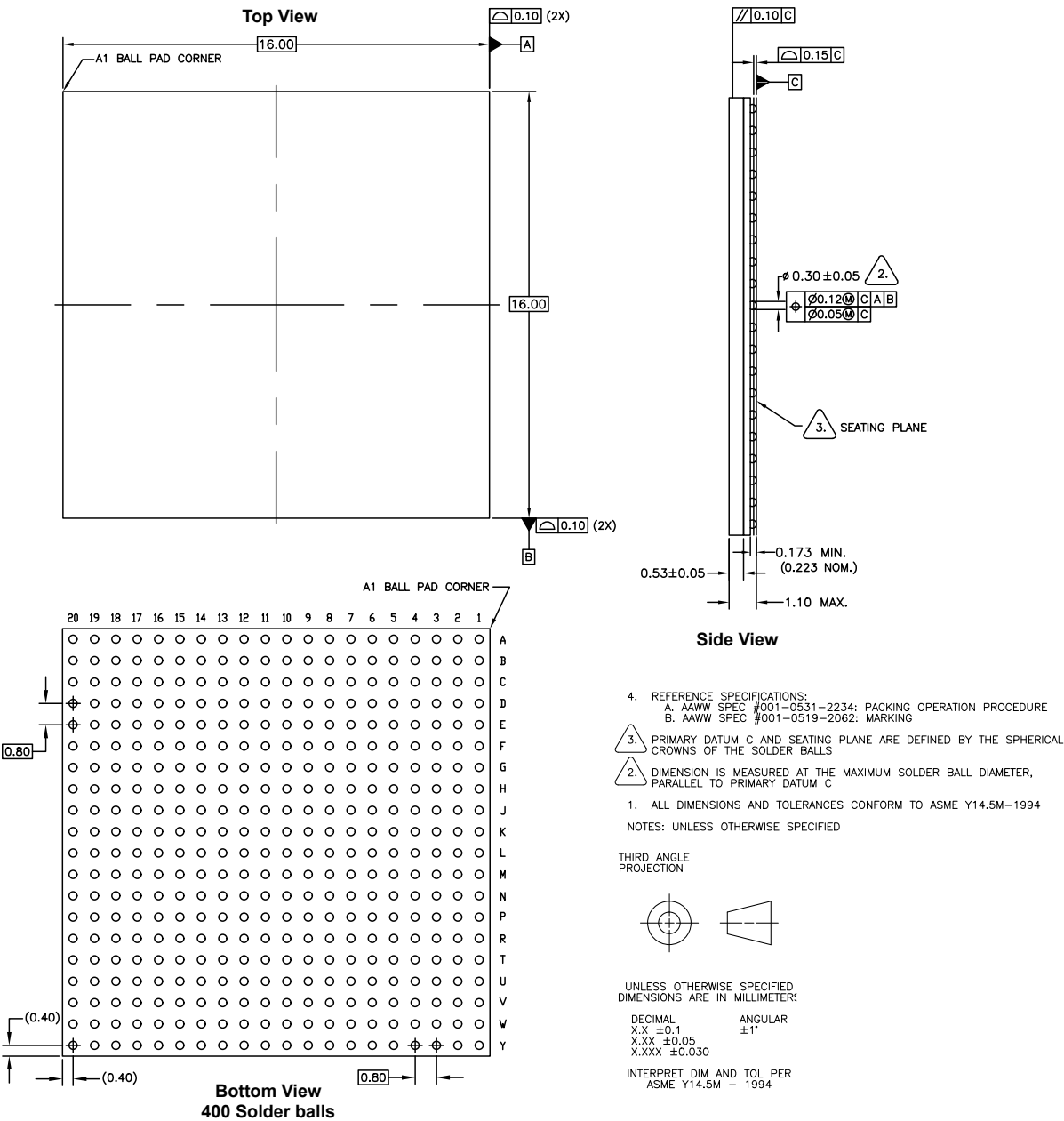
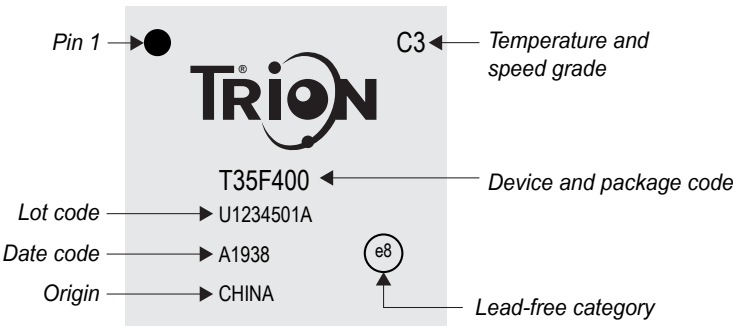


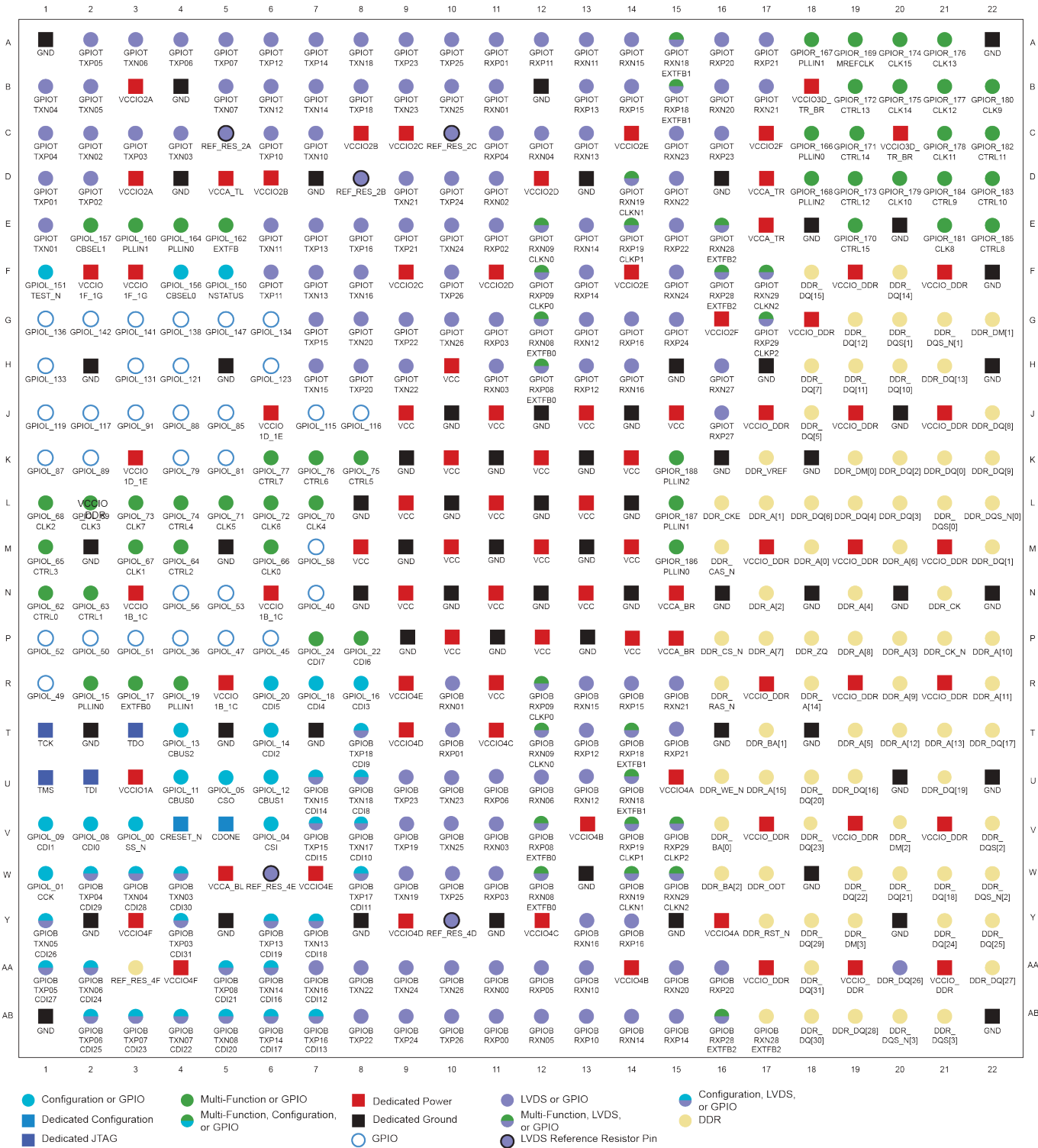
Figure 34: 400-Ball FPGA Package Marking



# 484-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 35: 484-Ball FBGA Pinout Diagram



**Figure 36: 484-Ball FBGA I/O Bank Diagram**

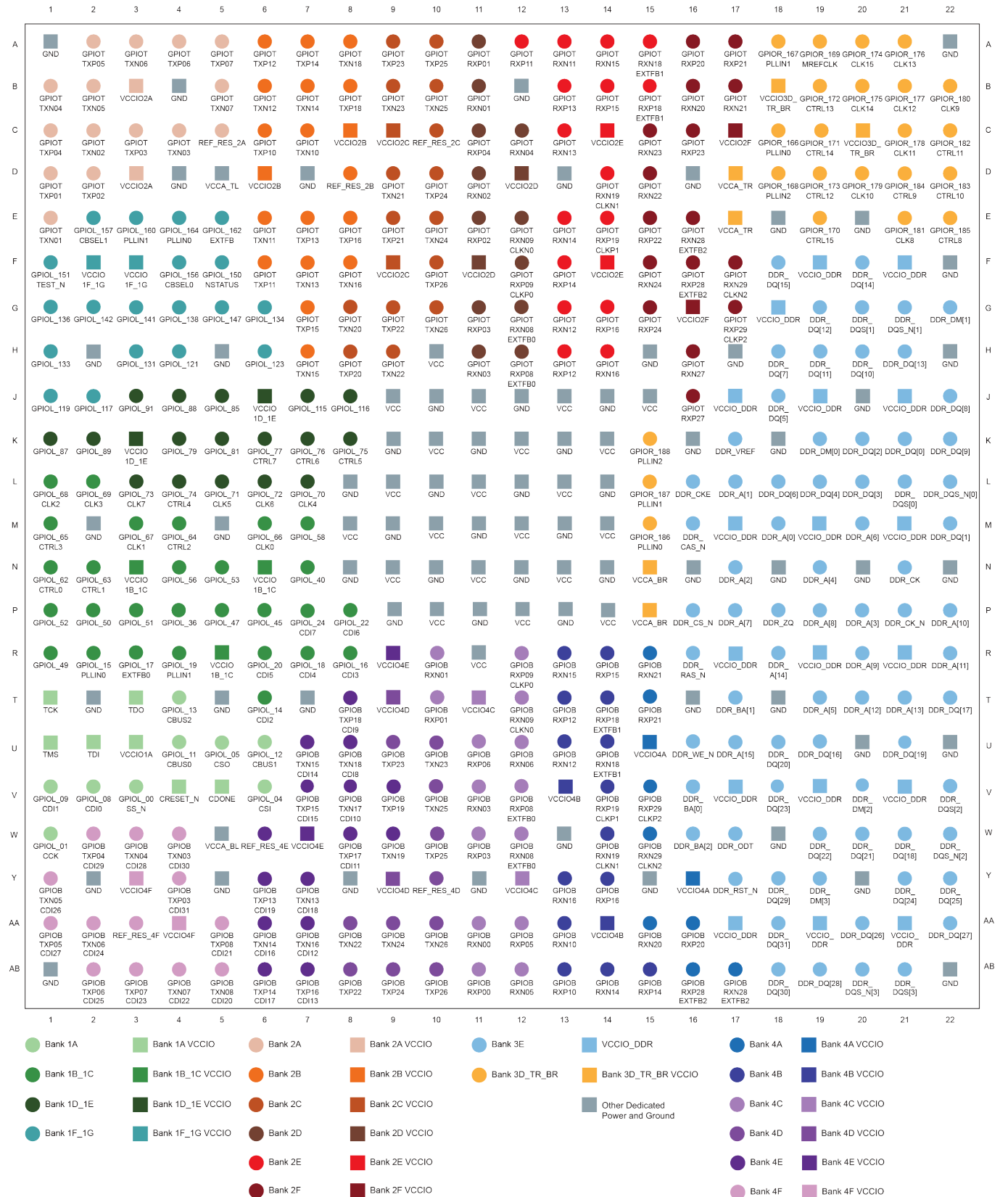
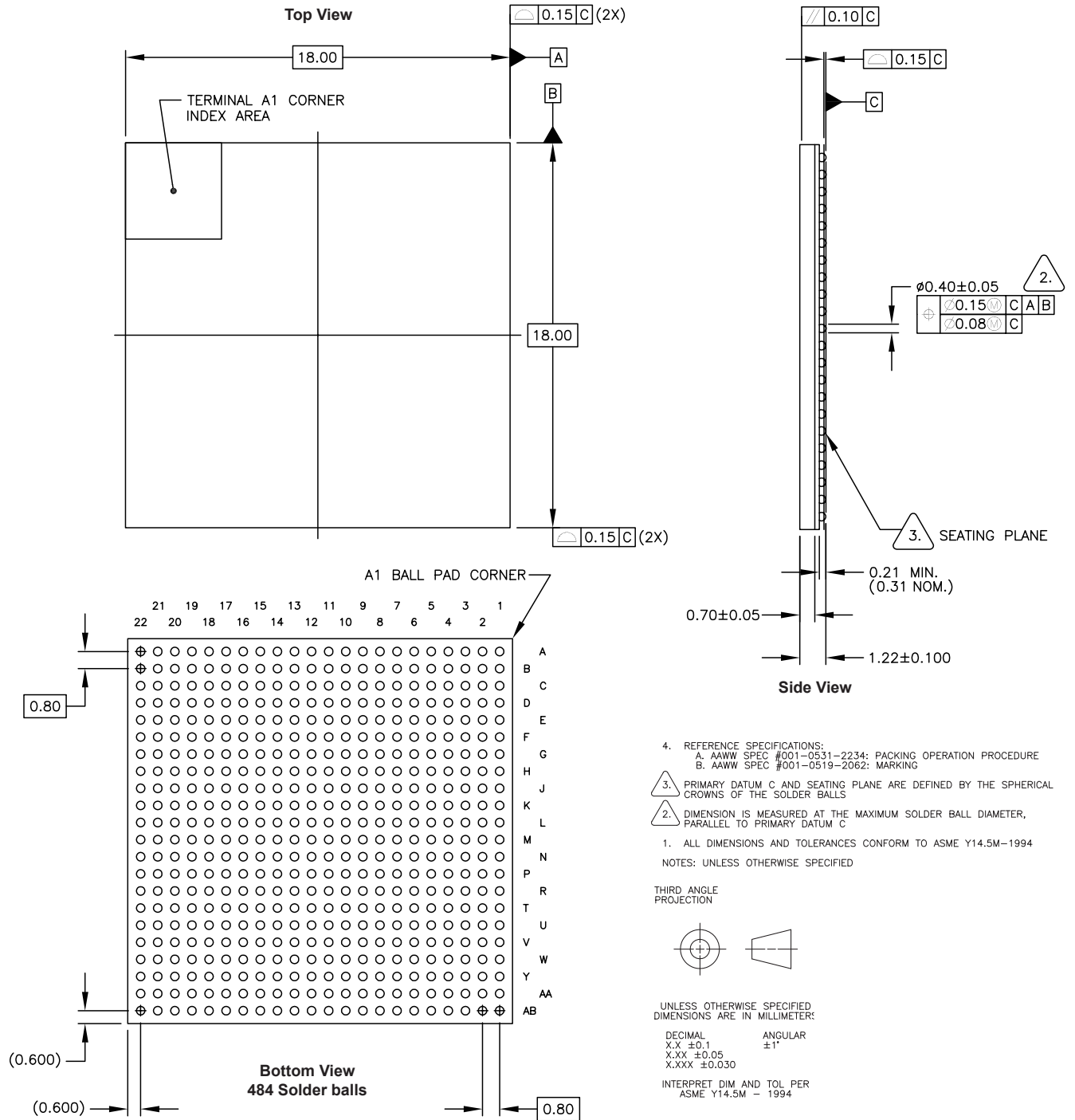


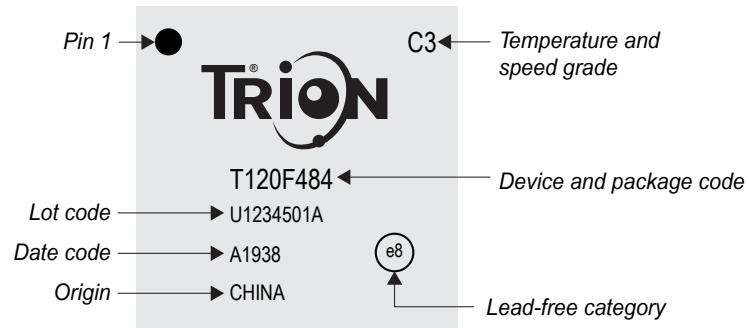


Figure 37: 484-Ball FBGA Package Outline





**Figure 38: 484-Ball FPGA Package Marking**



**Figure 39: 576-Ball FBGA Pinout Diagram**



Figure 40: 576-Ball FBGA I/O Bank Diagram

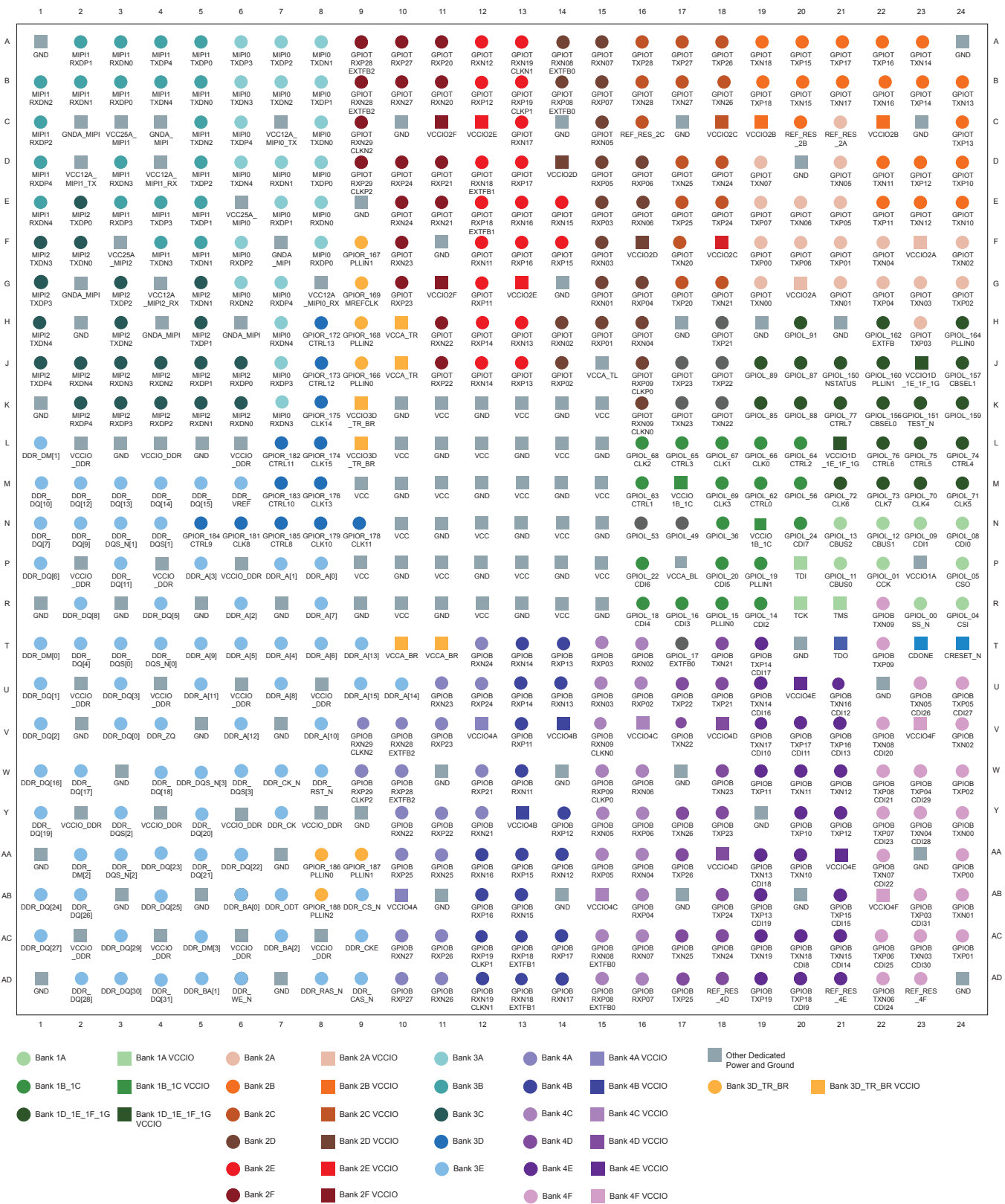


Figure 41: 576-Ball FBGA Package Outline

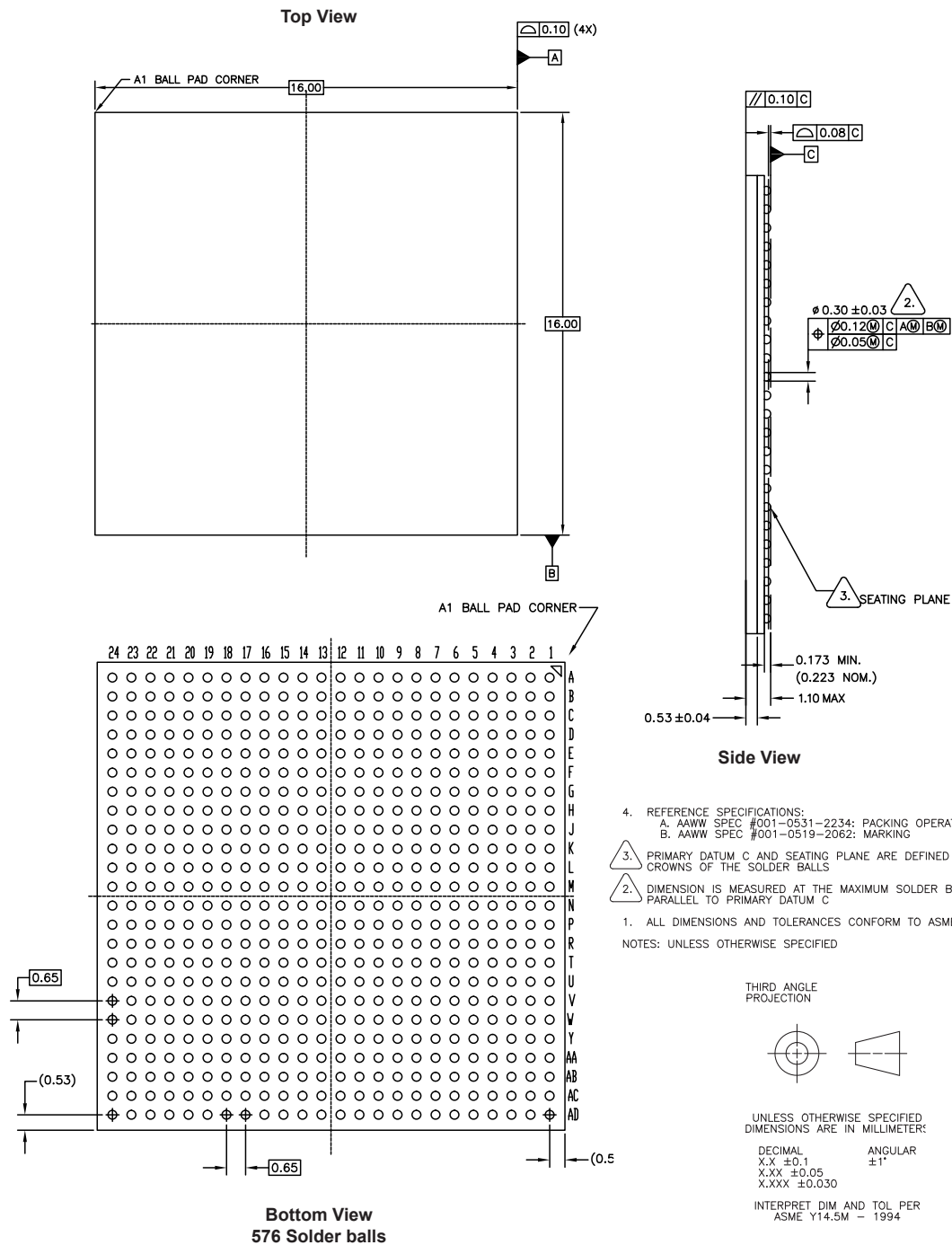
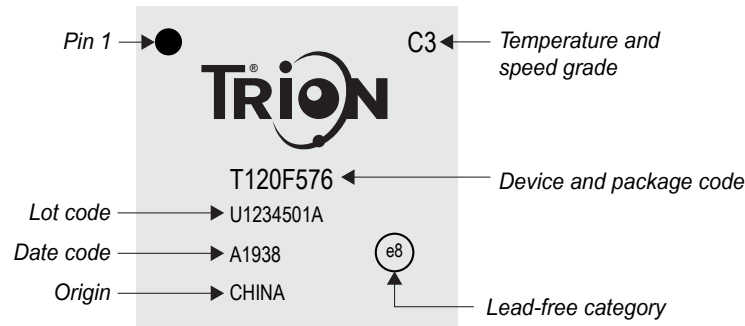


Figure 42: 576-Ball FPGA Package Marking



## Solder Reflow Guidelines for Surface-Mount Devices

This section provides general guidelines for solder reflow process for 易灵思® surface-mount FPGAs. The data used in this document is based on IPC/JEDEC (Association Connecting Electronics Industries/JEDEC Solid State Technology Association) standards. Each printed circuit board (PCB) has its own profile, which depends upon the reflow equipment used and the board design. You must characterize each PCB to find the profile that is reliable.

### Reflow

During solder reflow, follow these guidelines:

- Use caution when profiling to ensure that the maximum temperature difference between components is less than 10 °C.
- For best results, perform forced convection reflow with nitrogen.

### Inspection

Follow these inspection guidelines:

- **Pre-reflow**—Use visual inspection to verify solder paste dispense location and quantity.
- **Pick and place**—Use machine vision as necessary to ensure proper component placement.
- **Post reflow**—Use electrical testing to verify solder joint formation.

### BGA Reballing

易灵思® does not recommend BGA reballing. Reballled BGA packages void the original 易灵思® specifications.

## Peak Reflow Temperatures

*Table 7: Peak Reflow Temperature (Tp) by Package*

| Package | Number of Leads/Balls | Moisture Sensitivity Level | Peak Reflow Temperature (+0/-5 °C) |
|---------|-----------------------|----------------------------|------------------------------------|
| FBGA    | 49                    | 3                          | 260                                |
| WLCSP   | 80                    | 1                          | 260                                |
| FBGA    | 81                    | 3                          | 260                                |
| FBGA    | 169                   | 3                          | 260                                |
| FBGA    | 256                   | 3                          | 260                                |
| FBGA    | 324                   | 3                          | 260                                |
| FBGA    | 400                   | 3                          | 260                                |
| FBGA    | 484                   | 3                          | 260                                |
| FBGA    | 576                   | 3                          | 260                                |
| LQFP    | 144                   | 3                          | 260                                |



**Note:** These packages are "green" and RoHS compliant.

## Reflow Profile for SMT Packages

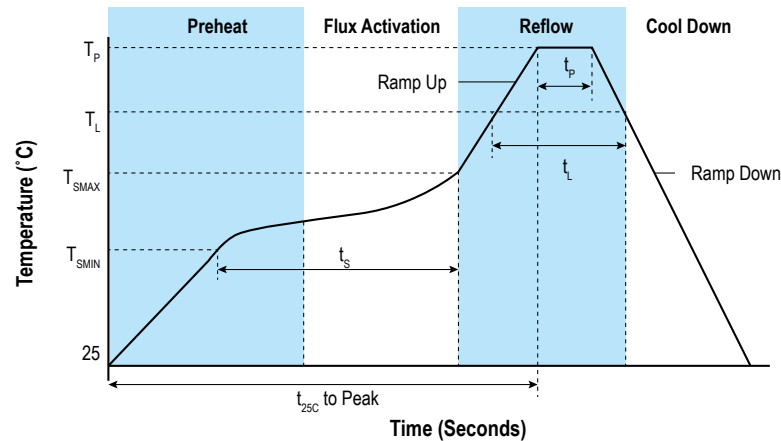
The reflow process usually includes four phases:

1. **Preheat Phase**—The preheat phase brings the assembly from 25 °C to  $T_S$ . During this phase, the solvent evaporates from the solder paste. The preheat temperature ramp rate should be less than 2 °C/second to avoid solder balling defects such as solder ball spattering and bridging.
  - **Solder Ball Spattering**—Spattering, the most common solder balling defect, is caused by solvents evaporating explosively. To eliminate spattering, use a slower temperature rise in the preheat phase.
  - **Bridging**—Bridging is usually caused by inaccurate or splashy screen printing, and can often occur with fine pitch components. It can also be caused by solder paste slumping during a rapid temperature rise in the preheat phase.
2. **Flux Activation Phase**—As the temperature rises slowly, it reaches a point at which the flux completely wets the surfaces to be soldered.
3. **Reflow Phase**—The temperature rises to a level sufficient to reflow the solder. The flux wicks surface oxides and contaminants away from the melted solder, resulting in a clean solder joint.
4. **Cool Down Phase**—Ramp down the temperature as fast as possible to control grain size; however, do not exceed 6 °C/second.

*Table 8: Peak Reflow Temperature ( $T_P$ ) Parameters*

| Parameter                 | Description                                     | Specification (Lead and Halogen Free Packages) |
|---------------------------|-------------------------------------------------|------------------------------------------------|
| Ramp up                   | Average ramp-up rate ( $T_{S_{MAX}}$ to $T_P$ ) | 3 °C/second maximum                            |
| $T_{S_{MIN}}$             | Preheat peak minimum temperature                | 150 °C                                         |
| $T_{S_{MAX}}$             | Preheat peak maximum temperature                | 200 °C                                         |
| $t_s$                     | Time between $T_{S_{MIN}}$ and $T_{S_{MAX}}$    | 60 - 120 seconds                               |
| $T_L$                     | Solder melting point                            | 217 °C                                         |
| $t_L$                     | Time maintained above $T_L$                     | 60 - 150 seconds                               |
| $t_p$                     | Time within 5 °C of peak temperature            | 30 seconds                                     |
| Ramp down                 | Ramp-down rate                                  | 6 °C/second maximum                            |
| $t_{25C \text{ to } T_P}$ | Time from 25 °C to peak temperature             | 8 minutes maximum                              |

Figure 43: Thermal Reflow Profile



## Thermal Resistance

Thermal management is an important consideration when designing your system. 易灵思® device data sheets describe the maximum allowable junction temperature so you can assess your system's thermal characteristics. To ensure that the device and package do not exceed the junction temperature requirements, you should always complete a thermal analysis of your specific design.

The data shown in this section is relative and actual values depend on a variety of factors such as die size, paddle size, airflow, power applied, printed circuit board design, proximity of other devices, and user applications. Because of this, 易灵思 FPGAs do not come with preset thermal solutions.

Table 9: Device/Package Thermal Resistance

| Device         | Package | Dimensions (mm) | $\Theta_{JA}/W$<br>Still Air | $\Theta_{JA}$<br>(200 LFM)/W | $\Theta_{JA}$<br>(500 LFM)/W | $\Theta_{JB}/W$ | $\Theta_{JC}/W$ |
|----------------|---------|-----------------|------------------------------|------------------------------|------------------------------|-----------------|-----------------|
| T4, T8         | FBGA49  | 3 x 3           | 90.446                       | 84.782                       | 81.797                       | 56.464          | 46.431          |
|                | FBGA81  | 5 x 5           | 80.476                       | 75.363                       | 72.797                       | 55.352          | 32.583          |
| T8, T20        | LQFP144 | 20 x 20         | 42.82                        | 37.68                        | 35.50                        | 31.12           | 10.51           |
| T13, T20       | FBGA169 | 9 x 9           | 38.25                        | 33.33                        | 31.60                        | 23.64           | 12.39           |
|                | FBGA256 | 13 x 13         | 24.24                        | 20.52                        | 17.59                        | 31.57           | 11.85           |
| T20            | WLCSP80 | 4.5 x 3.5       | 44.94                        | 39.35                        | 37.54                        | 18.91           | 0.12            |
| T20, T35       | FBGA324 | 12 x 12         | 20.69                        | 17.89                        | 16.89                        | 10.12           | 2.59            |
|                | FBGA400 | 16 x 16         | 18.70                        | 16.95                        | 15.92                        | 12.45           | 11.10           |
| T55, T85, T120 | FBGA324 | 12 x 12         | 16.9                         | 14.4                         | 13.5                         | 8.04            | 2.01            |
|                | FBGA484 | 18 x 18         | 15.85                        | 12.83                        | 11.99                        | 6.10            | 4.10            |
|                | FBGA576 | 16 x 16         | 15.376                       | 13.648                       | 12.568                       | 6.601           | 1.712           |

Where:

- $\Theta_{JA}$  is the junction-to-ambient thermal resistance

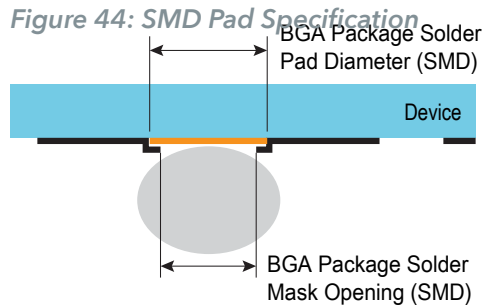


- $\Theta_{JB}$  is the junction-to-board thermal resistance
- $\Theta_{JC}$  is the junction-to-case thermal resistance

## PCB Guidelines for BGA Packages

### Solder Mask Defined Guidelines

易灵思 provides solder mask defined (SMD) diameter information. Use this data when creating your board layout so that the board pads match the landing pads.



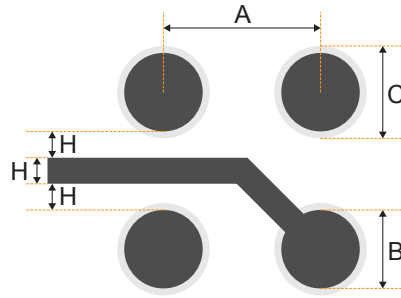
**Table 10: PCB Solder Pad Recommendations**

| Package                  | Pitch (mm) | BGA Package Solder Mask Opening (mm) | Optimum PCB (SMD) Opening (mm) |
|--------------------------|------------|--------------------------------------|--------------------------------|
| FBGA49                   | 0.40       | 0.275                                | 0.200                          |
| WLCSP80                  | 0.4        | N/A                                  | 0.2                            |
| FBGA81                   | 0.50       | 0.325                                | 0.245                          |
| FBGA169                  | 0.65       | 0.350                                | 0.250                          |
| FBGA256                  | 0.80       | 0.500                                | 0.370                          |
| FBGA324 (T20, T35)       | 0.65       | 0.335                                | 0.275                          |
| FBGA324 (T55, T85, T120) | 0.65       | 0.380                                | 0.275                          |
| FBGA400                  | 0.80       | 0.380                                | 0.275                          |
| FBGA484                  | 0.80       | 0.450                                | 0.350                          |
| FBGA576                  | 0.65       | 0.380                                | 0.275                          |

## Non-Solder-Mask Defined Guidelines

Non-solder-mask defined (NSMD) pad designs perform better than solder mask defined pads due to lower stresses in the solder near the top of pad. Additionally, they provide a better “grip” area around the pad edge. For best reliability, the Generic Requirements for Surface Mount Design and Land Pattern Standard (IPC-7351A) recommends a NSMD pad with a diameter that is slightly smaller than the solder ball. This size allows you to use a trace between pads while meeting clearance requirements.

*Figure 45: Routing Traces between Pads on the Top Layer*



*Table 11: Routing Measurements*

| Measurement | Description                                          | Ball Count |      |      |      |               |      |      | Unit |
|-------------|------------------------------------------------------|------------|------|------|------|---------------|------|------|------|
|             |                                                      | F49        | F81  | W80  | F169 | F324,<br>F576 | F484 | F256 |      |
| A           | Ball pitch.                                          | 0.4        | 0.5  | 0.4  | 0.65 | 0.65          | 0.8  | 0.8  | mm   |
|             | Ball $\phi$ .                                        | 0.25       | 0.25 | 0.25 | 0.25 | 0.3           | 0.4  | 0.46 | mm   |
| B           | Width of the solder landing pad $\phi$ .             | 0.25       | 0.25 | 0.25 | 0.25 | 0.3           | 0.4  | 0.46 | mm   |
| C           | Width of the solder mask opening $\phi$ .            | 0.35       | 0.35 | 0.35 | 0.35 | 0.4           | 0.5  | 0.56 | mm   |
| H (min.)    | Minimum space between the trace and the landing pad. | (2)        | 0.08 | (2)  | 0.1  | 0.1           | 0.1  | 0.1  | mm   |

<sup>(2)</sup> The via is under the pad, no traces between landing pads.

# Guidelines for Vias

You use vias to drop routing down to lower layers. This type of via, called an “offset via,” is very robust. The solder mask completely covers the via, which prevents short circuits during paste application, allows for paste overprinting, and prevents etch entrapment.

PCB fabricators use a laser drill for these size vias. Confirm that your fabricator can maintain the tight tolerances required to ensure adequate clearances between vias and pads.

Figure 46: Via Dimensions

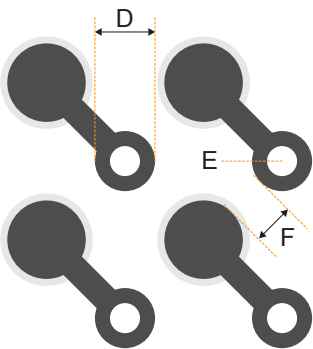


Table 12: Via Measurements

| Measurement | Description                            | Ball Count           |                      |                |       |               |      |      | Unit |
|-------------|----------------------------------------|----------------------|----------------------|----------------|-------|---------------|------|------|------|
|             |                                        | F49                  | F81                  | W80            | F169  | F324,<br>F576 | F484 | F256 |      |
| D           | Via capture pad width.                 | 0.25                 | 0.25                 | 0.25           | 0.4   | 0.4           | 0.5  | 0.5  | mm   |
| E           | Finished via $\phi$ .                  | 0.127 <sup>(3)</sup> | 0.127 <sup>(3)</sup> | 0.127          | 0.2   | 0.2           | 0.25 | 0.25 | mm   |
| F (min.)    | Space between the landing pad and via. | <sup>(4)</sup>       | 0.072                | <sup>(4)</sup> | 0.122 | 0.122         | 0.15 | 0.15 | mm   |

<sup>(3)</sup> Laser via.

<sup>(4)</sup> The via is under the pad, no traces between landing pads.

## Routing Guidelines

You can route a trace between two solder pads, which allows you to route the outer two rows of solder pads on the top layer. If you use all of the top-layer routing tracks to route the first and second rows, the inner rows of solder pads must connect to another routing layer with vias for routing outside of the BGA area.

You can use this method to route all of the inner solder pads. Because there is only enough space to route one trace between vias, you need an additional routing layer for every inner row of solder pads after the fourth row.

Figure 47: BGA Trace Routing for Top and Second Layers

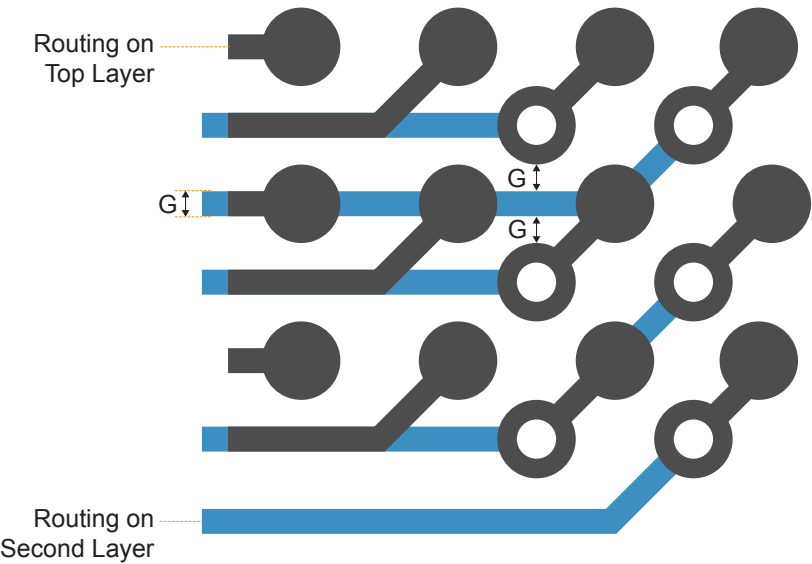


Table 13: Routing Measurements

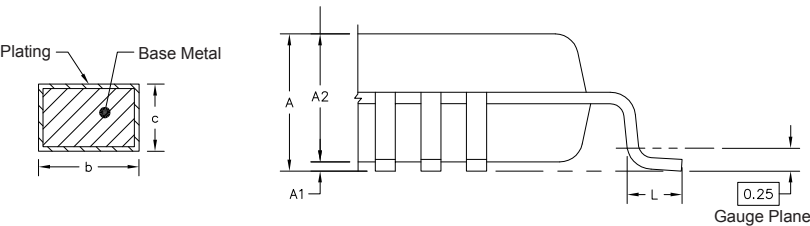
| Measurement | Description                                           | Ball Count |     |     |      |               |      |      | Unit |
|-------------|-------------------------------------------------------|------------|-----|-----|------|---------------|------|------|------|
|             |                                                       | F49        | F81 | W80 | F169 | F324,<br>F576 | F484 | F256 |      |
| G (min.)    | Minimum space required between via trace and spacing. | 0.1        | 0.1 | 0.1 | 0.1  | 0.1           | 0.1  | 0.1  | mm   |

# PCB Guidelines for QFP Packages

## PCB Solder Pad (LQFP Packages)

易灵思 provides LQFP lead dimension information. Use this data when creating your board layout so that the board pads match the landing pads.

Figure 48: LQFP Lead Specification



|                 | Symbol | Min  | Nom  | Max  |
|-----------------|--------|------|------|------|
| Total thickness | A      | –    | –    | 1.6  |
| Stand-off       | A1     | 0.05 | –    | 0.15 |
| Mold thickness  | A2     | 1.35 | 1.4  | 1.45 |
| Lead width      | b      | 0.17 | 0.22 | 0.27 |
| L/F thickness   | c      | 0.09 | –    | 0.2  |
|                 | L      | 0.45 | 0.6  | 0.75 |

Table 14: PCB Solder Pad Recommendations

| Package | Lead Pitch (mm) | Lead Width (mm) |
|---------|-----------------|-----------------|
| LQFP144 | 0.50            | 0.22            |

# Green Packaging

易灵思 FPGAs use packaging solutions that are safer for the environment. These packages are lead (Pb) free and are RoHS compliant. 易灵思 refers to these products as "green" packaging.

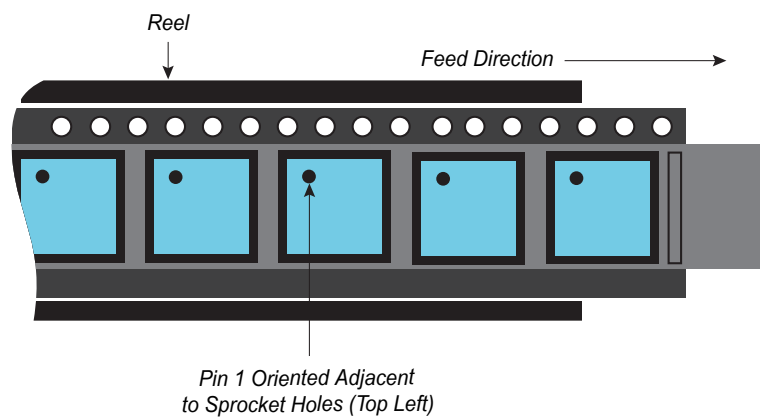
# Tape and Reel Packaging

易灵思 offers BGA and WLCSP devices in tape and reel packaging.

**Table 15: Tape and Reel Packaging**

| Package | Carrier Width (mm) | Cover Width (mm) | Pitch (mm) | Reel Size (in) | Maximum Quantity per Reel |
|---------|--------------------|------------------|------------|----------------|---------------------------|
| FBGA49  | 12                 | 9.3              | 8          | 13             | 5,000                     |
| FBGA81  | 12                 | 9.3              | 8          | 13             | 5,000                     |
| WLCSP80 | 12                 | 9.5              | 8          | 13             | 2,500                     |

**Figure 49: Pin 1 Location (BGA49 and BGA81 Packages)**



**Figure 50: Tape Outline (BGA49 and BGA81 Packages)**

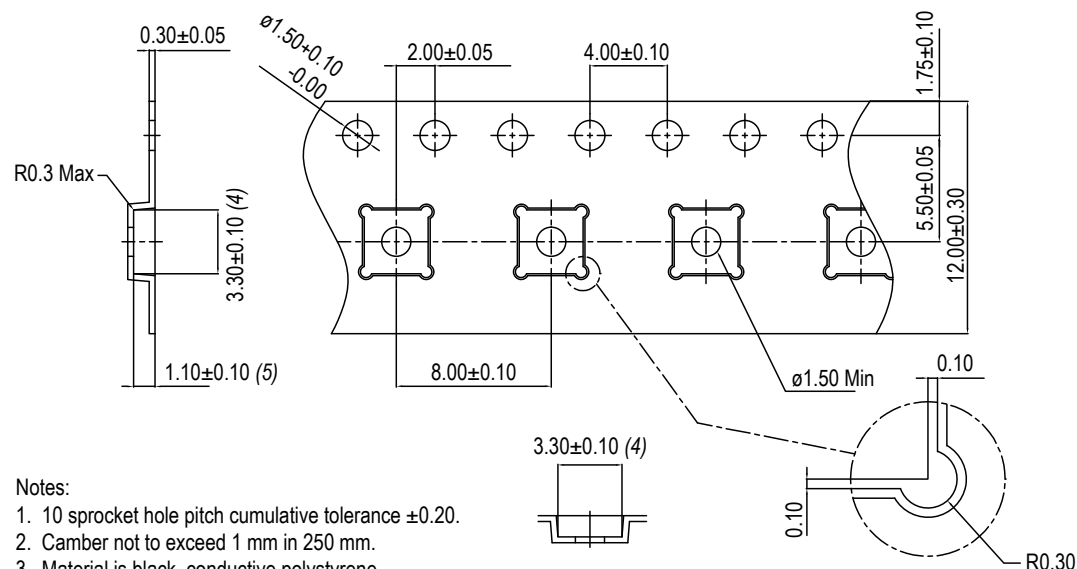


Figure 51: Pin 1 Location (WLCSP80 Packages)

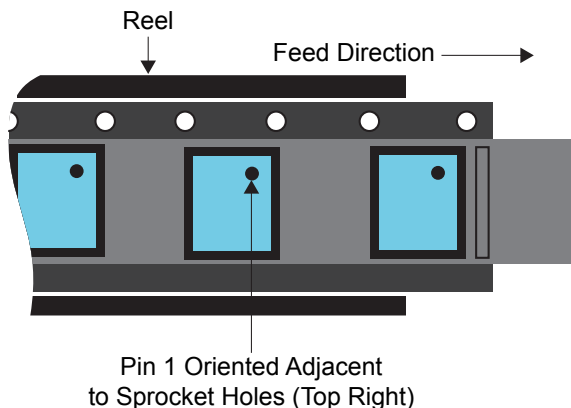
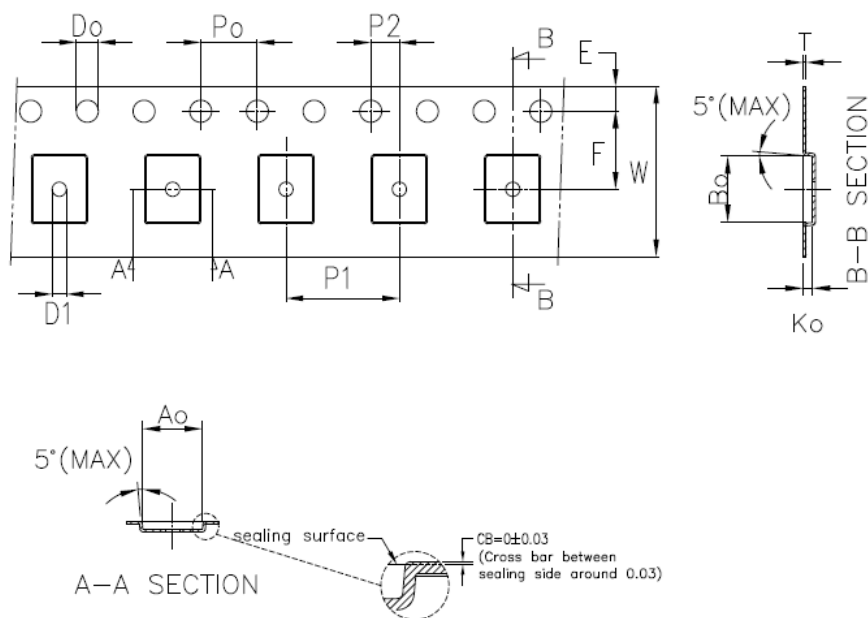


Figure 52: Tape Outline (WLCSP80 Packages)



Unit: mm

| Symbol | $A_o$           | $B_o$           | $K_o$               | $P_o$           | $P_1$           | $P_2$           | $T$             |
|--------|-----------------|-----------------|---------------------|-----------------|-----------------|-----------------|-----------------|
| Spec   | $3.76 \pm 0.05$ | $4.66 \pm 0.05$ | $0.66 \pm 0.05$     | $4.00 \pm 0.10$ | $8.00 \pm 0.10$ | $2.00 \pm 0.05$ | $0.25 \pm 0.03$ |
| Symbol | $E$             | $F$             | $D_o$               | $D_1$           | $W$             | $10P_o$         |                 |
| Spec   | $1.75 \pm 0.10$ | $5.50 \pm 0.05$ | $1.50^{+0.10}_{-0}$ | $1.00 \pm 0.05$ | $12.0 \pm 0.30$ | $40.0 \pm 0.20$ |                 |

## Notice:

1. 10 Sprocket hole pitch cumulative tolerance is  $\pm 0.20$ mm.
2. Carrier camber shall be not more than 1mm per 250mm.
3.  $A_o$  &  $B_o$  measured on a place in the middle of corner radii.
4.  $K_o$  measured from a place on the inside bottom of the pocket to top surface of carrier.
5. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
6. Surface resistivity  $\geq 1.0 \times 10^5$  &  $\leq 1.0 \times 10^8$  ohm/sq.

# Tray Packaging

易灵思 offers BGA and LQFP devices in tray packaging.

*Table 16: Tray Packaging*

| Package | Quantity per Tray | Tray Matrix | Tray Stack | Minimum Quantity per Stack |
|---------|-------------------|-------------|------------|----------------------------|
| FBGA256 | 119               | 7 x 17      | 10 + 1     | 1,190                      |
| FBGA169 | 260               | 10 x 26     | 10 + 1     | 2,600                      |
| LQFP144 | 60                | 12 x 5      | 10 + 1     | 600                        |
| FBGA324 | 168               | 21 x 8      | 10 + 1     | 1,680                      |
| FBGA400 | 84                | 14 x 6      | 10 + 1     | 840                        |
| FBGA484 | 84                | 14 x 6      | 10 + 1     | 840                        |
| FBGA576 | 84                | 14 x 6      | 10 + 1     | 840                        |



# Revision History

**Table 17: Revision History**

| Date          | Version | Description                                                                                                                                                                                                                                                        |
|---------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| December 2021 | 4.0     | Fix incorrect pin names for T55/T85/T120 FPGAs in the BGA324 package. (DOC-671)                                                                                                                                                                                    |
| November 2021 | 3.9     | Fixed incorrect color coding for I/O banks VCCIO_1F_1G in the BGA484 package. (DOC-639)                                                                                                                                                                            |
| November 2021 | 3.8     | Corrected symbols for pins L19 and R15 for the 400 BGA package. (DOC-564)                                                                                                                                                                                          |
| August 2021   | 3.7     | Corrected pin numbering for the WLCSP80 package. (DOC-504)<br>Corrected pitch for F576 in the PCB Solder Pad Recommendations table. (DOC-504)<br>Updated PCB solder pad recommendations (DOC-504)<br>Corrected pin A9 for F256 package pinout. (DOC-493)           |
| July 2021     | 3.6     | Rotated package outline, pinout, and I/O banks figures for the WLCSP80 to make it easier to identify pin 1.                                                                                                                                                        |
| June 2021     | 3.5     | Added thermal resistance data for WLCSP80 package. (DOC-439)<br>Added tape and reel information for WLCSP80. (DOC-439)<br>Added peak reflow temperature for WLCSP80.<br>Corrected typos in BGA256 pinout and fixed mislabeled banks in BGA256 I/O banks. (DOC-452) |
| December 2020 | 3.4     | Added WLCSP80 package information.                                                                                                                                                                                                                                 |
| August 2020   | 3.3     | Updated routing measurements and via measurements.                                                                                                                                                                                                                 |
| July 2020     | 3.2     | Corrected the BGA169 pinout.                                                                                                                                                                                                                                       |
| July 2020     | 3.1     | Updated solder ball co-planarity limit from 0.1 to 0.15.<br>Updated 81-ball FPGA package marking.                                                                                                                                                                  |
| May 2020      | 3.0     | Added guidelines for traces, pads, and vias for PCB design.<br>Added BGA400 package information.<br>Updated side view BGA576 package dimensions.                                                                                                                   |
| February 2020 | 2.1     | Fixed typos in BGA576 pinout and I/O bank diagrams.                                                                                                                                                                                                                |
| January 2020  | 2.0     | Added BGA324, BGA484, and BGA576 package information.                                                                                                                                                                                                              |
| October 2019  | 1.6     | Added LQFP144 package information.                                                                                                                                                                                                                                 |
| August 2019   | 1.5     | Updated BGA169 and BGA256 package marking.                                                                                                                                                                                                                         |
| June 2019     | 1.4     | Added 169 ball FBGA package information.                                                                                                                                                                                                                           |
| February 2019 | 1.3     | Added Thermal resistance, solder pad dimensions, and peak reflow data for the 256 BGA package.<br>Added information on tray packaging.<br>Clarified PLL ground pin in the 81 ball BGA diagram and pinout.<br>Updated 256 ball FBGA package marking.                |
| November 2018 | 1.2     | Added 256 ball FBGA package information.                                                                                                                                                                                                                           |
| August 2018   | 1.1     | Updated BGA81 pin figure.                                                                                                                                                                                                                                          |
| July 2018     | 1.0     | Initial release.                                                                                                                                                                                                                                                   |