










# 钛金系列 FPGA Selector Guide

								
35K to 1,000K Logic Elements	10 Kb Embedded RAM Blocks	DSP Blocks	PLLs	High-Voltage I/O (HVIO)	High-Speed I/O (HSIO)	MIPI D-PHY 2.5 Gbps	DDR4, LPDDR4 Controller & PHY	SerDes 16G/25.8G

## 钛金系列 Ordering Codes

You can use HSIO pairs for a various differential standards such as LVDS (1.6 Gbps), differential HSTL/SSTL, or MIPI RX and TX data/clock lanes (1.5 Gbps).

FPGA	LEs	RAM (kbits)	RAM Blocks (10 Kb)	DSP Blocks	Package	Pins	HVIO	HSIO	PLLs	2.5G MIPI D-PHY	DDR	16G SerDes	PCIe Gen4	25.8G SerDes	Temperature	Speed Grade	Ordering Code
Ti35	36,176	1.53	49	93	FBGA	100	-	61	3	-	-	-	-	-	C	3, 4	Ti35F100S3F2C3/4
					FBGA	225	23	140	4	-	-	-	-	I	4	Ti35F100S3F2I4	
					FBGA	225	23	140	4	-	-	-	-	C	3, 4	Ti35F225C3/4	
					FBGA	225	23	140	4	-	-	-	-	I	4	Ti35F225I4	
Ti60	62,016	2.6	256	160	WLCSP	64	-	35	2	-	-	-	-	-	I	4	Ti60W64I4
					FBGA	100	-	61	3	-	-	-	-	C	3, 4	Ti60F100S3F2C3/4	
					FBGA	100	-	61	3	-	-	-	-	I	4	Ti60F100S3F2I4	
					FBGA	225	23	140	4	-	-	-	-	C	3, 4	Ti60F225C3/4	
					FBGA	225	23	140	4	-	-	-	-	I	4	Ti60F225I4	
					FBGA	225	23	140	4	-	-	-	-	I	4	Ti60F225I4	

## Package Dimensions

Package	Pitch	Dimensions (mm)
64-ball FBGA	0.4	3.5x3.4
100-ball FBGA	0.5	5.5x5.5
225-ball FBGA	0.5	8x8

## Example Ordering Code

钛金系列 FPGA — **Ti60 F225 C 3** — Speed Grade 3, 4

Package Code

Operating Temperature

C: Commercial ( $T_j = 0^\circ\text{C}$  to  $85^\circ\text{C}$ )  
I: Industrial ( $T_j = -40^\circ\text{C}$  to  $100^\circ\text{C}$ )

Some ordering codes include extra characters in the package code to designate additional components in the package. For example, the Ti60 in the F100 package has HyperRAM and flash as indicated by the S3F2 in the package code.