Aurora 8B/10B IP core
by ALSE

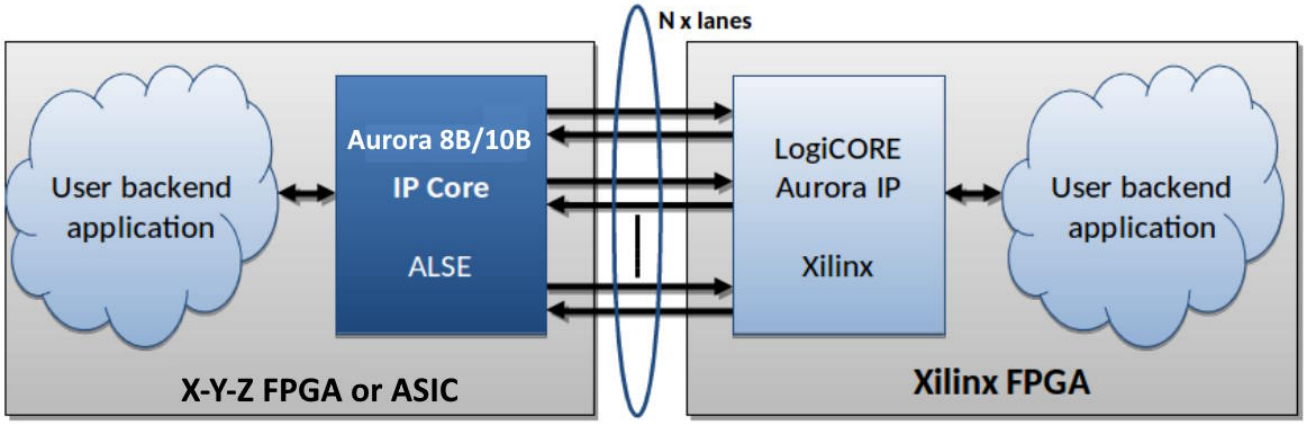
Advanced Logic Synthesis for Electronics

Introduction

Aurora 8B/10B is a public and lightweight protocol suitable for chip-to-chip, board-to-board and backplane communication using high speed transceivers. The **A.L.S.E** Aurora 8B/10B IP core has been ported to most existing FPGAs (Altera/Intel, Lattice, Microchip, Elitestek), it is available for ASICs, and it is compatible and fully interoperable with the Xilinx LogiCORE Aurora 8B/10B IP.

The A.L.S.E IP core provides an efficient way to interconnect FPGAs from the same vendor or from different vendors (and even ASICs) using the open and public Aurora 8B/10B protocol. A common use case is to connect a Xilinx FPGA to an FPGA from another vendor.

Deliverables include a sophisticated HDL simulation environment for seamless development, verification and integration in the final application.



Typical Application

Features

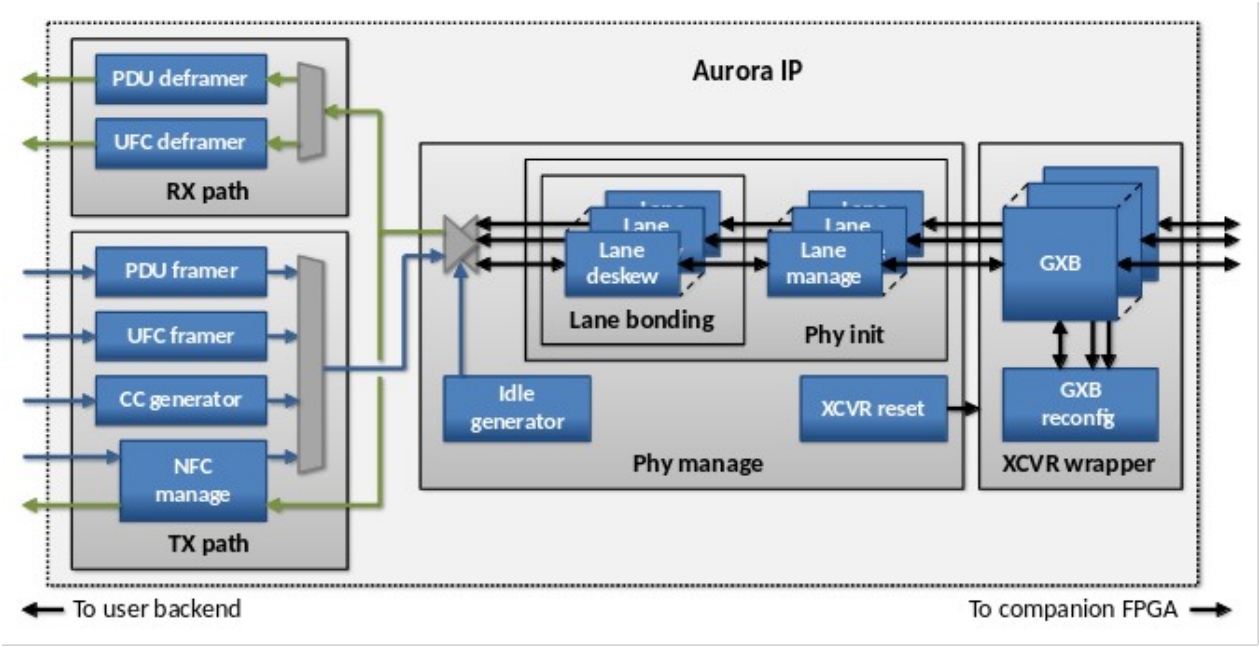
- 8B/10B encoding
- Fully compatible with the standard Xilinx Aurora 8B/10B protocol
- Fully interoperable with the AMD/Xilinx Logicore IP.
- Up to 16 Transceiver (XCVR) physical lanes
- Link Rate up to Device maximum transceiver Rate (e.g Cyclone V = 6.6 Gbps)
- Full Duplex, Simplex Tx and Simplex RX configurations
- Framing and Streaming interfaces
- User Flow Control (UFC)
- Native Flow Control (NFC, immediate/completion modes)
- Additional CRC (optional) for PDU Frames
- Clock Compensation Sequence Generation
- Per lane polarity inversion, skew compensation
- Avalon-ST / AXI like Streaming user interfaces
- Provided with Hardware Reference designs, QIP files (Altera), SDC constraints

Examples of available Reference Designs

- ALSE Cyclone V Clovis/AVDB board ↔ Xilinx Virtex6 ML605 or Xilinx Virtex7 VC707 : 1 lane @ 3.125Gbps
- ReflexCES Intel Arria 10 Attila board ↔ Xilinx Virtex7 VC707 : 1 lane @ 6.25Gbps
- ReflexCES Intel Arria 10 Achilles board ↔ Arria 10 Attila Board : 4 lanes @ 6.25Gbps (Intel-FPGAs on both sides)
- Microchip Polarfire Dev kit ↔ VC 707 @ 5Gbps
- Lattice Certus Pro Nx board ↔ VC 707 @ 5Gbps
- Elitestek TJ-Series TJ375 N1156X Development Kit ↔ VC 707 @ 3.125 Gbps
- etc …

Please note that ALSE can potentially build a demonstrator on any suitable board within a short delay.

Block diagram



High Level Architecture

IP Resource utilization examples

Device	XCVR Lanes	Framing / Streaming	Data Path Width per lane	ALMs	LCs combinational	LC register	Memory Blocks (Memory Bits)
Cyclone V	1	Framing	16	~780	~1280	~1100	2 M10Ks (4096)
	4	Framing	32	~2930	~4850	~4100	10 M10Ks (77824)
	4	Streaming	32	~1750	~2950	~2450	10 M10Ks (77824)
Stratix V	1	Framing	32	~1080	~1760	~1560	4 M20Ks (36864)
	4	Framing	32	~3100	~5100	~4280	8 M20Ks (110592)
	4	Streaming	32	~1950	~3250	~2610	8 M20Ks (110592)
Arria V	1	Framing	32	~970	~1490	~1440	2 M10Ks (4096)
Arria 10	4	Framing	32	~2280	~3040	~3950	4 M20Ks (73728)
	4	Streaming	32	~1200	~1900	~2200	4 M20Ks (73728)
Cyclone 10 GX	4	Framing	32	~2150	~2800	~3550	4 M20Ks (73728)
Stratix 10	4	Framing	32	~2900	~3500	~4000	4 M20Ks (73728)
Microchip MPF300	1	Streaming	32		1112	949	1 x USRam 64x12
Elitestek TJ-Series	1	Streaming	16	99 ADDs	1664 LUTs	943 FFs	0

Note: the numbers above are for **Full Duplex** and include the transceiver logic. Contact ALSE for getting implementation results on other FPGAs, or with specific modes (Simplex, CRC, Number of lanes, etc).

Deliverables and Licensing Schemes

HDL Simulation Environment

- Pre-compiled simulations libraries
- Testbench and Simulation scripts

Complete User's Guide

SDC Constraints, QIP integration file

Hardware Tester Reference Design

Various licensing schemes

- Encrypted RTL (for Altera/Intel)
  - Timed or Untimed
  - Node Locked or Floating
  - Single or Multi-projects
- Source code RTL
- Netlist (per project or for multiple projects)

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