TJ-Series PCIe® Controller Registers User Guide

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Physical Function Configuration Register Set

The PCIe controller has 4 physical functions, which are assigned to function numbers 0 and 3. You can access the function registers by setting `MGMTADDR[20]` to 0 and `MGMT_ADDR[19:12]` to the function number.

Vendor ID and Device ID @0x0

16-bit Vendor ID register and 16-bit Device ID register.

Table 1: i_vendor_id_device_id

Bits	SW	Name	Description	Reset
15:0	R	Vendor ID [VID]	This is the Vendor ID assigned by PCI SIG to the manufacturer of the device. The Vendor ID is set in the Vendor ID Register within the local management register block.	16'h17cd
31:16	R	Device ID [DID]	Device ID assigned by the manufacturer of the device. This field can be re-written independently for each Function from the local management bus.	16'h100

Command and Status Register @0x4

16-bit Command Register and 16-bit Status Register.

Table 2: i_command_status

Bits	SW	Name	Description	Reset
0	R/W	I/O-Space Enable [ISE]	Controls a Function's response to I/O Space accesses received from PCIe Link. The Controller internally uses this bit to respond to received I/O Requests as follows: • When this bit is Clear, all received I/O Space accesses are handled as Unsupported Requests. • When this bit is Set, all received I/O Space accesses are decoded and processed normally. This field can be written from the local management bus.	0x0
1	R/W	Mem-Space Enable [MSE]	Controls a Function's response to Memory Space accesses received from PCIe Link. The Controller internally uses this bit to respond to received Memory Requests as follows: • When this bit is Clear, all received Memory Space accesses are handled as Unsupported Requests. • When this bit is Set, all received Memory Space accesses are decoded and processed normally. This field can be written from the local management bus.	0x0
2	R/W	Bus-Master Enable [BE]	Controls the ability of a Function to issue Memory and I/O Read/Write Requests in the Upstream direction. This field can be written from the local management bus. *Note:* The Controller does not gate any requests based on this bit. The Client Application logic must use this bit to gate requests as follows: • When this bit is Set, the Function is allowed to issue Memory or I/O Requests on the pcie_master_AXI interface. • When this bit is Clear, the Function must not be allowed to issue any Memory or I/O Requests on the pcie_master_AXI interface.	0x0

Bits	SW	Name	Description	Reset
5:3	R	Reserved [R0]	Reserved	0x0
6	R/W	Parity Error Response Enable [PERE]	When this bit is 1, the Controller sets the Master Data Parity Error status bit when it detects the following error conditions: **1.** The Controller receives a poisoned completion from the link in response to a request. **2.** The Controller sends out a poisoned write request on the link (this may be because an underflow occurred during the packet transfer at the host interface of the Controller). When this bit is 0, the Master Data Parity Error status bit is never set. This field can be written from the local management bus.	0x0
7	R	Reserved [R1]	Reserved	0x0
8	R/W	SERR Enable [SE]	Enables the reporting of fatal and non-fatal errors detected by the Controller to the Root Complex. This field can be written from the local management bus.	0x0
9	R	Reserved [R2]	Reserved	0x0
10	R/W	INTx Message Disabled [IMD]	Enables or disables the transmission of INTx Assert and De-assert messages from the Controller. Setting this bit to 1 disables generation of INTx assert/de-assert messages in the Controller. This field can be written from the local management bus.	0x0
15:11	R	Reserved [R3]	Reserved	0x0
18:16	R	Reserved [R4]	Reserved	0x0
19	R	Interrupt Status [IS]	This bit is valid only when the Controller is configured to support legacy interrupts. Indicates that the Controller has a pending interrupt, that is, the Controller has sent an Assert_INTx message but has not transmitted a corresponding Deassert_INTx message.	0x0
20	R	Capabilities List [CL]	Indicates the presence of PCI Extended Capabilities registers. This bit is hardwired to 1.	0x1
23:21	R	Reserved [R5]	Reserved	0x0
24	R/WOCLR	Master Data Parity Error [MDPE]	When the Parity Error Response enable bit is 1, the Controller sets this bit when it detects the following error conditions: **1.** The Controller receives a poisoned completion from the link in response to a request. **2.** The Controller sends out a poisoned write request on the link (this may be because an underflow occurred during the packet transfer at the host interface of the Controller). This bit remains 0 when the Parity Error Response enable bit is 0. This field can also be cleared from the local management bus by writing a 1 into this bit position.	0x0
26:25	R	Reserved [R6]	Reserved	0x0
27	R/WOCLR	Signaled Target Abort [STA]	This bit is set when the Controller has sent a completion to the link with the Completer Abort status. This field can also be cleared from the local management bus by writing a 1 into this bit position.	0x0
28	R/WOCLR	Received Target Abort [RTA]	This bit is set when the Controller has received a completion from the link with the Completer Abort status. This field can also be cleared from the local management bus by writing a 1 into this bit position.	0x0
29	R/WOCLR	Received Master Abort [RMA]	This bit is set when the Controller has received a completion from the link with the Unsupported Request status. This field can also be cleared from the local management bus by writing a 1 into this bit position.	0x0
30	R/WOCLR	Signaled System Error [SSE]	If the SERR enable bit is 1, this bit is set when the Controller has sent out a fatal or non-fatal error message on the link to the Root Complex. If the SERR enable bit is 0, this bit remains 0. This field can also be cleared from the local management bus by writing a 1 into this bit position.	0x0
31	R/WOCLR	Detected Parity Error [DPE]	This bit is set when the Controller has received a poisoned TLP. The Parity Error Response enable bit (bit 6) has no effect on the setting of this bit. This field can also be cleared from the local management bus by writing a 1 into this bit position.	0x0

Revision ID and Class Code Register @0x8

This register contains the Revision ID and Class Code associated with the device incorporating the PCIe Controller.

Table 3: i_revision_id_class_code

Bits	SW	Name	Description	Reset
7:0	R	Revision ID [RID]	Assigned by the manufacturer of the device to identify the revision number of the device. This field can be re-written independently for each Function from the local management bus.	8'h0
15:8	R	Programming Interface Byte [PIB]	Identifies the register set layout of the device. This field can be re-written independently for each Function from the local management bus.	8'h0
23:16	R	Sub-Class Code [SCC]	Identifies a sub-category within the selected function. This field can be re-written independently for each Function from the local management bus.	8'h0
31:24	R	Class Code [CC]	Identifies the function of the device. This field can be re-written independently for each Function from the local management bus.	8'h0

BIST, Header Type, Latency Timer and Cache Line Size Registers @0xc

This location contains the BIST, header-type, Latency Timer and Cache Line Size Registers.

Table 4: i_bist_header_latency_cache_line

Bits	SW	Name	Description	Reset
7:0	R/W	Cache Line Size [CLS]	Cache Line Size Register defined in PCI Specifications 3.0. This field can be read or written both from the link and from the local management bus, but its value is not used.	0x0
15:8	R	Latency Timer [LT]	This is an unused field and is hardwired to 0.	0x0
22:16	R	Header Type [HT]	Identifies format of header. This field is hardwired to 0.	0x0
23	R	Device Type [DT]	Identifies whether the device supports a single Function or multiple Functions. This bit is read as 0 when only Function 0 has been enabled in the Physical Function Configuration Register (in the local management block), and as 1 when more than one Function has been enabled.	0x1
31:24	R	BIST Register [BR]	BIST control register. It can be accessed using local management bus.	0x0

Base Address Register 0 @0x10

This is one of the six Base Address Registers defined by the PCI Specifications 3.0. These registers are used to define address ranges for memory and I/O access to the Endpoint device. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1s into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if BAR 0 is not configured. Otherwise, the number of 1s returned is based on the size of the BAR. BAR 0 can be setup as 32-bit memory or I/O BAR, or can be paired with BAR 1 to form a 64-bit memory BAR. The settings of this BAR are defined in the BAR Configuration Register associated with this PF. The BAR aperture can be controller in two different ways:

1. When the Resizable BAR Capability is enabled, the aperture is controlled by the setting of the BAR width field in Resizable BAR Control Register. The Resizable BAR Capability is enabled by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register 1.
2. When the Resizable BAR Capability is disabled for the Physical Function, the aperture is controlled by the setting of the PF BAR Configuration Register.

Table 5: i_base_addr_0

Bits	SW	Name	Description	Reset
0	R	Memory Space Indicator [MSI0]	Specifies whether this BAR defines a memory address range or an I/O address range (0 = memory, 1 = I/O). The value read in this field is determined by the setting of BAR Configuration Registers of the associated Physical Function.	0x0
1	R	Reserved [R7]	This bit is hardwired to 0 for both memory and I/O BARs.	0x0
2	R	Size [S0]	When the BAR is used to define a memory address range, this field indicates whether the address range is 32-bit or 64-bit (0 = 32-bit, 1 = 64 bit). For 64-bit address ranges, the value in BAR 1 is treated as a continuation of the base address in BAR 0. The value read in this field is determined by the setting of BAR Configuration Registers of the associated Physical Function.	0x0
3	R	Prefetchability [P0]	When the BAR is used to define a memory address range, this field declares whether data from the address range is prefetchable (0 = non- prefetchable, 1 = prefetchable). The value read in this field is determined by the setting of BAR Configuration Registers of the associated Physical Function.	0x0
7:4	R	Reserved [R8]	These bits are hardwired to 0.	0x0
11:8	R	Base Address - RO part [BAMR0]	This field defines the base address of the memory address range. The number of implemented bits in this field determines the BAR aperture configured in BAR Configuration Registers of the associated Physical Function. All other bits are not writeable, and are read as 0's.	0x0
31:12	R/W	Base Address - RW part [BAMRW]	This field defines the base address of the memory address range. The number of implemented bits in this field determines the BAR aperture configured in BAR Configuration Registers of the associated Physical Function.	0x0

Base Address Register 1 @0x14

This is one of the six Base Address Registers defined by the PCI Specifications 3.0. BAR 1 can be setup as 32-bit memory or I/O BAR, or can be paired with BAR 0 to form a 64-bit memory BAR. This register can be used in two distinct ways:

1. When BAR 0 defines a 64-bit memory address range, this register is used to define the high-order bits of the base address. The number of writable bits in this field is based on the aperture setting of the BAR.

2. When the BAR 0 is used to define a 32-bit memory address range or an I/O address range, this register can be used to define a new 32-bit memory address range or an I/O address range. The individual fields in the register have the same format as those of BAR 0 and is described below. The settings of this BAR are defined in the BAR Configuration Register associated with this PF. When configured as a 32-bit memory or I/O BAR, the BAR aperture can be controller in two different ways:
   a. When the Resizable BAR Capability is enabled, the aperture is controlled by the setting of the BAR width field in Resizable BAR Control Register 1. The Resizable BAR Capability is enabled by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register.
   b. When the Resizable BAR Capability is disabled for the Physical Function, the aperture is controlled by the setting of the Physical Function BAR Configuration Register.

Table 6: i_base_addr_1

Bits	SW	Name	Description	Reset
31:0	R	Reserved [R7]	This field is reserved at power-on. This can be changed using BAR configuration register in LM space.	0x0

Base Address Register 2 @0x18

This is one of the six Base Address Registers defined by the PCI Specifications 3.0. These registers are used to define address ranges for memory and I/O accesses to the Endpoint device. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1s into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if BAR 2 is not configured. Otherwise, the number of 1s returned is based on the size of the BAR. BAR2 can be setup as 32-bit memory or I/O BAR, or can be paired with BAR 3 to form a 64-bit memory BAR. The settings of this BAR is defined in the BAR Configuration Register associated with this PF. The BAR aperture can be controller in two different ways:

1. When the Resizable BAR Capability is enabled, the aperture is controlled by the setting of the BAR width field in Resizable BAR Control Register. The Resizable BAR Capability is enabled by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register 1.
2. When the Resizable BAR Capability is disabled for the Physical Function, the aperture is controlled by the setting of the PF BAR Configuration Register.

Table 7: i_base_addr_2

Bits	SW	Name	Description	Reset
31:0	R	Reserved [R7]	This field is reserved at power-on. This can be changed using BAR configuration register in LM space.	0x0

Base Address Register 3 @0x1c

This is one of the six Base Address Registers defined by the PCI Specifications 3.0. BAR 3 can be set up as 32-bit memory or I/O BAR, or can be paired with BAR 2 to form a 64-bit memory BAR. This register can be used in two distinct ways:

- When BAR 2 defines a 64-bit memory address range, this register is used to define the high-order bits of the base address. The number of writable bits in this field is based on the aperture setting of the BAR.
- When the BAR 2 is used to define a 32-bit memory address range or an I/O address range, this register can be used to define a new 32-bit memory address range or an I/O address range.

The individual fields in the register have the same format as those of BAR 2 and is described below. The settings of this BAR are defined in the BAR Configuration Register associated with this PF. When configured as a 32-bit memory or I/O BAR, the BAR aperture can be controller in two different ways:

1. When the Resizable BAR Capability is enabled, the aperture is controlled by the setting of the BAR width field in Resizable BAR Control Register 3. The Resizable BAR Capability is enabled by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register.
2. When the Resizable BAR Capability is disabled for the Physical Function, the aperture is controlled by the setting of the Physical Function BAR Configuration Register.

Table 8: i_base_addr_3

Bits	SW	Name	Description	Reset
31:0	R	Reserved [R7]	This field is reserved at power-on. This can be changed using BAR configuration register in LM space.	0x0

Base Address Register 4 @0x20

This is one of the six Base Address Registers defined by the PCI Specifications 3.0. These registers are used to define address ranges for memory and I/O accesses to the Endpoint device. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1s into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if BAR 4 is not configured. Otherwise, the number of 1s returned is based on the size of the BAR. BAR 4 can be setup as 32-bit memory or I/O BAR, or can be paired with BAR 5 to form a 64-bit memory BAR. The settings of this BAR is defined in the BAR Configuration Register associated with this PF. The BAR aperture can be controller in two different ways:

- When the Resizable BAR Capability is enabled, the aperture is controlled by the setting of the BAR width field in Resizable BAR Control Register. The Resizable BAR Capability is enabled by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register 1.
- When the Resizable BAR Capability is disabled for the Physical Function, the aperture is controlled by the setting of the PF BAR Configuration Register.

Table 9: i_base_addr_4

Bits	SW	Name	Description	Reset
31:0	R	Reserved [R7]	This field is reserved at power-on. This can be changed using BAR configuration register in LM space.	0x0

Base Address Register 5 @0x24

This is one of the six Base Address Registers defined by the PCI Specifications 3.0. BAR 5 can be setup as 32-bit memory or I/O BAR, or can be paired with BAR 4 to form a 64-bit memory BAR. This register can be used in two distinct ways:

1. When BAR 4 defines a 64-bit memory address range, this register is used to define the high-order bits of the base address. The number of writable bits in this field is based on the aperture setting of the BAR.
2. When BAR 4 is used to define a 32-bit memory address range or an I/O address range, this register can be used to define a new 32-bit memory address range or an I/O address range. The individual fields in the register have the same format as those of BAR 4 and is described below. The settings of this BAR is defined in the BAR Configuration Register associated with this PF. When configured as a 32-bit memory or I/O BAR, the BAR aperture can be controller in two different ways:

- When the Resizable BAR Capability is enabled, the aperture is controlled by the setting of the BAR width field in Resizable BAR Control Register 5. The Resizable BAR Capability is enabled by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register.
- When the Resizable BAR Capability is disabled for the Physical Function, the aperture is controlled by the setting of the Physical Function BAR Configuration Register.

Table 10: i_base_addr_5

Bits	SW	Name	Description	Reset
31:0	R	Reserved [R7]	This field is reserved at power-on. This can be changed using BAR configuration register in LM space.	0x0

Reserved @0x28

Table 11: rsvd_0A

Bits	SW	Name	Description	Reset
31:0	R	Reserved [RSVD]	Reserved	0x0

Subsystem Vendor ID and Subsystem ID Register @0x2c

This register contains the Subsystem Vendor ID and Subsystem ID associated with the device incorporating the PCIe Controller.

Table 12: i_subsystem_vendor_id_subsystem_i

Bits	SW	Name	Description	Reset
15:0	R	Subsystem Vendor ID [SVID]	Specifies the Subsystem Vendor ID assigned by the PCI SIG to the manufacturer of the device. Its value comes fom the Subsystem Vendor ID Register in the local management register block.	16'h17cd
31:16	R	Subsystem ID [SID]	Specifies the Subsystem ID assigned by the manufacturer of the device. This field can be re-written independently for each Function from the local management bus.	16'h0

Expansion ROM Base Address Register @0x30

This register is used to define the base address and range of an optional expansion ROM associated with a Function. During the initial configuration of the device, the configuration program determines the presence of the expansion ROM and the size of its address range by writing a pattern of all 1s into the register and reading them back.

If the expansion ROM is not present, a value of all 0s is returned. Otherwise, the program determines the size and base address of the expansion ROM from the value returned, as it is done in the case of other base address registers. A value of 0 is returned by the Controller if the expansion ROM is not configured in the Controller. Otherwise, the number of 1s returned is based on the length of the Expansion ROM Base Address Register. The address bits [10:0] of the Expansion ROM Base Address are always set to 0. Thus, the ROM address space always starts at a 2 Kbyte boundary. The maximum allowed size of the expansion ROM address space is 16 Mbytes. In this version of the Controller, the aperture of the Expansion ROM BAR can be set to any power of 2 in the range from 256 bytes to 16K bytes by programming the EXP_ROM_BAR_aperture field in the PF BAR Configuration Register of the associated

Function. The Expansion ROM BAR is enabled by the setting of the EXP_ROM_BAR_enable bit of the PF BAR Configuration Register associated with the corresponding Function.

Table 13: i_expan_rom_base_addr

Bits	SW	Name	Description	Reset
0	R/W	Address Decode Enable [ADE]	This bit must be set to 1 by the configuration software to enable the expansion ROM. This bit can also be written from the local management bus.	0x0
10:1	R	Reserved [R1]	Reserved	0x0
11	R	ROM Base Address [RBARO]	Defines the base address and range of the expansion ROM address space. The number of writeable bits in this field determines the size of the range (BAR aperture). All other bits are not writeable, and are read as 0's.	0x0
31:12	R/W	ROM Base Address [RBARW]	Defines the base address and range of the expansion ROM address space. The number of writeable bits in this field determines the size of the range (BAR aperture). All other bits are not writeable, and are read as 0's.	0x0

Capabilities Pointer @0x34

This location contains the pointer to the first PCI Capabilities Structure. Its default value points to the Power Management Capability Structure (register number 0x80 hex).

Table 14: i_capabilities_pointer

Bits	SW	Name	Description	Reset
7:0	R	Capabilities Pointer [CP]	Contains pointer to the first PCI Capability Structure. It can be re-written independently for every Function from the local management bus.	0x80
31:8	R	Reserved [R15]	Reserved	0x0

Reserved @0x38

Table 15: rsvd_0E

Bits	SW	Name	Description	Reset
31:0	R	Reserved [RSVD]	Reserved	0x0

Interrupt Line and Interrupt Pin Register @0x3c

This location contains the PCI 3.0 Interrupt Line and Interrupt Pin Registers. These registers are used only when the Controller is configured to support PCI legacy interrupts. If the legacy interrupt mode is configured, the Controller receives interrupt indications from the client logic on its INTA_IN, INTB_IN, INTC_IN and INTD_IN inputs, and sends out Assert_INTx or Deassert_INTx messages on the link in response to their activation or deactivation, respectively. The Interrupt Pin Register defines which of the four inputs is connected to the Function corresponding to this register set. The Interrupt Line register defines the input of the interrupt controller (IRQ0 - IRQ15) in the Root Complex that is activated by each Assert_INTx message.

Table 16: i_intrpt_line_intrpt_pin

Bits	SW	Name	Description	Reset
7:0	R/W	Interrupt Line Register [ILR]	Identifies the IRQx input of the interrupt controller at the Root Complex that is activated by this Functions interrupt (00 = IRQ0, ... , 0F = IRQ15, FF = unknown or not connected). This field is writable from the local management bus.	8'hff
10:8	R	Interrupt Pin Register [IPR]	Identifies the interrupt input (A, B, C, D) to which this Functions interrupt output is connected to (01 = INTA, 02 = INTB, 03 = INTC, 04 = INTD). The assignment of interrupt inputs to Functions is fixed when the Controller is configured. This field can be re-written independently for each Function from the local management bus.	0x1
31:11	R	Reserved [R16]	Reserved	0x0

Reserved @0x40 + [0..15 * 0x4]

Reserved

Table 17: rsvd_010_01F

Bits	SW	Name	Description	Reset
31:0	R	Reserved [RSVD]	Reserved	0x0

Power Management Capabilities Register @0x80

This location contains the Power Management Capabilities Register, its Capability ID, and a pointer to the next capability. This version of the Controller supports the PCI power states D0, D1, and D3.

Table 18: i_pwr_mgmt_cap

Bits	SW	Name	Description	Reset
7:0	R	Capability ID [CID]	Identifies that the capability structure is for Power Management. This field is set by default to 01 hex. It can be re-written independently for each Function from the local management bus.	0x01
15:8	R	Capabilities Pointer [CP]	Contains pointer to the next PCI Capability Structure. This field can be re-written independently for each Function from the local management bus.	8'h90
18:16	R	Version ID [VID]	Indicates the version of the PCI Bus Power Management Specifications that the Function implements. This field is set by default to 011 (Version 1.2). It can be re-written independently for each Function from the local management bus.	0x3
19	R	PME Clock [PC]	Not applicable to PCI Express. This bit is hardwired to 0.	0x0
20	R	Reserved [R0]	Reserved	0x0
21	R	Device Specific Initialization Bit [DSI]	This bit, when set, indicates that the device requires additional configuration steps beyond setting up its PCI configuration space to bring it to the D0 active state from the D0 uninitialized state. This bit is hardwired to 0.	0x0
24:22	R	Max Current Required from Aux Power Supply [MCRAPS]	Specifies the maximum current drawn by the device from the aux power source in the D3cold state. This field is not implemented in devices not supporting PME notification when in the D3cold state, and is therefore hardwired to 0.	0x0
25	R	D1 Support [D1S]	Set if the Function supports the D1 power state. This bit can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.	0x1
26	R	D2 Support [D2S]	Set if the Function supports the D2 power state. Currently hardwired to 0.	0x0

Bits	SW	Name	Description	Reset
27	R	PME Support for D0 State [PSD0S]	Indicates whether the Function is capable of sending PME messages when in the D0 state. This bit is set to 1 by default, but can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.	0x01
28	R	PME Support for D1 State [PSD1S]	Indicates whether the Function is capable of sending PME messages when in the D1 state. This bit can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.	0x1
29	R	PME Support for D2 State [PSD2S]	Indicates whether the Function is capable of sending PME messages when in the D2 state. This bit is hardwired to 0 because D2 state is not supported.	0x0
30	R	PME Support for D3(hot) Statue [PSDHS]	Indicates whether the Function is capable of sending PME messages when in the D3hot state. This bit is set to 1 by default, but can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.	0x01
31	R	PME Support for D3(cold) State [PSDCS]	Indicates whether the Function is capable of sending PME messages when in the D3cold state. Because the device does not have aux power, this bit is hardwired to 0.	0x0

Power Management Control/Status Report @0x84

This location contains the Power Management Control/Status and Data Registers.

Table 19: i_pwr_mgmt_ctrl_stat_rep

Bits	SW	Name	Description	Reset
1:0	R/W	Power State [PS]	Indicates the power state this Function is currently in. This field can be read by the software to monitor the current power state, or can be written to cause a transition to a new state. The valid settings are 00 (state D0), 01 (state D1) and 11 (state D3hot). The software should not write any other value into this field. This field can also be written from the local management bus independently for each Function.	0x0
2	R	Reserved [R4]	Reserved	0x0
3	R	No Soft Reset [NSR]	When this bit is set to 1, the Function will maintain all its state in the PM state D3hot. The software is not required to re-initialize the Function registers on the transition back to D0. This bit is set to 1 by default, but can be modified independently for each PF from the local management bus.	0x01
7:4	R	Reserved [R3]	Reserved	0x0
8	R/W	PME Enable [PE]	Setting this bit enables the notification of PME events from the associated Function. This bit can be set also by writing into this register from the local management bus. This is a sticky field.	0x0
14:9	R	Reserved [R2]	Reserved	0x0
15	R/WOCLR	PME Status [PMES]	When PME notification is enabled, writing a 1 into this bit position from the local management bus sets this bit and causes the Controller to send a PME message from the associated Function. When the Root Complex processes this message, it will turn off this bit by writing a 1 into this bit position through a Config Write. This bit can be set or cleared from the local management bus by writing a 1 or 0, respectively. It can only be cleared from the configuration path (by writing a 1). This is a sticky field.	0x0
23:16	R	Reserved [R1]	Reserved	0x0
31:24	R	Data Register [DR]	This optional register is not implemented in the PCIe Controller. This field is hardwired to 0.	0x0

Reserved @0x88 + [0..1 * 0x4]

Reserved

Table 20: rsvd_022_023

Bits	SW	Name	Description	Reset
31:0	R	Reserved [RSVD]	Reserved	0x0

MSI Control Register @0x90

This register is used only when the Controller is configured to support Message Signaled Interrupts (MSIs). In addition to the MSI control bits, this location also contains the Capability ID for MSI and the pointer to the next PCI Capability Structure.

Table 21: i_msi_ctrl_reg

Bits	SW	Name	Description	Reset
7:0	R	Capability ID [CID1]	Specifies that the capability structure is for MSI. Hardwired to 05 hex.	0x05
15:8	R	Capabilities Pointer [CP1]	Pointer to the next PCI Capability Structure. This can be modified from the local management bus. This field can be written from the local management bus.	8'hb0
16	R/W	MSI Enable [ME]	Set by the configuration program to enable the MSI feature. This field can also be written from the local management bus.	0x0
19:17	R	Multiple Message Capable [MMC]	Encodes the number of distinct messages that the Controller is capable of generating for this Function (000 = 1, 001 = 2, 010 = 4, 011 = 8, 100 = 16, 101 = 32). Thus, this field defines the number of the interrupt vectors for this Function. The Controller allows up to 32 distinct messages, but the setting of this field must be based on the number of interrupt inputs of the Controller that are actually used by the client. For example, if the client logic uses 8 of the 32 distinct MSI interrupt inputs of the Controller for this Function, then the value of this field must be set to 011. This field can be written from the local management bus.	0x0
22:20	R/W	Multiple Message Enable [MME]	Encodes the number of distinct messages that the Controller is programmed to generate for this Function (000 = 1, 001 = 2, 010 = 4, 011 = 8, 100 = 16, 101 = 32). This setting must be based on the number of interrupt inputs of the Controller that are actually used by this Function. This field can be written from the local management bus.	0x0
23	R	64-Bit Address Capable [BAC64]	Set to 1 to indicate that the device is capable of generating 64-bit addresses for MSI messages. Can be modified using the local management interface	0x1
24	R	MSI masking capable [MC]	Can be modified using the local management interface.	0x1
31:25	R	Reserved [R0]	Reserved	0x0

MSI Message Low Address Register @0x94

This register contains the first 32 bits of the address to be used in the MSI messages generated by the Controller for this Function. This address is taken as a 32-bit address if the value programmed in the MSI Message High Address Register is 0. Otherwise, this address is taken as the least significant 32 bits of the 64-bit address sent in MSI messages.

Table 22: i_msi_msg_low_addr

Bits	SW	Name	Description	Reset
1:0	R	Reserved [R1]	The two lower bits of the address are hardwired to 0 to align the address on a double-word boundary.	0x0

Bits	SW	Name	Description	Reset
31:2	R/W	Message Address Low [MAL]	Lower bits of the address to be used in MSI messages. This field can also be written from the local management bus.	0x0

MSI Message High Address Register @0x98

This register contains the most significant 32 bits of the 64-bit address sent by the Controller in MSI messages. A value of all zeroes in this register is taken to mean that the Controller should use 32-bit addresses in the messages.

Table 23: i_msi_msg_hi_addr

Bits	SW	Name	Description	Reset
31:0	R/W	Message Address High [MAH]	Contains bits 63:32 of the 64-bit address to be used in MSI Messages. A value of 0 specifies that 32-bit addresses are to be used in the messages. This field can also be written from the local management bus.	0x0

MSI Message Data Register @0x9c

This register contains the write data to be used in the MSI messages to be generated for the associated PCI Function. When the number of distinct messages programmed in the MSI Control Register is 1, the 32-bit value from this register is used as the data value in the MSI packets generated by the Controller for this Function. If the number of distinct messages is more than 1, the least significant bits of the programmed value are replaced with the encoded interrupt vector [31:0] of the specific message to generate the write data value for the message.

Table 24: i_msi_msg_data

Bits	SW	Name	Description	Reset
15:0	R/W	Message Data [MD]	Message data to be used for this Function. This field can also be written from the local management bus.	0x0
31:16	R	Reserved [R2]	Hardwired to 0.	0x0

MSI Mask Register @0xa0

This register contains the MSI mask bits, one for each of the interrupt levels.

Table 25: i_msi_mask

Bits	SW	Name	Description	Reset
0	R/W	MSI Mask [MM]	Mask bits for MSI interrupts. The Multiple Message Capable field of the MSI Control Register specifies the number of distinct interrupts for the Function, which determines the number of valid mask bits. Please note that if the Multiple Message Capable field is changed from the local management APBbus, then the width of the MSI Mask field also changes accordingly.	0x0
31:1	R	Reserved [R0]	Please note that if the Multiple Message Capable field is changed from the local management APBbus, then the width of this field also changes accordingly.	0x0

MSI Pending Bits Register @0xa4

This register contains the MSI pending interrupt bits, one for each of the interrupt levels.

Table 26: i_msi_pending_bits

Bits	SW	Name	Description	Reset
0	R	MSI Pending Bits [MP]	Pending bits for MSI interrupts. This field can be written from either the APB interface or the MSI_PENDING_STATUS_IN inputs of the Controller depending on the MSI Pending Status In Mode select Bit in the Local Management space. The Multiple Message Capable field of the MSI Control Register specifies the number of distinct interrupts for the Function, which determines the number of valid pending bits. Please note that if the Multiple Message Capable field is changed from the local management APBbus, then the width of the MSI Pending Bits field also changes accordingly.	0x0
31:1	R	Reserved [R0]	Please note that if the Multiple Message Capable field is changed from the local management APB bus, then the width of this field also changes accordingly.	0x0

Reserved @0xa8 + [0..1 * 0x4]

Reserved

Table 27: rsvd_02A_02B

Bits	SW	Name	Description	Reset
31:0	R	Reserved [RSVD]	Reserved	0x0

MSI-X Control Register @0xb0

This register contains the MSI-X configuration bits, the Capability ID for MSI-X and the pointer to the next PCI Capability Structure.

Table 28: i_msix_ctrl

Bits	SW	Name	Description	Reset
7:0	R	Capability ID [CID]	Identifies that the capability structure is for MSI-X. This field is set by default to 11 hex. It can be re-written independently for each Function from the local management bus.	0x11
15:8	R	Capabilities Pointer [CP]	Contains pointer to the next PCI Capability Structure. This is set to point to the PCI Express Capability Structure at 30 hex. This can be re-written independently for each Function from the local management bus.	8'hc0
26:16	R	MSI-X Table Size [MSIXTS]	Specifies the size of the MSI-X Table; that is, the number of interrupt vectors defined for the Function. The programmed value is 1 minus the size of the table (that is, this field is set to 0 if the table size is 1.). It can be re-written independently for each Function from the local management bus.	11'h0
29:27	R	Reserved [R0]	Reserved	0x0
30	R/W	Function Mask [FM]	This bit serves as a global mask to all the interrupt conditions associated with this Function. When this bit is set, the Controller will not send out MSI- X messages from this Function. This field can also be written from the local management bus.	0x0
31	R/W	MSI-X Enable [MSIXE]	Set by the configuration program to enable the MSI-X feature. This field can also be written from the local management bus.	0x0

MSI-X Table Offset Register @0xb4

This register is used to specify the location of the MSI-X Table in memory. All the 32 bits of this register can be re-written independently for each Function from the local management bus.

Table 29: i_msix_tbl_offset

Bits	SW	Name	Description	Reset
2:0	R	BAR Indicator Register [BARI]	Identifies the BAR corresponding to the memory address range where the MSI-X Table is located (000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5).	3'd0
31:3	R	Table Offset [TO]	Offset of the memory address where the MSI- X Table is located relative to the selected BAR. The three least significant bits of the address are omitted as the addresses are QWORD aligned.	29'h0

MSI-X Pending Interrupt Register @0xb8

This register is used to specify the location of the MSI-X Pending Bit Array (PBA). The PBA is a structure in memory containing the pending interrupt bits. All the 32 bits of this register can be re-written independently for each Function from the local management bus.

Table 30: i_msix_pending_intrpt

Bits	SW	Name	Description	Reset
2:0	R	BAR Indicator Register [BARI1]	Identifies the BAR corresponding to the memory address range where the PBA Structure is located (000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5). The value programmed must be the same as the BAR Indicator configured in the MSI-X Table Offset Register. Identifies the BAR corresponding to the memory address range where the PBA Structure is located (000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5). The value programmed must be the same as the BAR Indicator configured in the MSI-X Table Offset Register.	3'd0
31:3	R	PBA Offset [PBAO]	Offset of the memory address where the PBA is located relative to the selected BAR. The three least significant bits of the address are omitted as the addresses are QWORD aligned.	29'h1

Reserved @0xbc Reserved

Table 31: rsvd_02F

Bits	SW	Name	Description	Reset
31:0	R	Reserved [RSVD]	Reserved	0x0

PCI Express Capability List Register @0xc0

This location identifies the PCI Express device type and its capabilities. It also contains the Capability ID for the PCI Express Structure and the pointer to the next capability structure.

Table 32: i_pcie_cap_list

Bits	SW	Name	Description	Reset
7:0	R	Capability ID [CID]	Specifies Capability ID assigned by PCI SIG for this structure. This field is hardwired to 10 hex.	0x010
15:8	R	Next Capability Pointer [NCP]	Points to the next PCI capability structure. Set to 0 because this is the last capability structure.	0x0
19:16	R	Capability Version [PCV]	Identifies the version number of the capability structure. This field is set to 2 by default to indicate that the Controller is compatible to PCI Express Base Specification Revision 3.0. This field can be modified through the local management interface.	0x2
23:20	R	Device Type [DT]	Indicates the type of device implementing this Function. This field is hardwired to 0 in the EP mode.	0x0

Bits	SW	Name	Description	Reset
24	R	Slot Status [SS]	Set to 1 when the link connected to a slot. Hardwired to 0.	0x0
29:25	R	Interrupt Message Number [IMN]	Identifies the MSI or MSI-X interrupt vector for the interrupt message generated corresponding to the status bits in the Slot Status Register, Root Status Register, or this capability structure. This field must be defined based on the chosen interrupt mode: MSI or MSI-X. This field is hardwired to 0.	0x0
30	R	TCS Routing Supported [TRS]	When set to 1, this bit indicates that the device supports routing of Trusted Configuration Requests. Not valid for Endpoints. Hardwired to 0.	0x0
31	R	Reserved [R0]	Reserved	0x0

PCI Express Device Capabilities Register @0xc4

This register advertises the capabilities of the PCI Express device encompassing this Function.

Table 33: i_pcie_dev_cap

Bits	SW	Name	Description	Reset
2:0	R	Max Payload Size [MPS]	Specifies maximum payload size supported by the device.	3'b010
4:3	R	Phantom Functions Supported [PFS]	This field is used to extend the tag field by combining unused Function bits with the tag bits. This field is hardwired to 00 to disable this feature.	0x0
5	R	Extended Tag Field Supported [ETFS]	Set when device allows the tag field to be extended from 5 to 8 bits. It can be re-written independently for each Function from the local management bus.	0x1
8:6	R	Acceptable L0S Latency [AL0SL]	Specifies acceptable latency that the Endpoint can tolerate while transitioning from L0S to L0. It can be re-written independently for each Function from the local management bus.	0x4
11:9	R	Acceptable L1 Latency [AL1SL]	Specifies acceptable latency that the Endpoint can tolerate while transitioning from L1 to L0. It can be re-written independently for each Function from the local management bus.	0x0
14:12	R	Reserved [R1]	Reserved	0x0
15	R	Role-Based Error Reporting [RBER]	Enables role-based error reporting. It is hardwired to 1. It can be re-written independently for each Function from the local management bus.	0x01
17:16	R	Reserved [R2]	Reserved	0x0
25:18	R	Captured Slot Power Limit Value [CSPLV]	Specifies upper limit on power supplied by slot. It can be re-written independently for each Function from the local management bus.	0x0
27:26	R	Captured Power Limit Scale [CPLS]	Specifies the scale used by Slot Power Limit Value. It can be re-written independently for each Function from the local management bus.	0x0
28	R	FLR Capable [FC]	Set when device has Function-Level Reset capability. It is set by default to 1. It can be re-written independently for each Function from the local management bus.	0x01
31:29	R	Reserved [R3]	Reserved	0x0

PCI Express Device Control and Status Register @0xc8

This register contains control and status bits associated with the device implementing this Function. All the read-write bits in this register can also be written from the local management bus. Likewise, bits designated as RW1C can also be cleared by writing a 1 from the local management bus.

Table 34: i_pcie_dev_ctrl_status

Bits	SW	Name	Description	Reset
0	R/W	Enable Correctable Error Reporting [ECER]	Enables the sending of ERR_COR messages by the Controller on the detection of correctable errors.	0x0
1	R/W	Enable Non- Fatal Error Reporting [ENFER]	Enables the sending of ERR_NONFATAL messages by the Controller on the detection of non-fatal errors.	0x0
2	R/W	Enable Fatal Error Reporting [EFER]	Enables the sending of ERR_FATAL messages by the Controller on the detection of fatal errors.	0x0
3	R/W	Enable Unsupported Request Reporting [EURR]	Enables the sending of error messages by the Controller on receiving unsupported requests.	0x0
4	R/W	Enable Relaxed Ordering [ERO]	When set, this bit indicates that the device is allowed to set the Relaxed Ordering bit in the Attributes field of transactions initiated from it when the transactions do not require Strong Ordering.	0x01
7:5	R/W	Max Payload Size [MPS]	Specifies the maximum TLP payload size configured. The device must be able to receive a TLP of this maximum size and should not generate TLPs larger than this value. The configuration program sets this field based on the maximum payload size in the Device Capabilities Register and the capability of the other side.	0x0
8	R/W	Extended Tag Field Enable [ETFE]	Enables the extension of the tag field from 5 to 8 bits.	0x1
9	R	Enable Phantom Functions [EPH]	This field is hardwired to 0 as the Controller does not support this feature.	0x0
10	R	Enable Aux Power [EAP]	Used only when device used aux power. This field is hardwired to 0.	0x0
11	R/W	Enable No Snoop [ENS]	When set to 1, the device is allowed to set the No Snoop bit in initiated transactions in which cache coherency is not needed.	0x1
14:12	R/W	Max Read Request Size [MRRS]	Specifies the maximum size allowed in read requests generated by the device.	0x02
15	R/W	Function-Level Reset [FLR]	Writing a 1 into this bit position generates a Function-Level Reset for the selected Function. This bit reads as 0.	0x0
16	R/WOCLR	Correctable Error Detected [CED]	Set to 1 by the Controller when it detects a correctable error, regardless of whether error reporting is enabled or not, and regardless of whether the error is masked.	0x0
17	R/WOCLR	Non-Fatal Error Detected [NFED]	Set to 1 by the Controller when it detects a non-fatal error, regardless of whether error reporting is enabled or not, and regardless of whether the error is masked.	0x0
18	R/WOCLR	Fatal Error Detected [FED]	Set to 1 by the Controller when it detects a fatal error, regardless of whether error reporting is enabled or not, and regardless of whether the error is masked.	0x0
19	R/WOCLR	Unsupported Request Detected [URD]	Set to 1 by the Controller when it receives an unsupported request, regardless of whether its reporting is enabled or not.	0x0
20	R	Aux Power Detected [APD]	Set when auxiliary power is detected by the device. This is an unused field.	0x0
21	R	Transaction Pending [TP]	Indicates if any of the Non-Posted requests issued by the Function are still pending.	0x0
31:22	R	Reserved [R4]	Reserved	0x0

Link Capabilities Register @0xcc

This register advertises the link-specific capabilities of the device incorporating the PCIe Controller.

Table 35: i_link_cap

Bits	SW	Name	Description	Reset
3:0	R	Maximum Link Speed [MLS]	Indicates the maximum speed supported by the link (2.5 GT/s, 5 GT/s, 8 GT/s, 16 GT/s). This field is hardwired to 0001 (2.5GT/s) when the strap input PCIE_GENERATION_SEL is set to 000, to 0010 (5 GT/s) when the strap is set to 001, to 0011 (8 GT/s) when the strap input is set to 010, and to 0100 (16 GT/s) when the strap input is set to 011 .	0x4
9:4	R	Maximum Link Width [MLW]	Indicates the maximum number of lanes supported by the device. This field is hardwired based on the setting of the LANE_COUNT_IN strap input.	0x4
11:10	R	Active State Power Management [ASPM]	Indicates the level of ASPM support provided by the device. This field can be re-written independently for each Function from the local management bus. When SRIS is enabled in local management register bit, L0s capability is not supported and is forced low.	0x3
14:12	R	L0S Exit Latency [L0SEL]	Specifies the time required for the device to transition from L0S to L0. This parameter is dependent on the Physical Layer implementation. It can be re-written independently for each Function from the local management bus.	0x2
17:15	R	L1 Exit Latency [L1EL]	Specifies the exit latency from L1 state. This parameter is dependent on the Physical Layer implementation. It can be re-written independently for each Function from the local management bus.	0x3
18	R	Clock Power Management [CPM]	Indicates that the device supports removal of referenc clocks. It can be re-written independently for each function from the local management bus.	0x0
19	R	Surprise Down Error Reporting Capability [SDERC]	Indicates the capability of the device to report a Surprise Down error condition. This bit is hardwired to 0 as this capability is applicable to RC ONLY.	0x0
20	R	Data Link Layer Active Reporting Capability [DLLARC]	Set to 1 if the device is capable of reporting that the DL Control and Management State Machine has reached the DL_Active state. This bit is hardwired to 0 as this version of the Controller does not support the feature.	0x0
21	R	Link Bandwidth Notification Capability [LBNC]	A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms. Reserved for Endpoint.	0x0
22	R	ASPM Optionality Compliance [AOC]	Setting this bit indicates that the device supports the ASPM Optionality feature. It can be turned off by writing a 0 to this bit position through the local management bus.	0x1
23	R	Reserved [R5]	Reserved	0x0
31:24	R	Port Number [PN]	Specifies the port number assigned to the PCI Express link connected to this device. It an be modified from the local management bus by writing into Function 0 from the local management bus and will be same value for all functions in a multi-function device.	8'h0

Link Control and Status Register @0xd0

This register contains control and status bits specific to the PCI Express link. All the read-write bits in this register can also be written from the local management bus.

Table 36: i_link_ctrl_status

Bits	SW	Name	Description	Reset
1:0	R/W	Active State Power Management Control [ASPMC]	Controls the level of ASPM support on the PCI Express link associated with this Function. The valid setting are 00: ASPM disabled 01: L0s entry enabled, L1 disabled 10: L1 entry enabled, L0s disabled 11: Both L0s and L1 enabled.	0x0
2	R	Reserved [R6]	Reserved	0x0
3	R/W	Read Completion Boundary (RCB)	Indicates the Read Completion Boundary of the Root Port connected to this Endpoint (0 = 64 bytes, 1 = 128 bytes). This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0

Bits	SW	Name	Description	Reset
4	R	Link Disable [LD]	Writing a 1 to this bit position causes the LTSSM to go to the Disable Link state. The LTSSM stays in the Disable Link state while this bit is set. Reserved for Endpoint mode.	0x0
5	R	Retrain Link [RL]	Setting this bit to 1 causes the LTSSM to initiate link training. Reserved for Endpoint mode. This bit always reads as 0	0x0
6	R/W	Common Clock Configuration [CCC]	A value of 0 indicates that the reference clock of this device is asynchronous to that of the upstream device. A value of 1 indicates that the reference clock is common.	0x0
7	R/W	Extended Synch [ES]	Set to 1 to extend the sequence of ordered sets transmitted while exiting from the L0S state.	0x0
8	R	Enable Clock Power Management [ECPM]	When this bit is set to 1, the device may use the CLKREQ# pin on the PCIe connector to power manage the Link clock. This bit is writeable only when the Clock Power Management bit in the Link Capability Register is set to 1.	0x0
9	R/W	Hardware Autonomous Width Disable [HAWD]	When this bit is set, the local application must not request to change the operating width of the link other than attempting to correct unreliable Link operation by reducing Link width.	0x0
10	R	Link Bandwidth Management Interrupt Enable [LBMIE]	When set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been set. This enables an interrupt to be generated through PHY_INTERRUPT_OUT if triggered. Hardwired to 0 if Link Bandwidth Notification Capability is 0. Not applicable to Endpoints where field is hardwired to 0.	0x0
11	R	Link Autonomous Bandwidth Interrupt Enable [LABIE]	When set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been set. This enables an interrupt to be generated through PHY_INTERRUPT_OUT if triggered. Hardwired to 0 if Link Bandwidth Notification Capability is 0. Not applicable to Endpoints where field is hardwired to 0.	0x0
15:12	R	Reserved [R15_12]	Reserved	0x0
19:16	R	Negotiated Link Speed [NLS]	Negotiated link speed of the device. The only supported speed ids are 2.5 GT/s per lane (0001), 5.0 GT/s per lane (0010), 8.0 GT/s per lane (0011), and 16.0 GT/s per lane (0100).	0x4
25:20	R	Negotiated Link Width [NLW]	Set at the end of link training to the actual link width negotiated between the two sides. Value is undefined if this registers is accessed before link training.	0x4
26	R	Reserved [R8]	Reserved	0x0
27	R	Link Training Status [LTS]	This read-only bit indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/ Recovery state. Not applicable to Endpoints where field is hardwired to 0.	0x0
28	R	Slot Clock Configuration [SCC]	This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference clock on the connector, this bit must be clear. For PF0, this bit can also be written from the local management bus.	0x0
29	R	Data Link Layer Active [DLLA]	Indicates the status of the Data Link Layer. Set to 1 when the DL Control and Management State Machine has reached the DL_Active state. This bit is hardwired to 0 in this version of the Controller.	0x0
30	R/WOCLR	Link Bandwidth Management Status [LBMS]	This bit is set by hardware to indicate that either link training has completed following write to retrain link bit, or when HW has changed link speed or width to attempt to correct unreliable link operation. This triggers an interrupt to be generated through PHY_INTERRUPT_OUT if enabled. Hardwired to 0 if Link Bandwidth Notification Capability is 0. Not applicable to Endpoints where field is hardwired to 0.	0x0

Bits	SW	Name	Description	Reset
31	R/WOCLR	Link Autonomous Bandwidth Status [LABS]	This bit is set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This triggers an interrupt to be generated through PHY_INTERRUPT_OUT if enabled. Hardwired to 0 if Link Bandwidth Notification Capability is 0. Not applicable to Endpoints where field is hardwired to 0.	0x0

Reserved @0xd4

Table 37: rsvd_035

Bits	SW	Name	Description	Reset
31:0	R	Reserved [RSVD]	Reserved	0x0

Reserved @0xd8

Table 38: rsvd_036

Bits	SW	Name	Description	Reset
31:0	R	Reserved [RSVD]	Reserved	0x0

Reserved @0xdc + [0..1 * 0x4]

Table 39: rsvd_037_038

Bits	SW	Name	Description	Reset
31:0	R	Reserved [RSVD]	Reserved	0x0

PCI Express Device Capabilities Register 2 @0xe4

This register advertises the capabilities of the PCI Express device encompassing this Function.

Table 40: i_pcie_dev_cap_2

Bits	SW	Name	Description	Reset
3:0	R	Completion Timeout Ranges [CTR]	Specifies the Completion Timeout values supported by the device. This field is set by default to 0010 (10 ms - 250 ms). The actual timeout values are in two programmable local management registers, which allow the timeout settings of the two sub-ranges within Range B to be programmed independently.	0x02
4	R	Completion Timeout Disable Suported (CTDS)	A 1 in this field indicates that the associated Function supports the capability to turn off its Completion timeout. This bit is set to 1 by default, but can be re-written independently for each Function from the local management bus.	0x01
5	R	ARI forwarding support [AFS]	ARI forwarding supported.	0x0
6	R	OP routing supported [OPRS]	Atomic OP routing supported.	0x0
7	R	32-Bit Atomic Op Completer Supported [BAOCS32]	Hardwired to 0.	0x0
8	R	64-Bit Atomic Op Completer Supported [BAOCS64]	Hardwired to 0.	0x0

Bits	SW	Name	Description	Reset
9	R	128-Bit CAS Atomic Op Completer Supported [BAOCS128]	Hardwired to 0.	0x0
10	R	Reserved [R12]	Reserved	0x0
11	R	LTR Mechanism Supported [LMS]	A 1 in this bit position indicates that the Function supports the Latency Tolerance Reporting (LTR) Capability. This bit is set to 1 by default, but can be turned off for all Physical Functions by writing into PF 0.	0x01
13:12	R	TPH Completer Supported [TCS]	These bits, when set, indicate that the Function is capable of serving as a completer for requests with Transaction Processing Hints (TPH). It can be turned off for all Physical Functions by writing into PF 0. Defined Encodings are: 00b TPH and Extended TPH Completer not supported. 01b TPH Completer supported; Extended TPH Completer not supported. 10b Reserved. 11b Both TPH and Extended TPH Completer supported. Extended Streering tag is not selected in this configuration, hence bit 13 is reserved.	0x01
15:14	R	Reserved [R13]	Reserved	0x0
16	R	10-Bit Tag completer supported [T10CS]	If set function supports 1-bit completer capability; otherwise, the function does not. This field can be modified using local management interface.	0x1
17	R	10-Bit Tag Requester supported [T10RS]	If set function supports 1-bit requester capability; otherwise, the function does not. This bit can be disabled using local management register.	0x0
19:18	R	OBFF Supported [OPFFS]	A 1 in this bit position indicates that the Function supports the Optimized Buffer Flush/Fill (OBFF) capability using message signaling.	0x1
20	R	Extended Format Field Supported [EXFS]	Indicates that the Function supports the 3-bit definition of the Fmt field in the TLP header. This bit is hardwired to 1 for all physical functions.	0x1
21	R	End-End TLP Prefix Supported [EEPS]	Indicates whether the Function supports End-End TLP Prefixes. A 1 in this field indicates that the Function supports receiving TLPs containing End-End TLP Prefixes.	0x01
23:22	R	Max End-End TLP Prefixes [MEEP]	Indicates the maximum number of End-End TLP Prefixes supported by the Function. The supported values are: 01b 1 End-End TLP Prefix 10b 2 End-End TLP Prefixes	0x1
31:24	R	Reserved [R14]	Reserved	0x0

PCI Express Device Control and Status Register 2 @0xe8

This register contains control and status bits associated with the device implementing this Function.

Table 41: i_pcie_dev_ctrl_status_2

Bits	SW	Name	Description	Reset
3:0	R/W	Completion Timeout Value [CTV]	Specifies the Completion Timeout value for the device. Allowable values are 0101 (sub-range 1) and 0110 (sub-range 2). The corresponding timeout values are stored in the local management registers Completion Timeout Interval Registers 0 and 1, respectively. Value of 0 selects completion timeout from Completion-Timeout-Interval-Registers-0 in the local management register.	0x0
4	R/W	Completion Timeout Disable [CTD]	Setting this bit disables Completion Timeout in the device. This bit can also be written from the local management bus.	0x0
5	R	ARI forwarding enable [AFE]	ARI forwarding enable	0x0
6	R	Atomic Op Requester Enable [AORE]	This bit must be set to enable the generation of Atomic Op Requests from the Function. If the client logic attempts to send an Atomic Op for a Function for which this bit is not set, logic in the Controller will nullify the TLP on its way to the link.	0x0
7	R	Reserved [R16]	Reserved	0x0

Bits	SW	Name	Description	Reset
8	R	IDO Request Enable [IDORE]	When this bit is 1, the Function is allowed to set the ID-based Ordering (IDO) Attribute bit in the requests it generates.	0x0
9	R	IDO Completion Enable [IDOCE]	When this bit is 1, the Function is allowed to set the ID-based Ordering (IDO) Attribute bit in the Completions it generates.	0x0
10	R/W	LTR Mechanism Enable [LTRME]	This must be set to 1 to enable the Latency Tolerance Reporting Mechanism. This bit is implemented only in PF 0. Its default value is 1, but can be modified from the local management bus. This bit is read-only in PF 1.	0x0
11	R	Reserved [R17]	Reserved	0x0
12	R	10-Bit Tag Requester Enable [T10RE]	10-bit TAGs generation are not supported in this configuration.	0x0
14:13	R/W	OBFF Enable [OBFFE]	Enables the Optimized Buffer Flush/Fill (OBFF) capability in the device. This field is implemented only in PF 0. Valid settings are 00 (disabled), 01 (Variation A), and 10 (Variation B). This field can also be written from the local management bus. RW if OBFF capability is supported, RO otherwise.	0x0
31:15	R	Reserved [R18]	Reserved	0x0

Link Capabilities Register 2 @0xec

This register advertises the supported link speeds of the Controller.

Table 42: i_link_cap_2_reg

Bits	SW	Name	Description	Reset
0	R	RSVD	Reserved	1'h0
4:1	R	Supported Link Speeds Vector [SLSV]	This field indicates the supported link speeds of the Controller. For each bit, a value of 1 indicates that the corresponding link speed is supported, while a value of 0 indicates that the corresponding speed is not supported. The bits corresponding to various link speeds are: • Bit 1 = Link Speed 2.5 GT/s • Bit 2 = Link Speed 5 GT/s • Bit 3 = Link Speed 8 GT/s • Bit 4 = Link Speed 16 GT/s This field is hardwired to 00001 (2.5 GT/s) when the PCIE_GENERATION_SEL strap pins of the Controller are set to 000, 00011 (2.5 and 5 GT/s) when the strap is set to 001, 00111 (2.5, 5, and 8 GT/s) when the strap pin is set to 010, and 01111 (2.5, 5, 8 GT/s and 16 GT/s) when the strap pin is set to 011. For PF0, this field can be written through the LM interface.	0xf
5	R	RSVD	Reserved	1'h0
8:6	R	Reserved [R1]	Reserved	0x0
12:9	R	Lower SKP OS Generation Supported Speeds Vector [LSOGSSV]	If this field is non-zero, it indicates that the port, when operating at the indicated speed(s), supports SRIS and as well as software control of the SKP Ordered Set transmission scheduling rate.	0x0
15:13	R	Reserved [R2]	Reserved	0x0
19:16	R	Lower SKP OS Reception Supported Speeds Vector [LSORSSV]	If this field is non-zero, it indicates that the port, when operating at the indicated speed(s), supports SRIS and as well as receiving SKP OS at the rate defined for SRNS while running in SRIS.	0x0
20	R	RSVD	Reserved	1'h0
22:21	R	Reserved [R3]	Reserved	0x0
23	R	Retimer Presence Detect Supported [RTPDS]	When set to 1b, this bit indicates that the associated port supports detection and reporting of Retimer presence. This bit is valid for both Downstream Ports and Upstream Ports.	0x1
24	R	Two Retimers Presence Detect Supported [TWRTPDS]	When set to 1b, this bit indicates that the associated port supports detection and reporting of two Retimers presence. This bit is valid for both Downstream Ports and Upstream Ports.	0x1

Bits	SW	Name	Description	Reset
30:25	R	Reserved [R25]	Reserved	0x0
31	R	DRS Supported [R31]	Indicates support for the optional Device Readiness Status (DRS) capability. This capability is currently not supported in the Controller.	0x0

Link Control and Status Register 2 @0xf0

This register contains control and status bits specific to the PCI Express link. All the fields marked RW or RW(STICKY) can also be written from the local management bus.

Table 43: i_link_ctrl_status_2

Bits	SW	Name	Description	Reset
3:0	R/W	Target Link Speed [TLS]	For an upstream component, this field sets an upper limit on Link operational speed during reconfiguration. Additionally for both upstream and downstream components, this field sets the target speed when the software forces the link into Compliance mode by setting the Enter Compliance bit in this register (0001 = 2.5 GT/s, 0010 = 5 GT/s, 0011 = 8 GT/s, 0100 = 16 GT/s). The default value of this field is 0001 (2.5 GT/s) when the PCIE_GENERATION_SEL strap pins of the Controller are set to 000, 0010 (5 GT/s) when the strap is set to 001, 0011 (8 GT/s) when the strap pin is set to 010, and 0100 (16 GT/s) when the strap pin is set to 011. These bits are STICKY.	4'd4
4	R/W	Enter Compliance [EC]	This bit is used to force the Endpoint device to enter Compliance mode. Software sets this bit to 1 and initiates a hot reset to force the device into Compliance mode. The target speed for Compliance mode is determined by the Target Link Speed field of this register. STICKY.	0x0
5	R/W	Hardware Autonomous Speed Disable [HASD]	When this bit is set, the LTSSM is prevented from changing the operating speed of the link, other than reducing the speed to correct unreliable operation of the link. STICKY	0x0
6	R	Selectable De- emphasis [SDE]	This bit selects the de-emphasis level when the Controller is operating at 5 GT/s (0 = -6 dB, 1 = -3.5 dB). This is reserved for Endpoints.	0x0
9:7	R/W	Transmit Margin [TM]	This field is intended for debug and compliance testing purposes only. It controls the non-de-emphasized voltage level at the transmitter outputs. Its encodings are: • 000: Normal operating range • 001: 800 - 1200 mV for full swing and 400 - 700 mV for half swing • 010 - 111: See PCI Express Base Specification 2.0 This field is reset to 0 when the LTSSM enters the Polling Configuration substate during link training. STICKY.	0x0
10	R/W	Enter Modified Compliance [EMC]	This field is intended for debug and compliance testing purposes only. If this bit is set to 1, the device will transmit the Modified Compliance Pattern when the LTSSM enters the Polling Compliance substate. *Note:*Setting this bit alone will not cause the LTSSM to enter Polling.Compliance. The Enter Compliance bit must also be set and a Hot Reset needs to be initiated by Host to enter Polling.Compliance. STICKY.	0x0
11	R/W	Compliance SOS [CS]	When this bit is set to 1, the device will transmit SKP ordered sets between compliance patterns. STICKY.	0x0
15:12	R/W	Compliance De-Emphasis [CDE]	This bit sets the de-emphasis level (for 5 GT/s operation) or the Transmitter Preset level (for 8 GT/s or 16 GT/s operation) when the LTSSM enters the Polling.Compliance state because of software setting the Enter Compliance bit in this register. It is used only when the link is running at 5 GT/s, 8 GT/s, or 16 GT/s. At 5 GT/s, the only valid setting are 0 (-6 dB) and 1 (-3.5 dB). STICKY.	0x0

Bits	SW	Name	Description	Reset
16	R	Current De- Emphasis Level [CDEL]	This status bit indicates the current operating de-emphasis level of the transmitter (0 = -6 dB, 1 = -3.5 dB). This field is undefined when link is not at Gen2 speed.	0x0
17	R	Equalization 8.0 GT/s Complete [EQC]	This bit, when set to 1, indicates that the Transmitter Equalization procedure has completed for 8.0 GT/s. STICKY.	0x0
18	R	Equalization 8.0 GT/s Phase 1 Successful [EP1S]	This bit, when set to 1, indicates that the Phase 1 of the Transmitter Equalization procedure has completed successfully for 8.0 GT/s. STICKY.	0x0
19	R	Equalization 8.0 GT/s Phase 2 Successful [EP2S]	This bit, when set to 1, indicates that the Phase 2 of the Transmitter Equalization procedure has completed successfully for 8.0 GT/s. STICKY.	0x0
20	R	Equalization 8.0 GT/s Phase 3 Successful [EP3S]	This bit, when set to 1, indicates that the Phase 3 of the Transmitter Equalization procedure has completed successfully for 8.0 GT/s. STICKY.	0x0
21	R/WOCLR	Link Equalization Request 8.0 GT/s [LE]	This bit is Set by Controller hardware to request the 8.0 GT/s Link equalization process to be performed on the Link. Controller hardware sets this bit if a link equalization problem is detected at the end of equalization at 8GT/s. Additionally, the Client Firmware may set this bit while requesting equalization through Local Management EP 8GTs Request Equalization Retrain Link bit. This bit is cleared by writing a 1 to this bit position by the host, or writing a 0 from the LMI. STICKY.	0x0
22	R	Retimer Presence Detected [RTP]	When set to 1b, this bit indicates that a Retimer was present during the most recent Link negotiation.	0x0
23	R	Two Retimers Presence Detected [TWRTP]	When set to 1b, this bit indicates that two Retimers were present during the most recent Link negotiation.	0x0
27:24	R	Reserved [R21]	Reserved	0x0
30:28	R	Downstream Component Presence [DCP]	DRS is not supported by the Controller and hence this field is not implemented.	0x0
31	R	DRS Message Received [DMR]	DRS is not supported by the Controller and hence this field is not implemented.	0x0

Reserved @0xf4 + [0..2 * 0x4]

Table 44: rsvd_03D_03F

Bits	SW	Name	Description	Reset
31:0	R	Reserved [RSVD]	Reserved	0x0

Advanced Error Reporting (AER) Enhanced Capability Header Register @0x100

This is the first register in the PCI Express Advanced Error Reporting Capability Structure. This register contains the PCI Express Extended Capability ID, the capability version, and the pointer to the next capability structure.

Table 45: i_AER_enhanced_cap_hdr

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PEECI]	This field is hardwired to the Capability ID assigned by PCI SIG to the PCI Express AER Extended Capability Structure (0001 hex).	0x01
19:16	R	Capability Version [CV]	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 4'h2, but can be modified from the local management bus.	4'h2

Bits	SW	Name	Description	Reset
31:20	R	Next Capability Offset [NCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h140

Uncorrectable Error Status Register @0x104

This register provides the status of the various uncorrectable errors detected by the PCI Express Controller. Software may clear any error bit by writing a 1 into the corresponding bit position. The states of the bits in the Uncorrectable Error Mask Register have no effect on the status bits of this register. The setting of an uncorrectable error status bit causes the Controller to generate an ERR_FATAL message if the corresponding severity bit of the Uncorrectable Error Severity Register is 1. If the severity bit is 0, however, there are two separate ways the error can be processed:

- In certain cases, the uncorrectable error is treated as an Advisory Non-Fatal Error. These cases are treated as similar to correctable errors, causing the Controller to generate an ERR_COR message instead of an ERR_NONFATAL message. For details on these special cases, refer to Section 6.2.3.2.4 of the PCI Express Base Specifications, Version 1.1.
- In all other cases, the Controller sends an ERR_NONFATAL message when the error is detected.

In all cases, the sending of the error message can be suppressed by setting the bit corresponding to the error type in the Uncorrectable Error Mask Register. For errors that are not Function-specific, the error status bus is set in the registers belonging to all the Functions associated with the link, but only a single message is generated for the entire link. In the case of certain errors detected by the Transaction Layer, the associated TLP header is logged in the Header Log Registers. All the RW1C bits can also be cleared from the local management bus by writing a 1 into the bit position. If the error emulation emulation feature is enabled (i.e., if bit 12 of Debug MUX Control 3 register is asserted), f/w will be allowed to write into the AER uncorrectable Error status register.

Table 46: i_uncorr_err_status

Bits	SW	Name	Description	Reset
0	R/WOCLR	Link Training Error status [LTE]	This error indicates that link training is not successful and transition back to detect state. This Status bit is set on any LTSSM transition from Configuration to Detect or Recovery to Detect. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit 12 of Debug MUX Control 3 register is asserted).	0x0
3:1	R	Reserved [R0]	Reserved	0x0
4	R/WOCLR	Data Link Protocol Error Status [DLPES]	This bit is set when the Controller receives an Ack or Nak DLLP whose sequence number does not correspond to that of an unacknowledged TLP or that of the last acknowledged TLP (for details, refer to PCI Express Base Specification 1.1, Section 3.5.2). This error is not Function-specific and is reported by Function 0. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit 12 of Debug MUX Control 3 register is asserted).	0x0
5	R	Surprise down error status [SDES]	This error status indicates Link up to Link down event. So Status bit is set upon LINK_DOWN_RESET_OUT event. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit 12 of Debug MUX Control 3 register is asserted).	0x0
11:6	R	Reserved [R1]	Reserved	0x0

Bits	SW	Name	Description	Reset
12	R/WOCLR	Poisoned TLP Status [PTS]	This bit is set when the Controller receives a poisoned TLP from the link. This error is Function-specific. This error is considered non-fatal by default. The error is reported by sending an ERR_NONFATAL message. The header of the received TLP with error is logged in the Header Log Registers. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit 12 of Debug MUX Control 3 register is asserted).	0x0
13	R/WOCLR	Flow Control Protocol Error Status [FCPES]	This bit is set when certain violations of the flow control protocol are detected by the Controller. Controller reports FCPE upon the following conditions: **1.** InitFC/UpdateFC DLLP received which issues more than 2047 cumulative outstanding unused credits to the Transmitter for data payload or 127 for header, **2.** InitFC_P is received with Payload Credits less than 128B, **3.** InitFC_CPL is received with Payload Credits less than 128B. This error is not Function-specific. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit 12 of Debug MUX Control 3 register is asserted).	0x0
14	R/WOCLR	Completion Timeout Status [CTS]	This bit is set when the completion timer associated with an outstanding request times out. This error is Function-specific. This error is considered non-fatal by default. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit 12 of Debug MUX Control 3 register is asserted).	0x0
15	R/WOCLR	Completer Abort Status [CAS]	This bit is set when the Controller has returned the Completer Abort (CA) status to a request received from the link. This error is Function-specific. The header of the received request that caused the error is logged in the Header Log Registers. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit 12 of Debug MUX Control 3 register is asserted).	0x0
16	R/WOCLR	Unexpected Completion Status [UCS]	This bit is set when the Controller has received an unexpected Completion packet from the link. This error is not Function-specific. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit 12 of Debug MUX Control 3 register is asserted).	0x0
17	R/WOCLR	Receiver Overflow Status [ROS]	This bit is set when the Controller receives a TLP in violation of the receive credit currently available. This error is not Function-specific. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit 12 of Debug MUX Control 3 register is asserted).	0x0
18	R/WOCLR	Malformed TLP Status [MTS]	This bit is set when the Controller receives a malformed TLP from the link. This error is not Function-specific. This error is considered fatal by default, and is reported by sending an ERR_FATAL message. The header of the received TLP with error is logged in the Header Log Registers. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit 12 of Debug MUX Control 3 register is asserted).	0x0
19	R/WOCLR	ECRC Error Status [EES]	This bit is set when the Controller has detected an ECRC error in a received TLP. This error is not Function-specific. The header of the received TLP with error is logged in the Header Log Registers. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit 12 of Debug MUX Control 3 register is asserted).	0x0
20	R/WOCLR	Unsupported Request Error Status [URES]	This bit is set when the Controller has received a request from the link that it does not support. This error is not Function-specific. This error is considered non-fatal by default. In the special case described in Sections 6.2.3.2.4.1 of the PCI Express Specifications, the error is reported by sending an ERR_COR message. In all other cases, the error is reported by sending an ERR_NONFATAL message. The header of the received request that caused the error is logged in the Header Log Registers. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit 12 of Debug MUX Control 3 register is asserted).	0x0
21	R	Reserved [R2]	Reserved	0x0

Bits	SW	Name	Description	Reset
22	R/WOCLR	Uncorrectable Internal Error Status [UIE]	This bit is set when the Controller has detected an internal uncorrectable error (HAL parity error or an uncorrectable ECC error while reading from any of the RAMs). This bit is also set in response to the client signaling an internal error through the input UNCORRECTABLE_ERROR_IN. This error is not Function-specific. This error is considered fatal by default, and is reported by sending an ERR_FATAL message. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit 12 of Debug MUX Control 3 register is asserted).	0x0
31:23	R	Reserved [R3]	Reserved	0x0

Uncorrectable Error Mask Register @0x108

The mask bits in this register control the reporting of uncorrectable errors. For each error type in the Uncorrectable Error Status Register there is a corresponding bit in this register to mask its reporting. Setting the mask bit has the following effects:

- The occurrence of the error is not reported to the Root Complex (by a PCI Express error message).
- The header of the TLP in which the error was detected is not logged in the Header Log Registers.
- The First Error Pointer in the Advanced Error Capabilities and Control Register is not updated on detection of the error.

The individual bits of the mask register are described below. The bits marked RW can also be written from the local management bus.

Table 47: i_uncorr_err_mask

Bits	SW	Name	Description	Reset
0	R/W	Link Training Error Mask [LTEM]	This bit is set to mask the reporting of Link Training Error Mask. STICKY.	0x0
3:1	R	Reserved [R4]	Reserved	0x0
4	R/W	Data Link Protocol Error Mask [DLPEM]	This bit is set to mask the reporting of Data Link Protocol Errors. STICKY.	0x0
5	R	Surprise Down Error Status Mask [SDESM]	This bit is set to mask the reporting of Surprise Down Error Status Mask. STICKY.	0x0
11:6	R	Reserved [R5]	Reserved	0x0
12	R/W	Poisoned TLP Mask [PTM]	This bit is set to mask the reporting of a Poisoned TLP. STICKY.	0x0
13	R/W	Flow Control Protocol Error Mask [FCPEM]	This bit is set to mask the reporting of Flow Control Protocol Errors. STICKY.	0x0
14	R/W	Completion Timeout Mask [CTM]	This bit is set to mask the reporting of Completion Timeouts. STICKY.	0x0
15	R/W	Completer Abort Mask [CAM]	This bit is set to mask the reporting of the Controller sending a Completer Abort. STICKY.	0x0
16	R/W	Unexpected Completion Mask [UCM]	This bit is set to mask the reporting of unexpected Completions received by the Controller. STICKY.	0x0
17	R/W	Receiver Overflow Mask [ROM]	This bit is set to mask the reporting of violations of receive credit. STICKY.	0x0
18	R/W	Malformed TLP Mask [MTM]	This bit is set to mask the reporting of malformed TLPs received from the link. STICKY.	0x0
19	R/W	ECRC Error Mask [EEM]	This bit is set to mask the reporting of ECRC errors. STICKY.	0x0
20	R/W	Unsupported Request Error Mask [UREM]	This bit is set to mask the reporting of unexpected requests received from the link. STICKY.	0x0
21	R	Reserved [R6]	Reserved	0x0
22	R/W	Uncorrectable Internal Error Mask [UIEM]	This bit is set to mask the reporting of internal errors. STICKY.	0x1

Bits	SW	Name	Description	Reset
31:23	R	Reserved [R7]	Reserved	0x0

Uncorrectable Error Severity Register @0x10c

The setting of this register determines whether an uncorrectable error is reported as a fatal error on non-fatal error to the Root Complex. If a severity bit of this register is 0, the corresponding error is reported by the Controller using an ERR_NONFATAL message. Otherwise, it is reported using an ERR_FATAL message. The bits marked RW can also be written from the local management bus.

Table 48: i_uncorr_err_severity

Bits	SW	Name	Description	Reset
0	R/W	Link Training Error Severity [LTES]	Severity of Link Training Error (0 = Non-Fatal, 1 = Fatal). STICKY.	0x0
3:1	R	Reserved [R8]	Reserved	0x0
4	R/W	Data Link Protocol Error Severity [DLPER]	Severity of Data Link Protocol Errors (0 = Non-Fatal, 1 = Fatal). STICKY.	0x01
5	R	Surprise Down Error Severity [SDES]	Severity of Surprise Down Error Severity (0 = Non-Fatal, 1 = Fatal). STICKY.	0x1
11:6	R	Reserved [R10]	Reserved	0x0
12	R/W	Poisoned TLP Severity [PTS]	Severity of a Poisoned TLP error (0 = Non-Fatal, 1 = Fatal). STICKY.	0x0
13	R/W	Flow Control Protocol Error Severity [FCPES]	Severity of Flow Control Protocol Errors (0 = Non-Fatal, 1 = Fatal). STICKY.	0x01
14	R/W	Completion Timeout Severity [CTS]	Severity of Completion Timeouts (0 = Non-Fatal, 1 = Fatal). STICKY.	0x0
15	R/W	Completer Abort Severity [CAS]	Severity of sending a Completer Abort (0 = Non-Fatal, 1 = Fatal). STICKY.	0x0
16	R/W	Unexpected Completion Severity [UCS]	Severity of unexpected Completions received by the Controller (0 = Non-Fatal, 1 = Fatal). STICKY.	0x0
17	R/W	Receiver Overflow Severity [ROS]	Severity of receive credit violations (0 = Non-Fatal, 1 = Fatal). STICKY.	0x01
18	R/W	Malformed TLP Severity [MTS]	Severity of malformed TLPs received from the link (0 = Non-Fatal, 1 = Fatal). STICKY.	0x01
19	R/W	ECRC Error Severity [EES]	Severity of ECRC errors (0 = Non-Fatal, 1 = Fatal). STICKY.	0x0
20	R/W	Unsupported Requeset Error Severity [URES]	Severity of unexpected requests received from the link (0 = Non-Fatal, 1 = Fatal). STICKY.	0x0
21	R	Reserved [R11]	Reserved	0x0
22	R/W	Uncorrectable Internal Error Severity [UIES]	Severity of internal errors (0 = Non-Fatal, 1 = Fatal). STICKY.	0x01
31:23	R	Reserved [R12]	Reserved	0x0

Correctable Error Status Register @0x110

This register provides the status of the various correctable errors detected by the PCI Express Controller. Software may clear any error bit by writing a 1 into the corresponding bit position. The states of the bits in the Correctable Error Mask Register have no effect on the status bits of this register. The setting of a correctable error status bit causes the Controller to generate an ERR_COR error message to the Root Complex if the error is not masked in the Correctable Error Mask Register. For errors that are not Function-specific, the error status bus is set in the registers belonging to all the Functions associated with the link, but only a single message is generated for the entire link. Header logging of received TLPs does not apply to correctable errors. All the RW1C bits can also be cleared from the local management bus by writing a 1 into the bit position. F/w will be allowed to write into AER correctable error status field when

error emulation emulation feature is enabled (i.e., if bit 12 of Debug MUX Control 3 register is asserted).

Table 49: i_corr_err_status

Bits	SW	Name	Description	Reset
0	R/WOCLR	Receiver Error Status [RES]	This bit is set when an error is detected in the receive side of the Physical Layer of the Controller (e.g. a bit error or coding violation). This bit is set upon any of the following errors: **1.** PHY reported 8B10B error, Disparity Error, Elastic Buffer Overflow Error, Underflow Error **2.** GEN3 TLP, DLLP Framing Errors **3.** OS Block Received Without EDS **4.** Data Block Received After EDS **5.** Illegal OS Block After EDS **6.** OS Block Received After SKIP OS **7.** OS Block Received After SDS **8.** Sync Header Error **9.** Loss of Gen3 Block Alignment This error is not Function-specific. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted	0x0
5:1	R	Reserved [R12]	Reserved	0x0
6	R/WOCLR	Bad TP Status [BTS]	This bit is set when an error is detected in a received TLP by the Data Link Layer of the Controller. The conditions causing this error are: • an LCRC error • the packet terminates with EDB symbol, but its LCRC field does not equal the inverted value of the calculated CRC. This error is not Function-specific. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted)	0x0
7	R/WOCLR	Bad DLLP Status [BDS]	This bit is set when an LCRC error is detected in a received DLLP, and no errors were detected by the Physical Layer. This error is not Function- specific. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).	0x0
8	R/WOCLR	Replay Number Rollover Status [RNRS]	This bit is set when the replay count rolls over after three re-transmissions of a TLP at the Data Link Layer of the Controller. This error is not Function-specific STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).	0x0
11:9	R	Reserved [R13]	Reserved	0x0
12	R/WOCLR	Replay Timer Timeout Status [RTTS]	This bit is set when the replay timer in the Data Link Layer of the Controller times out, causing the Controller to retransmit a TLP. This error is not Function-specific. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).	0x0
13	R/WOCLR	Advisory Non- Fatal Error Status [ANFES]	This bit is set when an uncorrectable error occurs, which is determined to belong to one of the special cases described in Section 6.2.3.2.4 of the PCI Express 2.0 Specifications. This causes the Controller to generate an ERR_COR message in place of an ERR_NONFATAL message. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).	0x0
14	R/WOCLR	Corrected Internal Error Status [CIES]	This bit is set when the Controller has detected an internal correctable error condition (a correctable ECC error while reading from any of the RAMs). This bit is also set in response to the client signaling an internal error through the input CORRECTABLE_ERROR_IN. This error is not Function-specific. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).	0x0

Bits	SW	Name	Description	Reset
15	R/WOCLR	Header Log Overflow Status [HLOS]	This bit is set on a Header Log Register overflow, that is, when the header could not be logged in the Header Log Register because it is occupied by a previous header. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).	0x0
31:16	R	Reserved [R14]	Reserved	0x0

Correctable Error Mask Register @0x114

The mask bits in this register control the reporting of correctable errors. For each error type in the Correctable Error Status Register, there is a corresponding bit in this register to mask its reporting. When a mask bit is set, the occurrence of the error is not reported to the Root Complex (by a PCI Express error message). The individual bits of the mask register are described below. The bits marked RW can also be written from the local management bus.

Table 50: i_corr_err_mask

Bits	SW	Name	Description	Reset
0	R/W	Receiver Error Mask [REM]	This bit, when set, masks the generation of error messages in response to the Physical Layer errors STICKY.	0x0
5:1	R	Reserved [R15]	Reserved	0x0
6	R/W	Bad TLP Mask [BTM]	This bit, when set, masks the generation of error messages in response to a 'Bad TLP' received. STICKY.	0x0
7	R/W	Bad DLLP Mask [BDM]	This bit, when set, masks the generation of error messages in response to a 'Bad DLLP' received. STICKY.	0x0
8	R/W	Replay Number Rollover Mask [RNRM]	This bit, when set, masks the generation of error messages in response to a Replay Number Rollover event. STICKY.	0x0
11:9	R	Reserved [R16]	Reserved	0x0
12	R/W	Replay Timer Timeout Mask [RTTM]	This bit, when set, masks the generation of error messages in response to a Replay Timer timeout event. STICKY.	0x0
13	R/W	Advisory Non-Fatal Error Mask [ANFEM]	This bit, when set, masks the generation of error messages in response to an uncorrectable error occur, which is determined to belong to one of the special cases (as described in Section 6.2.3.2.4 of the PCI Express 2.0 Specifications). STICKY.	0x01
14	R/W	Corrected Internal Error Mask [CIEM]	This bit, when set, masks the generation of error messages in response to a corrected internal error condition. STICKY.	0x01
15	R/W	Header Log Overflow Mask [HLOM]	This bit, when set, masks the generation of error messages in response to a Header Log register overflow. STICKY.	0x01
31:16	R	Reserved [R17]	Reserved	0x0

Advanced Error Capabilities and Control Register @0x118

This register contains a pointer to the first error that is reported in the Uncorrectable Error Status Register, and bits to enable ECRC generation and checking.

Table 51: i_advcd_err_cap_ctrl

Bits	SW	Name	Description	Reset
4:0	R	First Error Pointer [FER]	This is a 5-bit pointer to the bit position in the Uncorrectable Error Status Register corresponding to the error that was detected first. When there are multiple bits set in the Uncorrectable Error Status Register, this field informs the software which error was observed first. To prevent the field from being overwritten before software was able to read it, this field is not updated while the status bit pointed by it in the Uncorrectable Error Status Register remains set. After the software clears this status bit, a subsequent error condition that sets any bit in the Uncorrectable Error Status Register will update the First Error Pointer. Any uncorrectable error type, including the special cases where the error is reported using an ERR_COR message, will set the First Error Pointer (assuming the software has reset the error pointed by it in the Uncorrectable Error Status Register). STICKY. F/w will be allowed to write into this first error pointer when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).	0x0
5	R	ECRC Generation Capability [EGC]	This read-only bit indicates to the software that the device is capable of generating ECRC in packets transmitted on the link. This bit is writable from the local management bus.	0x1
6	R/W	Enable ECRC Generation [EEG]	Setting this bit enables the ECRC generation on the transmit side of the Controller. This bit is writable from the local management bus. STICKY.	0x0
7	R	ECRC Check Capability [ECC]	This read-only bit indicates to the software that the device is capable of checking ECRC in packets received from the link. This bit is writable from the local management bus.	0x1
8	R/W	Enable ECRC Check [EEC]	Setting this bit enables ECRC checking on the receive side of the Controller. This bit is writable from the local management bus. STICKY.	0x0
9	R	Multiple Header Recording Capable (MHRC)	This bit is set when the Function has the capability to log more than one error header in its Header Log Registers. It is hardwired to 0.	0x0
10	R	Multiple Header Recording Enable [MHRE]	Setting this bit enables the Function to log multiple error headers in its Header Log Registers. It is hardwired to 0	0x0
11	R	Tlp Prefix Log Present [TPLP]	If Set and the First Error Pointer is valid, indicates that the TLP Prefix Log register contains valid information. If Clear or if First Error Pointer is invalid, the TLP Prefix Log register is undefined. Default value of this bit is 0. This bit is RsvdP if the End-End TLP Prefix Supported bit is CIf Set and the First Error Pointer is valid, indicates that the TLP Prefix Log register contains valid information. If Clear or if First Error Pointer is invalid, the TLP Prefix Log register is undefined.	0x0
31:12	R	Reserved [R18]	Reserved	0x0

Header Log Register 0 @0x11c

This is the first of a set of four registers used to capture the header of a TLP received by the Controller from the link upon detection of an uncorrectable error. When multiple bits are set in the Uncorrectable Error Status Register, the captured header corresponds to the error that was detected first, that is, the error pointed by the First Error Pointer. To prevent the captured header from being over-written before software was able to read it, this register is not updated while the status bit pointed by the First Error Pointer in the Uncorrectable Error Status Register remains set. After the software clears this status bit, a subsequent error condition that sets any bit in the Uncorrectable Error Status Register will also cause the Header Log Registers to be updated. The doublewords of the TLP header are stored in the Header Log Registers with their bytes transposed. That is, the byte containing the Type/Format fields of the header is stored at bit positions 31:24 of the Header Log Register 0. F/w will be allowed to write Header log info when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).

Table 52: i_hdr_log_0

Bits	SW	Name	Description	Reset
31:0	R	Header DWORD 0 [HD0]	First DWORD of captured TLP header STICKY.	0x0

Header Log Register 1 @0x120

This register contains the second DWORD of the captured TLP header. The bytes are stored in transposed order.

Table 53: i_hdr_log_1

Bits	SW	Name	Description	Reset
31:0	R	Header DWORD 1 [HD1]	Second DWORD of captured TLP header STICKY.	0x0

Header Log Register 2 @0x124

This register contains the third DWORD of the captured TLP header. The bytes are stored in transposed order.

Table 54: i_hdr_log_2

Bits	SW	Name	Description	Reset
31:0	R	Header DWORD 2 [HD2]	Third DWORD of captured TLP header STICKY.	0x0

Header Log Register 3 @0x128

If the captured TLP header is four DWORDs long, this register contains its fourth DWORD. If the captured header is a three-DWORD header, this register is unused. The bytes of the DWORD are stored in this register in transposed order.

Table 55: i_hdr_log_3

Bits	SW	Name	Description	Reset
31:0	R	Header DWORD 3 [HD3]	Fourth DWORD of captured TLP header STICKY.	0x0

Reserved @0x12c + [0..2 * 0x4]

Table 56: rsvd_04B_04D

Bits	SW	Name	Description	Reset
31:0	R	Reserved [RSVD]	Reserved	0x0

TLP Prefix Log Register 0 @0x138

First TLP Prefix (if present) associated with the TLP whose header is in the Header Log Register. The bytes are in transposed order. F/w will be allowed to write TLP prefix log info when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).

Table 57: i_tlp_pre_log_0

Bits	SW	Name	Description	Reset
31:0	R	TLP Prefix 0 [HD1]	First TLP Prefix of captured TLP STICKY.	0x0

TLP Prefix Log Register 1 @0x13c

Second TLP Prefix (if present) associated with the TLP whose header is in the Header Log Register. The bytes are in transposed order. F/w will be allowed to write TLP prefix log info when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).

Table 58: i_tlp_pre_log_1

Bits	SW	Name	Description	Reset
31:0	R	TLP Prefix 1 [HD1]	Second TLP Prefix of captured TLP STICKY.	0x0

ARI Extended Capability Header Register @0x140

This register is used to enable the Alternate Routing ID interpretation. This register contains the PCI Express Extended Capability ID, the capability version, and the pointer to the next capability structure.

Table 59: i_ARI_ext_cap_hdr

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECID]	This field is hardwired to the Capability ID assigned by PCI SIG to the ARI Extended Capability (000E hex).	0x0E
19:16	R	Capability Version [ARICV]	Specifies the SIG-assigned value for the version of the capability structure. This field is set to 1 by default, but can be modified independently for each Function from the local management bus	0x01
31:20	R	Next Capability Offset [ARINCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h150

ARI Capability Register and ARI Control Register @0x144

This location contains the ARI Capability Register and the ARI Control Register. The individual fields are described below.

Table 60: i_ARI_cap_and_ctrl

Bits	SW	Name	Description	Reset
0	R	MFVC Function Groups Capability [MFGC]	Set when device supports arbitration at the Function Group-level. This field is hardwired to 0.	0x0
1	R	ACS Function Groups Capability [AFGC]	Relevant only when ACS Capability is supported. This field is hardwired to 0.	0x0
7:2	R	RSVD	RSVD	6'h00
15:8	R	Next Function [NF]	Points to the next Physical Function in the device. This field is set by default to point to the next Physical Function, 0 for last Function. It can be re-written from the local management bus.	0x1
31:16	R	ARI Control Register [ACR]	ARI Control Register not implemented in this Controller. This field is hardwired to 0.	0x0

Reserved @0x148 + [0..1 * 0x4]

Table 61: rsvd_052_053

Bits	SW	Name	Description	Reset
31:0	R	Reserved [RSVD]	Reserved	0x0

Device Serial Number Capability Header Register @0x150

This register contains the PCI Express Extended Capability ID for Device Serial Number Capability, the capability version, and the pointer to the next capability structure.

Table 62: i_dev_ser_num_cap_hdr

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECID]	This field is hardwired to the Capability ID assigned by PCI SIG to the PCI Express Device Serial Number Capability (0001 hex).	0x03
19:16	R	Capability Version [DSNCV]	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus by writing into Function 0 from the local management bus.	0x01
31:20	R	Next Capability Offset [SNNCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h160

Device Serial Number Register 0 @0x154

This read-only register stores the first 32 bits of the device's serial number. This setting is common for all the Physical Functions and can be modified by writing into this register in Function 0 from the local management bus.

Table 63: i_dev_ser_num_0

Bits	SW	Name	Description	Reset
31:0	R	Device Serial Number, Doubleword 0 [DSND0]	This field contains the first 32 bits of the device's serial number.	0x0

Device Serial Number Register 1 @0x158

This read-only register stores the last 32 bits of the device's serial number. This setting is common for all the Physical Functions and can be modified by writing into this register in Function 0 from the local management bus.

Table 64: i_dev_ser_num_1

Bits	SW	Name	Description	Reset
31:0	R	Device Serial Number, Doubleword 1 (DSND1)	This field contains the last 32 bits of the device's serial number.	0x0

Reserved @0x15c

Table 65: rsvd_057

Bits	SW	Name	Description	Reset
31:0	R	Reserved [RSVD]	Reserved	0x0

Power Budgeting Enhanced Capability Header @0x160

This register contains the PCI Express Extended Capability ID for Power Budgeting Capability, its capability version, and the pointer to the next capability structure.

Table 66: i_pwr_bdgtg_enhc_cap_hdr

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECID]	This field is hardwired to the Capability ID assigned by PCI SIG to the PCI Express Power Budgeting Capability (0004 hex).	0x04
19:16	R	Capability Version [PCV]	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus by writing into Function 0 from the local management bus.	0x01
31:20	R	Next Capability Offset [PBNCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h1b8

Power Budgeting Data Select Register @0x164

This register is used to select the specific word of specific power-budgeting data returned on a read from the Power Budgeting Data Register. This version of the Controller stores power budgeting data for three distinct power states (i.e., D0, D1 and D3hot) for each Physical Function, which can be read from the Power Budgeting Data Register by indexing through this register, as described below.

Table 67: i_pwr_bdgtg_data_sel

Bits	SW	Name	Description	Reset
7:0	R/W	Power Budgeting Data Index [PBDN]	This field selects the power budgeting data read from the Power Budgeting Data Register. Its settings are: • 00: Selects power budgeting data for power state D0 MAX for the associated PF. • 01: Selects power budgeting data for power state D0 SUSTAINED for the associated PF. • 10: Selects power budgeting data for power state D3hot for the associated PF. • 11: Selects power budgeting data for power state D1 for the associated PF. • Others: Not a valid setting. A read from the Power Budgeting Data Register returns all zeroes.	0x0
31:8	R	Reserved [R0]	Reserved.	0x0

Power Budgeting Data Register @0x168

This read-only register returns the DWORD of Power Budgeting Data selected by the Data Select register. Each DWORD of the Power Budgeting Data describes the power usage of the device in a particular operating condition. All the fields can be modified independently for each PF by writing from the local management bus.

Table 68: i_pwr_bdgtg_data_register

Bits	SW	Name	Description	Reset
7:0	R	Base Power [BP]	Specifies base power (in watts) of the selected power state.	8'd240
9:8	R	Data Scale [DS]	Scale factor applicable to the Base Power field.	0x0
12:10	R	PM Sub-State [PSS]	Specifies the power management sub-state of the selected power state.	0x0
14:13	R	PM State [PS]	Specifies the power management state of the Function for which this power management data applies.	0x0
17:15	R	Type [TYPE]	Specifies the operation condition for which the data applies.	0x7
20:18	R	Power Rail [PR]	Specifies the power rail corresponding to the power management data in this register.	0x2
31:21	R	Reserved [R1]	Reserved	0x0

Power Budget Capability Register @0x16c

This register specifies whether the device power specified by this Capability Structure is included in the system power budget.

Table 69: i_pwr_bdgt_cap

Bits	SW	Name	Description	Reset
0	R	System Allocated [SA]	This bit is set to indicate that the device power specified by this Power Management Capability Structure is included in the system power budget. When this bit set, the software must exclude the device power reported by this Capability Structure from power calculations when making power budgeting decisions. This bit is set to 0 by default, but its setting can be modified individually for each PF from the local management bus.	0x0
31:1	R	Reserved [R4]	Reserved	0x0

Reserved @0x170 + [0..3 * 0x4]

Table 70: rsvd_05C_05F

Bits	SW	Name	Description	Reset
31:0	R	Reserved [RSVD]	Reserved	0x0

Resizable BAR Extended Capability Header Register @0x180

This register contains the PCI Express Extended Capability ID for the Resizable BAR Capability, its capability version, and the pointer to the next capability structure. This register is enabled only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration

Register (Section 8.4.2.24). When the Resizable BAR Capability is not enabled, a read from this location returns all zeroes.

Table 71: i_resize_BAR_ext_cap_hdr

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECID]	This field is hardwired to the Capability ID assigned by PCI SIG to the Resizable BAR Capability (0015 hex).	0x0
19:16	R	Capability Version [CV]	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus.	0x0
31:20	R	Next Capability Offset [NCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h0

Resizable BAR Capability Register 0 @0x184

This register advertises the available aperture settings of the first memory BAR of the associated Physical Function. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability (bit 31) of the associated Physical Function BAR Configuration Register 1. When the Resizable BAR Capability is not enabled, a read from this location returns all zeros. When the Resizable BAR Capability is enabled, any of the bits 4–22 can be modified from the local management bus.

Table 72: i_resize_BAR_cap_0

Bits	SW	Name	Description	Reset
3:0	R	Reserved [R0]	Reserved	0x0
4	R/W	Aperture 1M [A1M]	Indicates that the BAR aperture can be set to 1M.	0x0
5	R/W	Aperture 2M [A2M]	Indicates that the BAR aperture can be set to 2M.	0x0
6	R/W	Aperture 4M [A4M]	Indicates that the BAR aperture can be set to 4M.	0x0
7	R/W	Aperture 8M [A8M]	Indicates that the BAR aperture can be set to 8M.	0x0
8	R/W	Aperture 16M [A16M]	Indicates that the BAR aperture can be set to 16M.	0x0
9	R/W	Aperture 32M [A32M]	Indicates that the BAR aperture can be set to 32M.	0x0
10	R/W	Aperture 64M [A64M]	Indicates that the BAR aperture can be set to 64M.	0x0
11	R/W	Aperture 128M [A128M]	Indicates that the BAR aperture can be set to 128M.	0x0
12	R/W	Aperture 256M [A256M]	Indicates that the BAR aperture can be set to 256M.	0x0
13	R/W	Aperture 512M [A512M]	Indicates that the BAR aperture can be set to 512M.	0x0
14	R/W	Aperture 1G [A1G]	Indicates that the BAR aperture can be set to 1G.	0x0
15	R/W	Aperture 2G [A2G]	Indicates that the BAR aperture can be set to 2G.	0x0
16	R/W	Aperture 4G [A4G]	Indicates that the BAR aperture can be set to 4G.	0x0
17	R/W	Aperture 8G [A8G]	Indicates that the BAR aperture can be set to 8G.	0x0
18	R/W	Aperture 16G [A16G]	Indicates that the BAR aperture can be set to 16G.	0x0
19	R/W	Aperture 32G [A32G]	Indicates that the BAR aperture can be set to 32G.	0x0
20	R/W	Aperture 64G [A64G]	Indicates that the BAR aperture can be set to 64G.	0x0
21	R/W	Aperture 128G [A128G]	Indicates that the BAR aperture can be set to 128G.	0x0
22	R/W	Aperture 256G [A256G]	Indicates that the BAR aperture can be set to 256G.	0x0
23	R/W	Aperture 512G [A512G]	Indicates that the BAR aperture can be set to 512G.	0x0
31:24	R	Reserved [R1]	Reserved	0x0

Resizable BAR Control Register 0 @0x188

This register controls the aperture setting of the first memory BAR of the associated Physical Function, and also has a field that specifies the number of resizable BARs configurable through the Resizable BAR Capability Structure. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register. When the Resizable BAR Capability is not enabled, a read from this location returns all zeroes. When the Resizable BAR Capability is enabled, all valid fields of this register can be modified from the local management bus.

Table 73: i_resize_BAR_ctrl_0

Bits	SW	Name	Description	Reset
2:0	R/W	BAR Index [BARI]	Specifies the index of the BAR controlled by this register. This field can be modified independently for each PF from the local management bus.	0x0
4:3	R	Reserved [R2]	Reserved	0x0
7:5	R/W	Resizable BAR Count [RBARC]	Specifies the number of BARs that can be configured through the Resizable BAR Capability Structure for this PF. This field can be modified independently for each PF from the local management bus.	0x0
12:8	R/W	BAR Size [BARS]	When the Resizable BAR Capability is enabled for the Physical Function, this field controls the BAR aperture for the first BAR of the PF (0 = 1M, 1 = 2M, ... , 12 = 4G). This field can be modified independently for each PF from the local management bus.	0x0
31:13	R	Reserved [R3]	Reserved	0x0

Resizable BAR Capability Register 1 @0x18c

This register advertises the available aperture settings of the first memory BAR of the associated Physical Function. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability (bit 31) of the associated Physical Function BAR Configuration Register 1. When the Resizable BAR Capability is not enabled, a read from this location returns all zeros. When the Resizable BAR Capability is enabled, any of the bits 4-22 can be modified from the local management bus.

Table 74: i_resize_BAR_cap_1

Bits	SW	Name	Description	Reset
3:0	R	Reserved [R0]	Reserved	0x0
4	R/W	Aperture 1M [A1M]	Indicates that the BAR aperture can be set to 1M.	0x0
5	R/W	Aperture 2M [A2M]	Indicates that the BAR aperture can be set to 2M.	0x0
6	R/W	Aperture 4M [A4M]	Indicates that the BAR aperture can be set to 4M.	0x0
7	R/W	Aperture 8M [A8M]	Indicates that the BAR aperture can be set to 8M.	0x0
8	R/W	Aperture 16M [A16M]	Indicates that the BAR aperture can be set to 16M.	0x0
9	R/W	Aperture 32M [A32M]	Indicates that the BAR aperture can be set to 32M.	0x0
10	R/W	Aperture 64M [A64M]	Indicates that the BAR aperture can be set to 64M.	0x0
11	R/W	Aperture 128M [A128M]	Indicates that the BAR aperture can be set to 128M.	0x0
12	R/W	Aperture 256M [A256M]	Indicates that the BAR aperture can be set to 256M.	0x0
13	R/W	Aperture 512M [A512M]	Indicates that the BAR aperture can be set to 512M.	0x0
14	R/W	Aperture 1G [A1G]	Indicates that the BAR aperture can be set to 1G.	0x0
15	R/W	Aperture 2G [A2G]	Indicates that the BAR aperture can be set to 2G.	0x0
16	R/W	Aperture 4G [A4G]	Indicates that the BAR aperture can be set to 4G.	0x0

Bits	SW	Name	Description	Reset
17	R/W	Aperture 8G [A8G]	Indicates that the BAR aperture can be set to 8G.	0x0
18	R/W	Aperture 16G [A16G]	Indicates that the BAR aperture can be set to 16G.	0x0
19	R/W	Aperture 32G [A32G]	Indicates that the BAR aperture can be set to 32G.	0x0
20	R/W	Aperture 64G [A64G]	Indicates that the BAR aperture can be set to 64G.	0x0
21	R/W	Aperture 128G [A128G]	Indicates that the BAR aperture can be set to 128G.	0x0
22	R/W	Aperture 256G [A256G]	Indicates that the BAR aperture can be set to 256G.	0x0
23	R/W	Aperture 512G [A512G]	Indicates that the BAR aperture can be set to 512G.	0x0
31:24	R	Reserved [R1]	Reserved	0x0

Resizable BAR Control Register 1 @0x190

This register controls the aperture setting of the first memory BAR of the associated Physical Function, and has a field that specifies the number of resizable BARs configurable through the Resizable BAR Capability Structure. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register. When the Resizable BAR Capability is not enabled, a read from this location returns all zeroes. When the Resizable BAR Capability is enabled, all valid fields of this register can be modified from the local management bus.

Table 75: i_resize_BAR_ctrl_1

Bits	SW	Name	Description	Reset
2:0	R/W	BAR Index [BARI]	Specifies the index of the BAR controlled by this register. This field can be modified independently for each PF from the local management bus.	0x0
4:3	R	Reserved [R2]	Reserved	0x0
7:5	R/W	Resizable BAR Count [RBARC]	Specifies the number of BARs that can be configured through the Resizable BAR Capability Structure for this PF. This field can be modified independently for each PF from the local management bus.	0x0
12:8	R/W	BAR Size [BARS]	When the Resizable BAR Capability is enabled for the Physical Function, this field controls the BAR aperture for the first BAR of the PF (0 = 1M, 1 = 2M, ..., 12 = 4G). This field can be modified independently for each PF from the local management bus.	0x0
31:13	R	Reserved [R3]	Reserved	0x0

Resizable BAR Capability Register 2 @0x194

This register advertises the available aperture settings of the first memory BAR of the associated Physical Function. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability (bit 31) of the associated Physical Function BAR Configuration Register 1. When the Resizable BAR Capability is not enabled, a read from this location returns all zeros. When the Resizable BAR Capability is enabled, any of the bits 4–22 can be modified from the local management bus.

Table 76: i_resize_BAR_cap_2

Bits	SW	Name	Description	Reset
3:0	R	Reserved [R0]	Reserved	0x0
4	R/W	Aperture 1M [A1M]	Indicates that the BAR aperture can be set to 1M.	0x0
5	R/W	Aperture 2M [A2M]	Indicates that the BAR aperture can be set to 2M.	0x0
6	R/W	Aperture 4M [A4M]	Indicates that the BAR aperture can be set to 4M.	0x0
7	R/W	Aperture 8M [A8M]	Indicates that the BAR aperture can be set to 8M.	0x0

Bits	SW	Name	Description	Reset
8	R/W	Aperture 16M [A16M]	Indicates that the BAR aperture can be set to 16M.	0x0
9	R/W	Aperture 32M [A32M]	Indicates that the BAR aperture can be set to 32M.	0x0
10	R/W	Aperture 64M [A64M]	Indicates that the BAR aperture can be set to 64M.	0x0
11	R/W	Aperture 128M [A128M]	Indicates that the BAR aperture can be set to 128M.	0x0
12	R/W	Aperture 256M [A256M]	Indicates that the BAR aperture can be set to 256M.	0x0
13	R/W	Aperture 512M [A512M]	Indicates that the BAR aperture can be set to 512M.	0x0
14	R/W	Aperture 1G [A1G]	Indicates that the BAR aperture can be set to 1G.	0x0
15	R/W	Aperture 2G [A2G]	Indicates that the BAR aperture can be set to 2G.	0x0
16	R/W	Aperture 4G [A4G]	Indicates that the BAR aperture can be set to 4G.	0x0
17	R/W	Aperture 8G [A8G]	Indicates that the BAR aperture can be set to 8G.	0x0
18	R/W	Aperture 16G [A16G]	Indicates that the BAR aperture can be set to 16G.	0x0
19	R/W	Aperture 32G [A32G]	Indicates that the BAR aperture can be set to 32G.	0x0
20	R/W	Aperture 64G [A64G]	Indicates that the BAR aperture can be set to 64G.	0x0
21	R/W	Aperture 128G [A128G]	Indicates that the BAR aperture can be set to 128G.	0x0
22	R/W	Aperture 256G [A256G]	Indicates that the BAR aperture can be set to 256G.	0x0
23	R/W	Aperture 512G [A512G]	Indicates that the BAR aperture can be set to 512G.	0x0
31:24	R	Reserved [R1]	Reserved	0x0

Resizable BAR Control Register 2 @0x198

This register controls the aperture setting of the first memory BAR of the associated Physical Function, and has a field that specifies the number of resizable BARs configurable through the Resizable BAR Capability Structure. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register. When the Resizable BAR Capability is not enabled, a read from this location returns all zeroes. When the Resizable BAR Capability is enabled, all valid fields of this register can be modified from the local management bus.

Table 77: i_resize_BAR_ctrl_2

Bits	SW	Name	Description	Reset
2:0	R/W	BAR Index [BARI]	Specifies the index of the BAR controlled by this register. This field can be modified independently for each PF from the local management bus.	0x0
4:3	R	Reserved [R2]	Reserved	0x0
7:5	R/W	Resizable BAR Count [RBARC]	Specifies the number of BARs that can be configured through the Resizable BAR Capability Structure for this PF. This field can be modified independently for each PF from the local management bus.	0x0
12:8	R/W	BAR Size [BARS]	When the Resizable BAR Capability is enabled for the Physical Function, this field controls the BAR aperture for the first BAR of the PF (0 = 1M, 1 = 2M, ..., 12 = 4G). This field can be modified independently for each PF from the local management bus.	0x0
31:13	R	Reserved [R3]	Reserved	0x0

Resizable BAR Capability Register 3 @0x19c

This register advertises the available aperture settings of the first memory BAR of the associated Physical Function. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability (bit 31) of the associated Physical Function BAR Configuration Register 1. When the Resizable BAR Capability is not

enabled, a read from this location returns all zeros. When the Resizable BAR Capability is enabled, any of the bits 4–22 can be modified from the local management bus.

Table 78: i_resize_BAR_cap_3

Bits	SW	Name	Description	Reset
3:0	R	Reserved [R0]	Reserved	0x0
4	R/W	Aperture 1M [A1M]	Indicates that the BAR aperture can be set to 1M.	0x0
5	R/W	Aperture 2M [A2M]	Indicates that the BAR aperture can be set to 2M.	0x0
6	R/W	Aperture 4M [A4M]	Indicates that the BAR aperture can be set to 4M.	0x0
7	R/W	Aperture 8M [A8M]	Indicates that the BAR aperture can be set to 8M.	0x0
8	R/W	Aperture 16M [A16M]	Indicates that the BAR aperture can be set to 16M.	0x0
9	R/W	Aperture 32M [A32M]	Indicates that the BAR aperture can be set to 32M.	0x0
10	R/W	Aperture 64M [A64M]	Indicates that the BAR aperture can be set to 64M.	0x0
11	R/W	Aperture 128M [A128M]	Indicates that the BAR aperture can be set to 128M.	0x0
12	R/W	Aperture 256M [A256M]	Indicates that the BAR aperture can be set to 256M.	0x0
13	R/W	Aperture 512M [A512M]	Indicates that the BAR aperture can be set to 512M.	0x0
14	R/W	Aperture 1G [A1G]	Indicates that the BAR aperture can be set to 1G.	0x0
15	R/W	Aperture 2G [A2G]	Indicates that the BAR aperture can be set to 2G.	0x0
16	R/W	Aperture 4G [A4G]	Indicates that the BAR aperture can be set to 4G.	0x0
17	R/W	Aperture 8G [A8G]	Indicates that the BAR aperture can be set to 8G.	0x0
18	R/W	Aperture 16G [A16G]	Indicates that the BAR aperture can be set to 16G.	0x0
19	R/W	Aperture 32G [A32G]	Indicates that the BAR aperture can be set to 32G.	0x0
20	R/W	Aperture 64G [A64G]	Indicates that the BAR aperture can be set to 64G.	0x0
21	R/W	Aperture 128G [A128G]	Indicates that the BAR aperture can be set to 128G.	0x0
22	R/W	Aperture 256G [A256G]	Indicates that the BAR aperture can be set to 256G.	0x0
23	R/W	Aperture 512G [A512G]	Indicates that the BAR aperture can be set to 512G.	0x0
31:24	R	Reserved [R1]	Reserved	0x0

Resizable BAR Control Register 3 @0x1a0

This register controls the aperture setting of the first memory BAR of the associated Physical Function, and has a field that specifies the number of resizable BARs configurable through the Resizable BAR Capability Structure. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register. When the Resizable BAR Capability is not enabled, a read from this location returns all zeroes. When the Resizable BAR Capability is enabled, all valid fields of this register can be modified from the local management bus.

Table 79: i_resize_BAR_ctrl_3

Bits	SW	Name	Description	Reset
2:0	R/W	BAR Index [BARI]	Specifies the index of the BAR controlled by this register. This field can be modified independently for each PF from the local management bus.	0x0
4:3	R	Reserved [R2]	Reserved	0x0
7:5	R/W	Resizable BAR Count [RBARC]	Specifies the number of BARs that can be configured through the Resizable BAR Capability Structure for this PF. This field can be modified independently for each PF from the local management bus.	0x0

Bits	SW	Name	Description	Reset
12:8	R/W	BAR Size [BARS]	When the Resizable BAR Capability is enabled for the Physical Function, this field controls the BAR aperture for the first BAR of the PF (0 = 1M, 1 = 2M, ..., 12 = 4G). This field can be modified independently for each PF from the local management bus.	0x0
31:13	R	Reserved [R3]	Reserved	0x0

Resizable BAR Capability Register 4 @0x1a4

This register advertises the available aperture settings of the first memory BAR of the associated Physical Function. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability (bit 31) of the associated Physical Function BAR Configuration Register 1. When the Resizable BAR Capability is not enabled, a read from this location returns all zeros. When the Resizable BAR Capability is enabled, any of the bits 4–22 can be modified from the local management bus.

Table 80: i_resize_BAR_cap_4

Bits	SW	Name	Description	Reset
3:0	R	Reserved [R0]	Reserved	0x0
4	R/W	Aperture 1M [A1M]	Indicates that the BAR aperture can be set to 1M.	0x0
5	R/W	Aperture 2M [A2M]	Indicates that the BAR aperture can be set to 2M.	0x0
6	R/W	Aperture 4M [A4M]	Indicates that the BAR aperture can be set to 4M.	0x0
7	R/W	Aperture 8M [A8M]	Indicates that the BAR aperture can be set to 8M.	0x0
8	R/W	Aperture 16M [A16M]	Indicates that the BAR aperture can be set to 16M.	0x0
9	R/W	Aperture 32M [A32M]	Indicates that the BAR aperture can be set to 32M.	0x0
10	R/W	Aperture 64M [A64M]	Indicates that the BAR aperture can be set to 64M.	0x0
11	R/W	Aperture 128M [A128M]	Indicates that the BAR aperture can be set to 128M.	0x0
12	R/W	Aperture 256M [A256M]	Indicates that the BAR aperture can be set to 256M.	0x0
13	R/W	Aperture 512M [A512M]	Indicates that the BAR aperture can be set to 512M.	0x0
14	R/W	Aperture 1G [A1G]	Indicates that the BAR aperture can be set to 1G.	0x0
15	R/W	Aperture 2G [A2G]	Indicates that the BAR aperture can be set to 2G.	0x0
16	R/W	Aperture 4G [A4G]	Indicates that the BAR aperture can be set to 4G.	0x0
17	R/W	Aperture 8G [A8G]	Indicates that the BAR aperture can be set to 8G.	0x0
18	R/W	Aperture 16G [A16G]	Indicates that the BAR aperture can be set to 16G.	0x0
19	R/W	Aperture 32G [A32G]	Indicates that the BAR aperture can be set to 32G.	0x0
20	R/W	Aperture 64G [A64G]	Indicates that the BAR aperture can be set to 64G.	0x0
21	R/W	Aperture 128G [A128G]	Indicates that the BAR aperture can be set to 128G.	0x0
22	R/W	Aperture 256G [A256G]	Indicates that the BAR aperture can be set to 256G.	0x0
23	R/W	Aperture 512G [A512G]	Indicates that the BAR aperture can be set to 512G.	0x0
31:24	R	Reserved [R1]	Reserved	0x0

Resizable BAR Control Register 4 @0x1a8

This register controls the aperture setting of the first memory BAR of the associated Physical Function, and has a field that specifies the number of resizable BARs configurable through the Resizable BAR Capability Structure. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register. When the Resizable BAR Capability is not enabled, a read from this location returns all zeroes. When

the Resizable BAR Capability is enabled, all valid fields of this register can be modified from the local management bus.

Table 81: i_resize_BAR_ctrl_4

Bits	SW	Name	Description	Reset
2:0	R/W	BAR Index [BARI]	Specifies the index of the BAR controlled by this register. This field can be modified independently for each PF from the local management bus.	0x0
4:3	R	Reserved [R2]	Reserved	0x0
7:5	R/W	Resizable BAR Count [RBARC]	Specifies the number of BARs that can be configured through the Resizable BAR Capability Structure for this PF. This field can be modified independently for each PF from the local management bus.	0x0
12:8	R/W	BAR Size [BARS]	When the Resizable BAR Capability is enabled for the Physical Function, this field controls the BAR aperture for the first BAR of the PF (0 = 1M, 1 = 2M, ..., 12 = 4G). This field can be modified independently for each PF from the local management bus.	0x0
31:13	R	Reserved [R3]	Reserved	0x0

Resizable BAR Capability Register 5 @0x1ac

This register advertises the available aperture settings of the first memory BAR of the associated Physical Function. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability (bit 31) of the associated Physical Function BAR Configuration Register 1. When the Resizable BAR Capability is not enabled, a read from this location returns all zeros. When the Resizable BAR Capability is enabled, any of the bits 4–22 can be modified from the local management bus.

Table 82: i_resize_BAR_cap_5

Bits	SW	Name	Description	Reset
3:0	R	Reserved [R0]	Reserved	0x0
4	R/W	Aperture 1M [A1M]	Indicates that the BAR aperture can be set to 1M.	0x0
5	R/W	Aperture 2M [A2M]	Indicates that the BAR aperture can be set to 2M.	0x0
6	R/W	Aperture 4M [A4M]	Indicates that the BAR aperture can be set to 4M.	0x0
7	R/W	Aperture 8M [A8M]	Indicates that the BAR aperture can be set to 8M.	0x0
8	R/W	Aperture 16M [A16M]	Indicates that the BAR aperture can be set to 16M.	0x0
9	R/W	Aperture 32M [A32M]	Indicates that the BAR aperture can be set to 32M.	0x0
10	R/W	Aperture 64M [A64M]	Indicates that the BAR aperture can be set to 64M.	0x0
11	R/W	Aperture 128M [A128M]	Indicates that the BAR aperture can be set to 128M.	0x0
12	R/W	Aperture 256M [A256M]	Indicates that the BAR aperture can be set to 256M.	0x0
13	R/W	Aperture 512M [A512M]	Indicates that the BAR aperture can be set to 512M.	0x0
14	R/W	Aperture 1G [A1G]	Indicates that the BAR aperture can be set to 1G.	0x0
15	R/W	Aperture 2G [A2G]	Indicates that the BAR aperture can be set to 2G.	0x0
16	R/W	Aperture 4G [A4G]	Indicates that the BAR aperture can be set to 4G.	0x0
17	R/W	Aperture 8G [A8G]	Indicates that the BAR aperture can be set to 8G.	0x0
18	R/W	Aperture 16G [A16G]	Indicates that the BAR aperture can be set to 16G.	0x0
19	R/W	Aperture 32G [A32G]	Indicates that the BAR aperture can be set to 32G.	0x0
20	R/W	Aperture 64G [A64G]	Indicates that the BAR aperture can be set to 64G.	0x0
21	R/W	Aperture 128G [A128G]	Indicates that the BAR aperture can be set to 128G.	0x0
22	R/W	Aperture 256G [A256G]	Indicates that the BAR aperture can be set to 256G.	0x0
23	R/W	Aperture 512G [A512G]	Indicates that the BAR aperture can be set to 512G.	0x0

Bits	SW	Name	Description	Reset
31:24	R	Reserved [R1]	Reserved	0x0

Resizable BAR Control Register 5 @0x1b0

This register controls the aperture setting of the first memory BAR of the associated Physical Function, and has a field that specifies the number of resizable BARs configurable through the Resizable BAR Capability Structure. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register. When the Resizable BAR Capability is not enabled, a read from this location returns all zeroes. When the Resizable BAR Capability is enabled, all valid fields of this register can be modified from the local management bus.

Table 83: i_resize_BAR_ctrl_5

Bits	SW	Name	Description	Reset
2:0	R/W	BAR Index [BARI]	Specifies the index of the BAR controlled by this register. This field can be modified independently for each PF from the local management bus.	0x0
4:3	R	Reserved [R2]	Reserved	0x0
7:5	R/W	Resizable BAR Count [RBARC]	Specifies the number of BARs that can be configured through the Resizable BAR Capability Structure for this PF. This field can be modified independently for each PF from the local management bus.	0x0
12:8	R/W	BAR Size [BARS]	When the Resizable BAR Capability is enabled for the Physical Function, this field controls the BAR aperture for the first BAR of the PF (0 = 1M, 1 = 2M, ..., 12 = 4G). This field can be modified independently for each PF from the local management bus.	0x0
31:13	R	Reserved [R3]	Reserved	0x0

Latency Tolerance Reporting (LTR) Extended Capability Header Register @0x1b8

This register contains the PCI Express Extended Capability ID for the Latency Tolerance Reporting (LTR) Capability, its capability version, and the pointer to the next capability structure. This register is implemented only for Physical Function 0. A read from this address of other Physical Functions configuration space returns all zeroes.

Table 84: i_LTR_ext_cap_hdr

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECID]	This field is hardwired to the Capability ID assigned by PCI SIG to the Latency Tolerance Reporting Capability (0018 hex).	0x018
19:16	R	Capability Version [CV]	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus.	0x01
31:20	R	Next Capability Offset [NCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h1c0

LTR Max Snoop/Max No-Snoop Latency Register @0x1bc

This register contains the maximum snoop latency and the maximum no-snoop latency that the device is allowed to request in an LTR message it originates.

Table 85: i_LTR_snoop_lat

Bits	SW	Name	Description	Reset
9:0	R/W	Max Snoop Latency [MSL]	When multiplied by the value of the Max Snoop Latency Scale, this field defines the maximum snoop value the device is permitted to request in an LTR message. This field can be written independently for each Physical Function from the local management bus.	0x0
12:10	R/W	Max Snoop Latency Scale [MSLS]	Specifies the scale value for the Max Snoop Latency. When the setting of this field is non- zero, the actual snoop latency is determined by multiplying the Max Snoop Latency by the following scale factors: • 001: 32 ns • 010: 1024 ns • 011: 32,768 ns • 100: 1,047,576 ns • 101: 33,554,432 ns • 110–111: Reserved	0x0
15:13	R	Reserved [R0]	Reserved	0x0
25:16	R/W	Max No- Snoop Latency [MNSL]	When multiplied by the value of the Max No-Snoop Latency Scale, this field defines the maximum no-snoop value the device is permitted to request in an LTR message. This field can be written independently for each Physical Function from the local management bus.	0x0
28:26	R/W	Max No-Snoop Latency Scale [MNSLS]	Specifies the scale value for the Max No-Snoop Latency. When the setting of this field is non-zero, the actual snoop latency is determined by multiplying the Max No-Snoop Latency by the following scale factors: • 001: 32 ns • 010: 1024 ns • 011: 32,768 ns • 100: 1,047,576 ns • 101: 33,554,432 ns • 110–111: Reserved	0x0
31:29	R	Reserved [R1]	Reserved	0x0

DPA Extended Capability Header Register @0x1c0

This location contains the PCI Express Extended Capability ID for DPA Capability and the offset to the next capability block.

Table 86: i_DPA_ext_cap_header_reg

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECID]	This field is hardwired to the Capability ID assigned by PCI SIG to the Dynamic Power Allocation Reporting Capability.	0x0016
19:16	R	Capability Version [CV]	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus.	0x1
31:20	R	Next Capability Offset [NCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h200

DPA Capability Register @0x1c4

This register contains the DPA capability parameters for the associated Function.

Table 87: i_DPA_cap_reg

Bits	SW	Name	Description	Reset
4:0	R	Maximum Number of Substates [MNS]	Maximum number of DPA substates supported by the Function (the value in this field is the number of substates minus 1).	5'd7
7:5	R	Reserved [R0]	Reserved	0x0
9:8	R	Transition Latency Unit [TLU]	This is the unit of the transition latencies specified in the Transition Latency Value 0 and Transition Latency Value 1 fields of this register (00 = 1 ms, 01 = 10 ms, 10 = 100 ms, 11 = reserved).	0x0
11:10	R	Reserved [R1]	Reserved	0x0
13:12	R	Power Allocation Scale [PAS]	This is the scale used to compute the actual power from the values specified in the Dynamic Power Allocation Array Registers 0 - 7. The actual power in Watts is obtained by multiplying the value in the Dynamic Power Allocation Array Register by this scale factor (00 = 10x, 01 = 1x, 10 = 0.1x, 11 = 0.01x).	0x0
15:14	R	Reserved [R2]	Reserved	0x0
23:16	R	Transition Latency Value 0 [TLV0]	Specifies the transition latency for the substate. Each of the 32 substates may specify one of the two transition latency values. This field contains the first of the two latency values. The unit of latency is specified by the Transition Latency Unit field of this register.	8'h10
31:24	R	Transition Latency Value 1 [TLV1]	Specifies the second of the two transition latency values for the substates. The unit of latency is specified by the Transition Latency Unit field of this register.	8'h8

DPA Latency Indicator Register @0x1c8

This location contains Transition Latency Indicator bits for the DPA substates.

Table 88: i_DPA_lat_indicator_reg

Bits	SW	Name	Description	Reset
31:0	R	Transition Latency Indicator Bits [TLIN]	Bit i of this register indicates the choice of the transition latency value for substate i. A setting of 0 indicates that Transition Latency Value 0 from the DPA Capability Register applies to this substate; a setting of 1 indicates that Transition Latency Value 1 applies.	See Description

DPA Control and Status Registers @0x1cc

This location contains the DPA Control Register and the DPA Status Register.

Table 89: i_DPA_ctrl_status_reg

Bits	SW	Name	Description	Reset
4:0	R	Substate Status [SS]	This field provides the current DPA substate of this Function. This field is writable from the local management bus and must be updated by the local software running on the Endpoint upon completion of a DPA transition to a new substate.	0x0
7:5	R	Reserved [R3]	Reserved	0x0
8	R/WOCLR	Substate Control Enabled [SCE]	This bit enables the Substate Control field. This bit is initialized to 1 by the hardware on a power-on reset or a Function-Level Reset. Software may clear this bit by writing a 1 to this bit position, but cannot set this bit directly through a configuration write. Clearing this bit disables the Substate Control field, thus preventing further substate transitions for this Function. This bit can be set to 0 or 1 through the local management bus by writing a 0 or 1, respectively.	0x1
15:9	R	Reserved [R4]	Reserved	0x0

Bits	SW	Name	Description	Reset
20:16	R/W	Substate Control [SC]	This field is used to initiate a transition of the Function's DPA to a new substate. To initiate the transition, software must write the desired substate value into this field and wait for the transition latency of the substate for the Function to complete the transition. This field can also be written from the local management bus. All substate transitions are disabled when the Substate Control Enabled bit is 0. The Controller generates a one-cycle pulse on the output DPA_INTERRUPT when the value if this field is changed (bit 0 is for PF 0 and so on). This interrupt informs the client of the request from software to change the DPA substate. In response, the client must read the Substate Control field from this register to determine the new substate, and perform the actions necessary to effect the substate change. On completion of the substate change, the client must update the Substate Status field to reflect the new substate the function is in.	0x0
31:21	R	Reserved [R5]	Reserved	0x0

Dynamic Power Allocation Array Register 0 @0x1d0

This is a register in an array of two registers that contain the power allocations for the DPA substates. Each location contains power allocation values for four substates, 8 bits per substate. The value in each 8-bit field, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.

Table 90: i_DPA_power_alloc_reg0

Bits	SW	Name	Description	Reset
7:0	R	Substate Power Allocation 0 [SPA0_0]	This field contains the power allocation for the DPA substate #0 covered by this register. This value, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.	8'h0
15:8	R	Substate Power Allocation 1 [SPA1_0]	This field contains the power allocation for the DPA substate #1 covered by this register. This value, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.	8'h1
23:16	R	Substate Power Allocation 2 [SPA2_0]	This field contains the power allocation for the DPA substate #2 covered by this register. This value, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.	8'h2
31:24	R	Substate Power Allocation 3 [SPA3_0]	This field contains the power allocation for the DPA substate #3 covered by this register. This value, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.	8'h3

Dynamic Power Allocation Array Register 1 @0x1d4

This is a register in an array of two registers that contain the power allocations for the DPA substates. Each location contains power allocation values for four substates, 8 bits per substate. The value in each 8-bit field, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.

Table 91: i_DPA_power_alloc_reg1

Bits	SW	Name	Description	Reset
7:0	R	Substate Power Allocation 4 [SPA0_1]	This field contains the power allocation for the DPA substate #4 covered by this register. This value, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.	8'h4

Bits	SW	Name	Description	Reset
15:8	R	Substate Power Allocation 5 [SPA1_1]	This field contains the power allocation for the DPA substate #5 covered by this register. This value, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.	8'h5
23:16	R	Substate Power Allocation 6 [SPA2_1]	This field contains the power allocation for the DPA substate #6 covered by this register. This value, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.	8'h6
31:24	R	Substate Power Allocation 7 [SPA3_1]	This field contains the power allocation for the DPA substate #7 covered by this register. This value, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.	8'h7

SR-IOV Extended Capability Header Register @0x200

This location contains the PCI Express Extended Capability ID for SR-IOV and the offset to the next capability block.

Table 92: i_SRIOV_ext_cap_header_reg

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECID]	This field is hardwired to the Capability ID assigned by PCI SIG to the SR-IOV Extended Capability Structure (0010 hex).	0x0010
19:16	R	Capability Version [CV]	Specifies the SIG-assigned value for the version of the capability structure. This field is set by default to 1, but can be modified independently for each Function from the local management bus.	0x1
31:20	R	Next Capability Offset [NCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h274

SR-IOV Capabilities Register @0x204

This register defines various capabilities of the SR-IOV implementation.

Table 93: i_SRIOV_cap_reg

Bits	SW	Name	Description	Reset
0	R	VF Migration Capable [VFMC]	Set when the Controller supports VF migration. Hardwired to 0.	0x0
1	R	ARI Capable Hierarchy Preserved [ACHP]	A 1 in this bit position indicates that the ARI Capable Hierarchy bit in the SR-IOV Control Register is preserved across certain power state transitions (see the PCI SIG Single Root I/O Virtualization and Sharing Specifications, Version 1.1, Section 3.3.3.5 for details). This bit is set to 1 by default, but can be modified from the local management bus.	0x1
2	R	VF 10-Bit Tag Requester supported. [VFT10RS]	If set all VFs associated with this PF supports 1-bit requester capability; otherwise, the VF does not. This bit can be disabled using local management register.	0x0
31:3	R	RSVD	RSVD	29'h00000000

SR-IOV Control and Status Registers @0x208

This location contains the SR-IOV Control Register and the SR-IOV Status Register.

Table 94: i_SRIOV_ctrl_status_reg

Bits	SW	Name	Description	Reset
0	R/W	VF Enable [VFE]	This bit must be set to enable the VFs associated with this PF.	0x0
1	R	VF Migration Enable [VFME]	Not supported. Hardwired to 0	0x0
2	R	VF Migration Interrupt Enable [VFMIE]	Not supported. Hardwired to 0	0x0
3	R/W	VF Memory Space Enable [VFMSE]	This bit must be set to allow access to the memory space of the VFs associated with this PF.	0x0
4	R/W	ARI Capable Hierarchy [ARIE]	This bit enables the ARI mode for Virtual Functions. ARI Capable Hierarchy is only present in the lowest numbered PF which is enabled (for example PF0) and affects all PFs of the Device. ARI Capable Hierarchy is Read Only Zero in other PFs of a Device.	0x0
5	R	VF 10-Bit Tag Requester Enable [T10RE]	10-bit TAGs generation are not supported in this configuration.	0x0
15:6	R	Reserved [R15]	Reserved	0x0
31:16	R	SRIOV Status Register [SSR]	Not implemented.	0x0

Initial VFs/Total VFs Register @0x20c

This location contains registers that specify the initial and the total number Virtual Functions (VFs) in the device.

Table 95: i_initial_total_VFs_reg

Bits	SW	Name	Description	Reset
15:0	R	Initial VFs [IVF]	This field contains the initial number of VFs configured for each PF. This field can be modified using local management registers.	0x10
31:16	R	Total VFs [TVF]	This field contains the total number of VFs per PF. Its default setting is identical to that of InitialVFs. This field can be modified using local management registers.	0x10

Function Dependency Link/NumVFs Register @0x210

This location contains the Function Dependency Link that defines VF dependencies and the NumVFs register that stores the number of VFs configured.

Table 96: i_func_dep_link_numVFs_reg

Bits	SW	Name	Description	Reset
15:0	R/W	NumVFs [NVF]	This field must be set by the software to the number of VFs that it wants to enable for each PF. This field can be changed only when the VF Enable bit in the SR-IOV Control Register is 0. Its value should not exceed the setting of TotalVFs for the corresponding Physical Function. This field can also be written from the local management bus.	0x0
31:16	R	Function Dependency Link [FDL]	This field is used to specify dependencies between PFs. It can be modified independently for each Function from the local management bus.	0x0

VF Offset/Stride Register @0x214

Specifies the offset and stride values for VF address assignment.

Table 97: i_VF_offset_stride_reg

Bits	SW	Name	Description	Reset
15:0	R	First VF Offset [FVFO]	Offset of First VF relative to its PF. Modifying this field is not supported.	16'd4
31:16	R	VF Stride [VFS]	Stride value used to assign RIDs for VFs. The stride value is hardwired to 1 for all Physical Functions.	0x1

VF Device ID Register @0x218

This register specifies the VF device id for the device.

Table 98: i_VF_device_id_reg

Bits	SW	Name	Description	Reset
15:0	R	Reserved [R2]	Reserved	0x0
31:16	R	VF Device ID [VFDI]	VF device id assigned to the device. Can be re-written independently for each PF from the local management bus.	0x0100

Supported Page Sizes Register @0x21c

This register specifies all the page sizes supported by the device.

Table 99: i_supported_page_size_reg

Bits	SW	Name	Description	Reset
15:0	R	Page Sizes [PS]	Page sizes supported by the device (one bit for each page size). The Controller implements only bits 15:0 of this register. Can be re-written independently for each PF from the local management bus.	16'h553
31:16	R	Reserved [R0]	Reserved	0x0

System Page Size Register @0x220

This register identifies the page size currently used by the system.

Table 100: i_system_page_size_reg

Bits	SW	Name	Description	Reset
15:0	R/W	System Page Size [SPS]	This field must be programmed by software to the current page size in use. The Controller implements only bits 15:0 of this register. This field can also be written from the local management bus.	0x1
31:16	R	Reserved [R0]	Reserved	0x0

VF Base Address Register 0 @0x224

This is part of the set of six Virtual Function Base Address Registers defined by the SR-IOV Specifications. These registers are used to define address ranges for memory accesses to the Endpoint device. This register may be used to define a range of 32-bit addresses, or paired with the next adjacent register to define a 64-bit address range. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1's into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if this BAR is not configured. Otherwise, the number of 1's returned is based on the length of the BAR.

Table 101: i_VF_BAR_0_reg

Bits	SW	Name	Description	Reset
0	R	Memory Space Indicator [MSI]	Specifies whether this BAR defines a memory address range or an I/O address range (0 = memory, 1 = I/O). The value read in this field is determined by the setting of BAR Configuration Registers of the associated Physical Function.	0x0
1	R	Reserved [R7]	This bit is hardwired to 0 for both memory and I/O BARs.	0x0
2	R	Size [S0]	When the BAR is used to define a memory address range, this field indicates whether the address range is 32-bit or 64-bit (0 = 32-bit, 1 = 64 bit). For 64-bit address ranges, the value in BAR 1 is treated as a continuation of the base address in BAR 0. The value read in this field is determined by the setting of BAR Configuration Registers of the associated Physical Function.	0x1
3	R	Prefetchability [P0]	When the BAR is used to define a memory address range, this field declares whether data from the address range is prefetchable (0 = non-prefetchable, 1 = prefetchable). The value read in this field is determined by the setting of BAR Configuration Registers of the associated Physical Function.	0x0
7:4	R	Reserved [R8]	These bits are hardwired to 0	0x0
21:8	R	Base Address - RO part [BAMR0]	This field defines the base address of the memory address range. The number of implemented bits in this field determines the BAR aperture configured in BAR Configuration Registers of the associated Physical Function. All other bits are not writeable, and are read as 0's.	0x0
31:22	R/W	Base Address - RW part [BAMRW]	This field defines the base address of the memory address range. The number of implemented bits in this field determines the BAR aperture configured in BAR Configuration Registers of the associated Physical Function.	0x0

VF Base Address Register 1 @0x228

This is part of the set of six Virtual Function Base Address Registers defined by the SR-IOV Specifications. These registers are used to define address ranges for memory accesses to the Endpoint device. This register may be used to define a range of 32-bit addresses. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1's into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if this BAR is not configured. Otherwise, the number of 1's returned is based on the length of the BAR.

Table 102: i_VF_BAR_1_reg

Bits	SW	Name	Description	Reset
31:0	R/W	Base Address - RW part [BAMRW]	This field defines the base address of the memory address range. The number of implemented bits in this field determines the BAR aperture setting of BAR Configuration Registers of the associated Physical Function. All other bits are not writeable, and are read as 0's.	0x0

VF Base Address Register 2 @0x22c

This is part of the set of six Virtual Function Base Address Registers defined by the SR-IOV Specifications. These registers are used to define address ranges for memory accesses to the Endpoint device. This register may be used to define a range of 32-bit addresses, or paired with the next adjacent register to define a 64-bit address range. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1's into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if this BAR is not configured. Otherwise, the number of 1's returned is based on the length of the BAR.

Table 103: i_VF_BAR_2_reg

Bits	SW	Name	Description	Reset
31:0	R	Reserved [R7]	This field is reserved at power-on. This can be changed using BAR configuration register in LM space.	0x0

VF Base Address Register 3 @0x230

This is part of the set of six Virtual Function Base Address Registers defined by the SR-IOV Specifications. These registers are used to define address ranges for memory accesses to the Endpoint device. This register may be used to define a range of 32-bit addresses. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1's into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if this BAR is not configured. Otherwise, the number of 1's returned is based on the length of the BAR.

Table 104: i_VF_BAR_3_reg

Bits	SW	Name	Description	Reset
31:0	R	Reserved [R7]	This field is reserved at power-on. This can be changed using BAR configuration register in LM space.	0x0

VF Base Address Register 4 @0x234

This is part of the set of six Virtual Function Base Address Registers defined by the SR-IOV Specifications. These registers are used to define address ranges for memory accesses to the Endpoint device. This register may be used to define a range of 32-bit addresses, or paired with the next adjacent register to define a 64-bit address range. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1's into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if this BAR is not configured. Otherwise, the number of 1's returned is based on the length of the BAR.

Table 105: i_VF_BAR_4_reg

Bits	SW	Name	Description	Reset
31:0	R	Reserved [R7]	This field is reserved at power-on. This can be changed using BAR configuration register in LM space.	0x0

VF Base Address Register 5 @0x238

This is part of the set of six Virtual Function Base Address Registers defined by the SR-IOV Specifications. These registers are used to define address ranges for memory accesses to the Endpoint device. This register may be used to define a range of 32-bit addresses. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1's into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if this BAR is not configured. Otherwise, the number of 1's returned is based on the length of the BAR.

Table 106: i_VF_BAR_5_reg

Bits	SW	Name	Description	Reset
31:0	R	Reserved [R7]	This field is reserved at power-on. This can be changed using BAR configuration register in LM space.	0x0

VF Migration State Array Offset Register Address @0x23c

Not implemented

Table 107: i_VF_migration_state_arr_offset_reg

Bits	SW	Name	Description	Reset
31:0	R	MSAOR	(no description)	0x0

TPH Requester Extended Capability Header Register @0x274

This location contains the PCI Express Extended Capability ID for Transaction Processing Hints (TPH) Requester Capability, its capability version, and the pointer to the next capability block.

Table 108: i_TPH_req_ext_cap_header_reg

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECID]	This field is hardwired to the Capability ID assigned by PCI SIG to the TPH Requester Capability.	0x0017
19:16	R	Capability Version [CV]	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified independently for each PF from the local management bus.	0x1
31:20	R	Next Capability Offset [NCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h300

TPH Requester Capability Register @0x278

This is a read-only register that specifies the capabilities associated with the implementation of the TPH in the device. All the fields in this register, except the reserved ones, can be modified from the local management bus.

Table 109: i_TPH_req_cap_reg

Bits	SW	Name	Description	Reset
0	R	No ST Mode Supported [NSM]	When set to 1, indicates that this Function supports the 'No ST Mode' for the generation of TPH Steering Tags. In the No ST Mode, the device must use a Steering Tag value of 0 for all requests. This bit is hardwired to 1 as all TPH Requesters are required to support the No ST Mode of operation.	0x1
1	R	Interrupt Vector Mode Supported [IVMS]	A setting of 1 indicates that the Function supports the Interrupt Vector Mode for TPH Steering Tag generation. In the Interrupt Vector Mode, Steering Tags are attached to MSI/MSI-X interrupt requests. The Steering Tag for each interrupt request is selected by the MSI/MSI-X interrupt vector number. This bit is set to 1 by default, but can be modified from the local management bus.	0x1

Bits	SW	Name	Description	Reset
2	R	Device- Specific Mode Supported [DSMS]	A setting of 1 indicates that the Function supports the Device- Specific Mode for TPH Steering Tag generation. In this mode, the Steering Tags are supplied by the client for each request through the HAL master interface. The client typically chooses the Steering Tag values from the ST Table, but is not required to do so. This bit is set to 1 by default, but can be modified from the local management bus.	0x1
7:3	R	Reserved [R0]	Reserved	0x0
8	R	Extended TPH Requester Supported [ERS]	When set to 1, indicates that the Function is capable of generating requests with a TPH TLP Prefix.	0x0
10:9	R	ST Table Location [STL]	The setting of this field indicates if a Steering Tag Table is implemented for this Function and its location if present. • 00 = ST Table not present • 01 = ST Table in the TPH Requester Capability Structure • 10 = ST values stored in the MSI-X Table in client RAM • 11 = Reserved This field can be modified from the local management bus.	0x1
15:11	R	Reserved [R1]	Reserved	0x0
26:16	R	ST Table Size [STS]	Specifies the number of entries in the Steering Tag Table (0 = 1 entry, 1 = 2 entries, and so on). Max limit is 64 entries when the ST Table is located in the TPH Requester Capability Structure, and 2048 entries when located in the MSI-X table. Each entry is 16 bits long. This field can be modified from the local management bus.	11'd7
31:27	R	Reserved [R2]	Reserved	0x0

TPH Requester Control Register @0x27c

This register can be used by the software to enable the TPH Requester Capability of the Function and to select the mode of generation of Steering Tags.

Table 110: i_TPH_req_ctrl_reg

Bits	SW	Name	Description	Reset
2:0	R/W	ST Mode [CSM]	This field selects the ST mode (000 = No Steering Tag Mode, 001 = Interrupt Vector Mode, 010 = Device-Specific Mode, other values are reserved). The TPH_ST_MODE output of the Controller reflects the setting of this register field. This field can also be written from the local management bus.	0x0
7:3	R	RSVD	RSVD	5'h00
9:8	R/W	TPH Requester Enable [CRE]	When set , the Function is allowed to generate requests with Transaction Processing Hints. Defined Encodings are: • 00b: Function operating as a Requester is not permitted to issue Requests with TPH or Extended TPH. • 01b: Function operating as a Requester is permitted to issue Requests with TPH and is not permitted to issue Requests with Extended TPH. • 10b: Reserved. • 11b: Function operating as a Requester is permitted to issue Requests with TPH and Extended TPH.	0x00
31:10	R	Reserved [R10]	Reserved	0x0

TPH ST Table @0x280

This table stores the Steering Tags for the TPH Capability. This table has eight entries per Function, each 16 bits long. Two of these entries occupy each 32-bit word of the table. Each of the entries can be read/written through the link (by a Configuration transaction) or through the local management bus.

Table 111: i_TPH_tab_0

Bits	SW	Name	Description	Reset
7:0	R/W	ST Lower 0 [STL0]	Lower 8 bits of the first Steering Tag. This is the 8-bit Steering Tag sent out in requests.	0x0
15:8	R	ST Upper 0 [STU0]	This field is used for the upper 8 bits of the first Steering Tag when Extended TPH Requester support is enabled.	0x0
23:16	R/W	ST Lower 1 [STL1]	Lower 8 bits of the second Steering Tag. This is the 8-bit Steering Tag sent out in requests.	0x0
31:24	R	ST Upper 1 [STU1]	This field is used for the upper 8 bits of the second Steering Tag when Extended TPH Requester support is enabled.	0x0

TPH ST Table @0x284

This table stores the Steering Tags for the TPH Capability. This table has eight entries per Function, each 16 bits long. Two of these entries occupy each 32-bit word of the table. Each of the entries can be read/written through the link (by a Configuration transaction) or through the local management bus.

Table 112: i_TPH_tab_1

Bits	SW	Name	Description	Reset
7:0	R/W	ST Lower 0 [STL0]	Lower 8 bits of the first Steering Tag. This is the 8-bit Steering Tag sent out in requests.	0x0
15:8	R	ST Upper 0 [STU0]	This field is used for the upper 8 bits of the first Steering Tag when Extended TPH Requester support is enabled.	0x0
23:16	R/W	ST Lower 1 [STL1]	Lower 8 bits of the second Steering Tag. This is the 8-bit Steering Tag sent out in requests.	0x0
31:24	R	ST Upper 1 [STU1]	This field is used for the upper 8 bits of the second Steering Tag when Extended TPH Requester support is enabled.	0x0

TPH ST Table @0x288

This table stores the Steering Tags for the TPH Capability. This table has eight entries per Function, each 16 bits long. Two of these entries occupy each 32-bit word of the table. Each of the entries can be read/written through the link (by a Configuration transaction) or through the local management bus.

Table 113: i_TPH_tab_2

Bits	SW	Name	Description	Reset
7:0	R/W	ST Lower 0 [STL0]	Lower 8 bits of the first Steering Tag. This is the 8-bit Steering Tag sent out in requests.	0x0
15:8	R	ST Upper 0 [STU0]	This field is used for the upper 8 bits of the first Steering Tag when Extended TPH Requester support is enabled.	0x0
23:16	R/W	ST Lower 1 [STL1]	Lower 8 bits of the second Steering Tag. This is the 8-bit Steering Tag sent out in requests.	0x0
31:24	R	ST Upper 1 [STU1]	This field is used for the upper 8 bits of the second Steering Tag when Extended TPH Requester support is enabled.	0x0

TPH ST Table @0x28c

This table stores the Steering Tags for the TPH Capability. This table has eight entries per Function, each 16 bits long. Two of these entries occupy each 32-bit word of the table. Each of

the entries can be read/written through the link (by a Configuration transaction) or through the local management bus.

Table 114: i_TPH_tab_3

Bits	SW	Name	Description	Reset
7:0	R/W	ST Lower 0 [STL0]	Lower 8 bits of the first Steering Tag. This is the 8- bit Steering Tag sent out in requests.	0x0
15:8	R	ST Upper 0 [STU0]	This field is used for the upper 8 bits of the first Steering Tag when Extended TPH Requester support is enabled.	0x0
23:16	R/W	ST Lower 1 [STL1]	Lower 8 bits of the second Steering Tag. This is the 8-bit Steering Tag sent out in requests.	0x0
31:24	R	ST Upper 1 [STU1]	This field is used for the upper 8 bits of the second Steering Tag when Extended TPH Requester support is enabled.	0x0

Secondary PCI Express Extended Capability Header Register @0x300

This register contains the PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability, its capability version, and the pointer to the next capability structure. This register is implemented only in the configuration space of PF 0.

Table 115: i_sec_pcie_cap_hdr_reg

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECI]	This field is hardwired to the Capability ID assigned by PCI SIG to the Secondary PCI Express Capability	0x019
19:16	R	Capability Version [CV]	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified independently for each PF from the local management bus.	0x1
31:20	R	Next Capability Offset [NCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h400

Link Control3 Register @0x304

Link Control3 Register.

Table 116: i_link_control3_reg

Bits	SW	Name	Description	Reset
8:0	R	Reserved [R1]	Reserved	0x0
12:9	R/W	Enable Lower SKP OS Generation Vector [ELSOSGV]	When the Link is in L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture.	0x0
31:13	R	Reserved [R2]	Reserved	0x0

Lane Error Status Register @0x308

This register contains one bit per lane indicating the physical-layer error status of the corresponding lane. A 1 indicates that a physical-layer error was detected by the Controller in the corresponding lane. The error can be cleared by writing a 1 into the bit position, either through a Configuration Write transaction from the link or from the local management bus. The following errors are reported in this status bit:

- Parity error detected in Gen3 SKP OS.
- Loss of Block Alignment in the lane.

Table 117: i_lane_error_status_reg

Bits	SW	Name	Description	Reset
3:0	R/ WOCLR	Lane Error Status [LES]	Each of these bits indicates the error status for the corresponding lane. STICKY.	0x0
31:4	R	Reserved [R0]	Reserved.	0x0

Lane Equalization Control Register 0 @0x30c

This register contains the 8.0GT/s Transmitter Preset and the Receiver Preset Hint values for lanes 0 and 1, received from the Upstream Device during the Link Equalization procedure.

Table 118: i_lane_equalization_control_reg0

Bits	SW	Name	Description	Reset
6:0	R	Reserved [R0]	Reserved	0x00
7	R	Reserved [R0_1]	Reserved	0x0
11:8	R	Upstream Port 8.0GT/ s Transmitter Preset [UPTP0]	8.0GT/s Lane 0 Transmitter Preset value received from the upstream device.	0xf
14:12	R	Upstream Port 8.0GT/s Receiver Preset Hint [UPRPH0]	8.0GT/s Lane 0 Receiver Preset Hint value received from the upstream device.	0x7
15	R	Reserved [R1]	Reserved	0x0
22:16	R	Reserved [R2]	Reserved	0x00
23	R	Reserved [R2_1]	Reserved	0x0
27:24	R	Upstream Port 8.0GT/ s Transmitter Preset [UPTP1]	8.0GT/s Lane 1 Transmitter Preset value received from the upstream device.	0xf
30:28	R	Upstream Port 8.0GT/s Receiver Preset Hint [UPRPH1]	8.0GT/s Lane 1 Receiver Preset Hint value received from the upstream device.	0x7
31	R	Reserved [R3]	Reserved	0x0

Lane Equalization Control Register 1 @0x310

This register contains the 8.0GT/s Transmitter Preset and the Receiver Preset Hint values for lanes 2 and 3, received from the Upstream Device during the Link Equalization procedure.

Table 119: i_lane_equalization_control_reg1

Bits	SW	Name	Description	Reset
6:0	R	Reserved [R0]	Reserved	0x00
7	R	Reserved [R0_1]	Reserved	0x0
11:8	R	Upstream Port 8.0GT/s Transmitter Preset [UPTP0]	8.0GT/s Lane 2 Transmitter Preset value received from the upstream device.	0xf
14:12	R	Upstream Port 8.0GT/s Receiver Preset Hint [UPRPH0]	8.0GT/s Lane 2 Receiver Preset Hint value received from the upstream device.	0x7
15	R	Reserved [R1]	Reserved	0x0
22:16	R	Reserved [R2]	Reserved	0x00
23	R	Reserved [R2_1]	Reserved	0x0
27:24	R	Upstream Port 8.0GT/s Transmitter Preset [UPTP1]	8.0GT/s Lane 3 Transmitter Preset value received from the upstream device.	0xf

Bits	SW	Name	Description	Reset
30:28	R	Upstream Port 8.0GT/s Receiver Preset Hint [UPRPH1]	8.0GT/s Lane 3 Receiver Preset Hint value received from the upstream device.	0x7
31	R	Reserved [R3]	Reserved	0x0

Vendor Specific Extended Capability Header @0x400

The Vendor-Specific Capability allows device vendors to use the Capability mechanism for vendor specific information.

Table 120: i_vsec_header_reg

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECI]	This field is hardwired to the Capability ID assigned by PCI SIG to the Vendor-Specific Extended Capability.	0x000B
19:16	R	Capability Version [CV]	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified independently for each PF from the local management bus.	0x1
31:20	R	Next Capability Offset [NCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h440

Vendor Specific Header Register @0x404

Vendor-Specific Header Register.

Table 121: i_vendor_specific_header_reg

Bits	SW	Name	Description	Reset
15:0	R	VSEC ID [VI]	This field contains a vendor defined ID number that indicates the nature and format of the information in the Vendor-Specific Capability Structure. This field can be written from the local management bus independently or each PF.	16'h0001
19:16	R	VSEC Revision [VR]	Vendor-defined version number for the VSEC structure. This field can be written from the local management bus independently or each PF.	4'h1
31:20	R	VSEC Length [VL]	Total byte count (in hex format) of the VSEC structure, including the Vendor-Specific Capability Header, the Vendor-Specific Header and the Vendor-Specific registers. This field can be written from the local management bus independently or each PF.	0x10

Vendor Specific Control Register @0x408

This contains the first four Bytes of Vendor-Specific Register space. In the implementation, the first four Bytes of Vendor Specific Registers is called as Vendor Specific Control Register and is described in the fields below.

Table 122: i_vendor_specific_control_reg

Bits	SW	Name	Description	Reset
7:0	R	VSEC Control In [VSEC_CIN]	The 8-bit value read from this field of PFx reflects the setting of Fx_VSEC_CONTROL_IN [7:0] input to the Controller. This field can also be read from the local management bus	0x0

Bits	SW	Name	Description	Reset
8	R/W	Host-Triggered Interrupt [HTI]	The state of this bit drives the output pins Fx_VSEC_INTERRUPT_OUT (where x is the function number). It can be used by the host to signal a software-driven interrupt to the application logic outside the Controller. This bit may be read and written by the host through a Config transaction, or via the local management interface.	0x0
31:9	R/W	VSEC Control Out [VSEC_COUT]	The state of these bits drive the output pins Fx_VSEC_CONTROL_OUT (where x is the function number). These are implemented as register bits that can be read and written by the host through a Config transaction, or via the local management interface.	0x0

Vendor Specific Data Register 0 @0x40c

This contains the Bytes 4, 5, 6, 7 of Vendor-Specific Register space. In the implementation, these four Bytes of Vendor Specific Registers are called as Vendor Specific Data Register 0 and is described below.

Table 123: i_vendor_specific_data_reg0

Bits	SW	Name	Description	Reset
31:0	R/W	General- Purpose Data [GPD]	These bits are implemented as register bits that can be read and written by the host through a Config transaction, or via the local management interface. Their use is application-dependent.	0x0

PASID Extended Capability Header @0x440

The presence of a PASID Extended Capability indicates that the Endpoint supports sending and receiving TLPs containing a PASID TLP Prefix.

Table 124: i_pasid_header_reg

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECI]	This field is hardwired to the Capability ID assigned by PCI SIG to the PASID Capability.	0x001B
19:16	R	Capability Version [CV]	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified independently for each PF from the local management bus.	0x1
31:20	R	Next Capability Offset [NCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h5c0

PASID Capability Header @0x444

PASID Capability Header fields are described below:

Table 125: i_pasid_cap_reg

Bits	SW	Name	Description	Reset
0	R	Reserved [RSVD1]	These bits are currently reserved. These are implemented as register bits that can be read and written by the host through a Config transaction, or via the local management interface.	0x0
1	R	Execute Permission Supported [EXPS]	If set, the Endpoint supports sending memory requests that have the Execute Requested bit set. If clear, the Endpoint should never set the Execute Requested bit.	0x1

Bits	SW	Name	Description	Reset
2	R	Priveleged Mode Supported [PRMS]	If set, the Endpoint supports operating in Privileged and Non-Privileged modes, and supports sending requests that have the Privileged Mode Requested bit set. If clear, the Endpoint should never set the Privileged Mode Requested bit.	0x1
7:3	R	Reserved [RSVD2]	These bits are currently reserved. These are implemented as register bits that can be read and written by the host through a Config transaction, or via the local management interface.	0x0
12:8	R	Max PASID Width [MPSW]	Indicates the width of the PASID field supported by the Endpoint. The value indicates support for PASID values 0 through 2n-1 (inclusive). The value 0 indicates support for a single PASID (0). The value 20 indicates support for all PASID values (20 bits). This field must be between 0 and 20 (inclusive).	0x14
15:13	R	Reserved [R15]	Reserved	0x0
16	R/W	PASID Enable [PASE]	If set, the Endpoint is permitted to send and receive TLPs that contain a PASID TLP Prefix. If clear, the Endpoint is not permitted to do so.	0x0
17	R/W	Execute Permission Enable [EXPE]	If set, the Endpoint is permitted to send requests that have the Execute Requested bit set. If clear, the Endpoint is not permitted to do so.	0x0
18	R/W	Privileged Mode Enable [PRME]	If set, the Endpoint is permitted to send requests that have the Privileged Mode Requested bit set. If clear, the Endpoint is not permitted to do so.	0x0
31:19	R	Reserved [R31]	Reserved	0x0

ATS Capability Header Register @0x5c0

This location contains the ATS Extended Capabilities Register, its Capability ID, Version, and a pointer to the next capability.

Table 126: ats_cap_header

Bits	SW	Name	Description	Reset
15:0	R	ATS Extended Capability ID [ATSCAPID]	Indicates the ATS Extended Capability structure. This field must return a Capability ID of 000Fh indicating that this is an ATS Extended Capability structure.	0x0F
19:16	R	ats_cap_version_ [ATSCAPVER]	Specifies the SIG assigned value for the version of the capability structure.	0x1
31:20	R	Next Capability Offset [ATSNXTCAP]	Indicates offset to the next PCI Express capability structure.	12'h640

ATS Capability Control Register @0x5c4

ATS Capability and Control Register

Table 127: ats_cap_control

Bits	SW	Name	Description	Reset
4:0	R	ATS Invalidate Queue Depth [ATSINVQD]	The number of Invalidate Requests that the Function can accept before putting backpressure on the upstream connection. If 0 0000b, the Function can accept 32 Invalidate Requests.	0x1
5	R	ATS Page Aligned Req [ATSPGALNREQ]	If Set, indicates the Untranslated Address is always aligned to a 4096 byte boundary.	0x1
6	R	Global invalidate supported [ATSGIS]	If Set, the Function supports InvalidationRequests that have the Global Invalidate bit Set. If Clear, the Function ignores the Global Invalidate bit in all Invalidate Requests.	0x1
15:7	R	Reserved [R15]	Reserved	0x0

Bits	SW	Name	Description	Reset
20:16	R/W	ATS Smallest Translation Unit [ATSSTU]	This value indicates to the Function the minimum number of 4096-byte blocks that is indicated in a Translation Completions or Invalidate Requests. This is a power of 2 multiplier and the number of blocks is 2STU. A value of 0 0000b indicates one block and a value of 1 1111b indicates 2^31 blocks.	0x0
30:21	R	Reserved [R30]	Reserved	0x0
31	R/W	ATS Enable [ATSEN]	When Set, the Function is enabled to cache translations. Default value is 0b.	0x0

ATS Page Request Capability Header Register @0x640

Page Request Extended Capability Structure is used to configure the Page Request Interface mechanism.

Table 128: ats_pr_cap_header

Bits	SW	Name	Description	Reset
15:0	R	Page Request Extended Capability ID [ATSPRCAPID]	Indicates that the associated extended capability structure is a Page Request Extended Capability. This field must return a Capability ID of 0013h.	0x0013
19:16	R	ATS Page Request Capability Version [ATSPRCAPVER]	This field is a PCI SIG defined version number that indicates the version of the Capability structure present.	0x1
31:20	R	ATS PR Next Capability Offset [ATSPRNXCAP]	The offset to the next PCI Extended Capability structure.	12'h900

ATS Page Request Control Status Register @0x644

ATS Page Request Control Status Register.

Table 129: ats_pr_control_status

Bits	SW	Name	Description	Reset
0	R/W	ATS Page Request Enable [ATSPREN]	This field, when set, indicates that the Page Request Interface is allowed to make page requests. If this field is Clear, the Page Request Interface is not allowed to issue page requests. If both this field and the Stopped field are Clear, then the Page Request Interface will not issue new page requests, but has outstanding page requests that have been transmitted or are queued for transmission. When the Page Request Interface is transitioned from not-Enabled to Enabled, its status flags (i.e., Stopped, Response Failure, and Unexpected Response flags) are cleared. Enabling a Page Request Interface that has not successfully Stopped has indeterminate results. Default value is 0b.	0x0
1	W	ATS Page Request Reset [ATSPRRST]	When the Enable field is clear, or is being cleared in the same register update that sets this field, writing a 1b to this field clears the associated implementation dependent page request credit counter and pending request state for the associated Page Request Interface. No action is initiated if this field is written to 0b or if this field is written with any value while the Enable field is Set. Reads of this field through PCIe link return 0b. Once this field is written by '1' through PCIe link, a vector output (ATS_PR_CONTROL_REG_RESET) of controller gets set. Client logic after clearing the credit counter and pending request state, has to clear this register through local management interface.	0x0
15:2	R	RSVD	RSVD	14'h0000

Bits	SW	Name	Description	Reset
16	R/WOCLR	ATS PR Response Failure [ats_pr_rf]	This field, when Set, indicates that the Function has received a PRG Response Message indicating a Response Failure. The Function expects no further responses from the host (any received are ignored). This field is Set by the Function and Cleared when a one is written to the field. For SR-IOV, this field is Set in the PF if any associated Function (PF or VF) receives a PRG Response Message indicating Response Failure. Default value is 0b.	0x0
17	R/WOCLR	ATS Unexpected Page Request Group Index [ATSPPRUPRGI]	This field, when Set, indicates that the Function has received a PRG Response Message containing a PRG index that has no matching request. This field is Set by the Function and cleared when a one is written to the field. For SR-IOV, this field is Set in the PF if any associated Function (PF or VF) receives a PRG Response Message that does has no matching request. Default value is 0b.	0x0
23:18	R	RSVD	RSVD	6'h00
24	R	ATS Page Request Stopped [ATSPRSTOP]	When this field is Set, the associated page request interface has stopped issuing additional page requests and that all previously issued Page Requests have completed. When this field is Clear the associated page request interface either has not stopped or has stopped issuing new Page Requests but has outstanding Page Requests. This field is only meaningful if Enable is Clear. If Enable is Set, this field is undefined. When the Enable field is Cleared, after having been previously Set, the interface transitions to the stopping state and Clears this field. After all page requests currently outstanding at the Function(s) have completed, this field is Set and the interface enters the disabled state. If there were no outstanding page requests, this field may be Set immediately when Enable is Cleared. Resetting the interface will cause an immediate transition to the disabled state. While in the stopping state, receipt of a Response Failure message will result in the immediate transition to the disabled state (Setting this field). For SR-IOV, this field is Set only when all associated Functions (PF and VFs) have stopped issuing page requests. Default value is 1b.	0x1
30:25	R	RSVD	RSVD	6'h00
31	R	PRG Response PASID Required [ATSPRGRPR]	If Set, the Function expects a PASID TLP Prefix on PRG Response Messages when the corresponding Page Requests had a PASID TLP Prefix. If Clear, the Function does not expect PASID TLP Prefixes on any PRG Response Message. Function behavior is undefined if this bit is Clear and the Function receives a PRG Response Message with a PASID TLP Prefix. Function behavior is undefined if this bit is Set and the Function receives a PRG Response Message with no PASID TLP Prefix when the corresponding Page Requests had a PASID TLP Prefix.	0x1

ATS Outstanding Page Request Capacity Register @0x648

This register contains the number of outstanding page request messages the associated Page Request Interface physically supports. This is the upper limit on the number of pages that can be usefully allocated to the Page Request Interface.

Table 130: ats_outstanding_pr_capacity

Bits	SW	Name	Description	Reset
31:0	R	ATS Outstanding Page Request Capacity [ATSOUTPRCAP]	This register contains the number of outstanding page request messages the associated Page Request Interface physically supports. This is the upper limit on the number of pages that can be usefully allocated to the Page Request Interface.	0x1

ATS Outstanding Page Request Allocation @0x64c

This register contains the number of outstanding page request messages the associated Page Request Interface is allowed to issue.

Table 131: ats_outstanding_pr_alloc

Bits	SW	Name	Description	Reset
31:0	R/W	ATS Outstanding Page Request Allocation [ATSOUTPRALLOC]	This register contains the number of outstanding page request messages the associated Page Request Interface is allowed to issue.	0x0

L1 PM Substates Extended Capability Header Register @0x900

L1 PM Substates Extended Capability Header Register. For a multi-Function device associated with an Endpoint implementing L1 PM Substates, this Extended Capability Structure is implemented only in Function 0, and controls the Endpoint's Link behavior on behalf of all the Functions of the device.

Table 132: i_L1_PM_ext_cap_hdr

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECID]	This field is hardwired to the Capability ID assigned by PCI SIG to the L1 PM Substates Extended Capability Structure (001E hex).	0x01e
19:16	R	Capability Version [CV]	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus.	0x01
31:20	R	Next Capability Offset [NCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h910

L1 PM Substates Capabilities Register @0x904

This register advertises the L1 PM Substates Capabilities.

Table 133: i_L1_PM_cap

Bits	SW	Name	Description	Reset
0	R	PML1.2 Supported [L1PML12SUPP]	When Set this bit indicates that PCI-PM L1.2 is supported. This bit can be modified using the local management interface.	0x1
1	R	PML1.1 Supported [L1PML11SUPP]	When Set this bit indicates that PCI-PM L1.1 is supported. This bit can be modified using the local management interface.	0x1
2	R	ASPML1.2 Supported [L1ASPML12SUPP]	When Set this bit indicates that ASPM L1.2 is supported. This bit can be modified using the local management interface.	0x1
3	R	ASPML1.1 Supported [L1ASPML11SUPP]	When Set this bit indicates that ASPM L1.1 is supported. This bit can be modified using the local management interface.	0x1
4	R	L1 PM Substates Supported [L1PMSUPP]	When Set this bit indicates that this Port supports L1 PM Substates. This bit can be modified using the local management interface.	0x1
7:5	R	RSVD	RSVD	3'h0
15:8	R	Port Common Mode Restore Time [L1PrtCmMdReStrTime]	Time (in us) required for this Port to re-establish common mode during exit from PM or ASPM L1.2 substate. This bit can be modified using the local management interface.	8'hff

Bits	SW	Name	Description	Reset
17:16	R	Port Power-On Time Scale [L1PrtPvrOnScale]	Specifies the scale used for the Port T_POWER_ON Value field in the L1 PM Substates Capabilities register. Range of Values: • 00b = 2µs • 01b = 10µs • 10b = 100µs • 11b = Reserved Default value is 00. This bit can be modified using the local management interface.	0x0
18	R	RSVD	RSVD	1'h0
23:19	R	Port Power-On Time Value [R0]	Along with the Port T_POWER_ON Scale field in the L1 PM Substates Capabilities register sets the time (in us) that this Port requires the port on the opposite side of Link to wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. The value of Port T_POWER_ON is calculated by multiplying the value in this field by the scale value in the Port T_POWER_ON Scale field in the L1 PM Substates Capabilities register. T Power On is the minimum amount of time that each component must wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. This is to ensure no device is ever actively driving into an unpowered component. This bit can be modified using the local management interface.	0xd
31:24	R	RSVD	RSVD	8'h00

L1 PM Substates Control 1 Register @0x908

This register is used to Control ASPM, PCI PM L1 substates.

Table 134: i_L1_PM_ctrl_1

Bits	SW	Name	Description	Reset
0	R/W	PML1.2 Enable [L1PML12EN]	When Set this bit enables PCI-PM L1.2.	0x0
1	R/W	PML1.1 Enable [L1PML11EN]	When Set this bit enables PCI-PM L1.1.	0x0
2	R/W	ASPML1.2 Enable [L1ASPML12EN]	When Set this bit enables ASPM L1.2.	0x0
3	R/W	ASPML1.1 Enable [L1ASPML11EN]	When Set this bit enables ASPM L1.1.	0x0
7:4	R	RSVD	RSVD	4'h0
15:8	R	Common Mode Restore Time [L1CmMdReStrTime]	This field is reserved for EP.	0x0
25:16	R/W	LTR L1.2 Threshold Value [L1ThrshldVal]	Along with the LTR_L1.2_THRESHOLD_Scale, this field indicates the LTR threshold used to determine if entry into L1 results in L1.1 (if enabled) or L1.2 (if enabled).	0x0
28:26	R	RSVD	RSVD	3'h0
31:29	R/W	LTR L1.2 Threshold Scale [L1ThrshldSc]	This field provides a scale for the value contained within the LTR_L1.2_THRESHOLD_Value. • 000 - Value times 1 ns • 001 - Value times 32 ns • 010 - Value times 1024 ns • 011 - Value times 32,768 ns • 100 - Value times 1,048,576 ns • 101 - Value times 33,554,422 ns • 110–111 - Not permitted	0x0

L1 PM Substates Control 2 Register @0x90c

L1 PM Substates Control 2 Register

Table 135: i_L1_PM_ctrl_2

Bits	SW	Name	Description	Reset
1:0	R/W	T_POWER_ON Scale [L1PwrOnSc]	Specifies the scale used for T_POWER_ON Value. Range of Values: • 00b = 2µs • 01b = 10µs • 10b = 100µs • 11b = Reserved	0x0
2	R	RSVD	RSVD	1'h0
7:3	R/W	T_POWER_ON Value [L1PwrOnVal]	Along with the T_POWER_ON Scale sets the minimum amount of time (in us) that the Port must wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. T_POWER_ON is calculated by multiplying the value in this field by the value in the T_POWER_ON Scale field.	0x5
31:8	R	RSVD	RSVD	24'h000000

DL Feature Extended Capability Header Register @0x910

Data Link Feature Extended Capability Structure is used to configure the DL Feature mechanism.

Table 136: i_dl_feature_extended_capability_header_reg

Bits	SW	Name	Description	Reset
15:0	R	DL Feature Extended Capability ID [DLFCAPID]	Indicates that the associated extended capability structure is the DL Feature Extended Capability. This field returns a Capability ID of 0025h.	0x0025
19:16	R	DL Feature Capability Version [DLFCAPVER]	This field is a PCI SIG defined version number that indicates the version of the Capability structure present.	0x1
31:20	R	DL Feature Next Capability Offset [DLFNXCAP]	The offset to the next PCI Extended Capability structure.	12'h920

DL Feature Capabilities Register @0x914

Data Link Feature Capabilities Register

Table 137: i_dl_feature_capabilities_reg

Bits	SW	Name	Description	Reset
0	R	Local Scaled Flow Control Supported [DLFCAPVER]	This bit indicates that this Port supports the Scaled Flow Control Feature.	0x1
30:1	R	Reserved [R0]	Reserved	0x0
31	R	DL Feature Exchange Enable [DLFEXEN]	If Set, this bit indicates that this Port will enter the DL_Feature negotiation state prior to Link Initialization.	0x1

DL Feature Status Register @0x918

Data Link Feature Status Register

Table 138: i_dl_feature_status_reg

Bits	SW	Name	Description	Reset
0	R	Remote Scaled Flow Control Supported [RSFSUP]	This bit indicates that the Remote end Device supports the Scaled Flow Control Feature.	0x0
22:1	R	Reserved [R0]	Reserved	0x0
23	R	Reserved [R23]	Reserved	0x0
30:24	R	Reserved [R1]	Reserved	0x0
31	R	Remote Data Link Feature Supported Valid [RDLFSVAL]	This bit indicates that the Port has received a Data Link Feature DLLP in state DL_Feature (see Section 3.2.1), and that the Remote Data Link Feature Supported and Remote Data Link Feature Ack fields are meaningful. This bit is Cleared on entry to state DL_Inactive. Default is 0b.	0x0

Margining Extended Capability Header Register @0x920

Margining Extended Capability Structure is used to configure the device for Receiver Margining.

Table 139: i_margining_extended_capability_header_reg

Bits	SW	Name	Description	Reset
15:0	R	Margining Extended Capability ID [MARCAPID]	Indicates that the associated extended capability structure is the Margining Extended Capability. This field returns a Capability ID of 0027h.	0x0027
19:16	R	Margining Capability Version [MARCAPVER]	This field is a PCI SIG defined version number that indicates the version of the Capability structure present.	0x1
31:20	R	Margining Next Capability Offset [MARNXCAP]	The offset to the next PCI Extended Capability structure.	12'h9c0

Margining Port Capabilities and Status Register @0x924

Margining Port Capabilities and Status Register.

Table 140: i_margining_port_capabilities_status_reg

Bits	SW	Name	Description	Reset
0	R	Margining uses Driver Software [MARUDS]	If Set, indicates that Margining is partially implemented using Device Driver software. Margining Software Ready indicates when this software is initialized. If Clear, Margining does not require device driver software. The Controller implementation requires driver software to initialize the Rx Margining parameter values in Local Management Registers for Lane Margining. Hence, the default value of this bit is set to 1.	0x1
15:1	R	Reserved [R0]	Reserved	0x0
16	R	Margining Ready [MRDY]	Indicates when the Margining feature is ready to accept margining commands. If the Margining uses Driver Software bit is 1, then the Controller sets this status bit when the Margining Software Ready bit is set and the Link is in Gen4 L0 state. If the Margining uses Driver Software bit is 0, then the Controller sets this status bit when the Link is in Gen4 L0 state.	0x0

Bits	SW	Name	Description	Reset
17	R	Margining Software Ready [MSRDY]	When Margining uses Driver Software is Set, then this bit, when Set, indicates that the required software has performed the required initialization. The value of this bit is Undefined if Margining users Driver Software is Clear. The Controller implementation sets the default value of this bit to 0. The driver software must initialize the Rx Margining parameters in the Local Management Lane Margining Registers and then program this bit to 1.	0x0
31:18	R	Reserved [R1]	Reserved	0x0

Margining Lane Control and Status Register for Lane 0 @0x928

Margining Lane Control and Status Register for Lane 0.

Table 141: i_margining_lane_control_status_reg0

Bits	SW	Name	Description	Reset
2:0	R/W	Receiver Number [RCVNUM]	Receiver Number for Margining Commands. This field is reset upon DL Down.	0x0
5:3	R/W	Margin Type [MRGTYP]	Margin Type for Margining Commands. This field is reset upon DL Down.	0x7
6	R/W	Usage Model [USGMOD]	Usage Model for Margining Commands. This field is reset upon DL Down.	0x0
7	R	Reserved [R0]	Reserved	0x0
15:8	R/W	Margin Payload [MRGPAY]	Margin Payload for Margining Commands. This field is reset upon DL Down.	0x9C
18:16	R	Receiver Number Status [RNSTS]	Receiver Number Status for Margining Commands. This field is reset upon DL Down.	0x0
21:19	R	Margin Type Status [MTSTS]	Margin Type Status for Margining Commands. This field is reset upon DL Down.	0x0
22	R	Usage Model Status [UMSTS]	Usage Model Status for Margining Commands. This field is reset upon DL Down.	0x0
23	R	Reserved [R1]	Reserved	0x0
31:24	R	Margin Payload Status [MPSTS]	Margin Payload Status for Margining Commands. This field is reset upon DL Down.	0x0

Margining Lane Control and Status Register for Lane 1 @0x92c

Margining Lane Control and Status Register for Lane 1.

Table 142: i_margining_lane_control_status_reg1

Bits	SW	Name	Description	Reset
2:0	R/W	Receiver Number [RCVNUM]	Receiver Number for Margining Commands. This field is reset upon DL Down.	0x0
5:3	R/W	Margin Type [MRGTYP]	Margin Type for Margining Commands. This field is reset upon DL Down.	0x7
6	R/W	Usage Model [USGMOD]	Usage Model for Margining Commands. This field is reset upon DL Down.	0x0
7	R	Reserved [R0]	Reserved	0x0
15:8	R/W	Margin Payload [MRGPAY]	Margin Payload for Margining Commands. This field is reset upon DL Down.	0x9C

Bits	SW	Name	Description	Reset
18:16	R	Receiver Number Status [RNSTS]	Receiver Number Status for Margining Commands. This field is reset upon DL Down.	0x0
21:19	R	Margin Type Status [MTSTS]	Margin Type Status for Margining Commands. This field is reset upon DL Down.	0x0
22	R	Usage Model Status [UMSTS]	Usage Model Status for Margining Commands. This field is reset upon DL Down.	0x0
23	R	Reserved [R1]	Reserved	0x0
31:24	R	Margin Payload Status [MPSTS]	Margin Payload Status for Margining Commands. This field is reset upon DL Down.	0x0

Margining Lane Control and Status Register for Lane 2 @0x930

Margining Lane Control and Status Register for Lane 2.

Table 143: i_margining_lane_control_status_reg2

Bits	SW	Name	Description	Reset
2:0	R/W	Receiver Number [RCVNUM]	Receiver Number for Margining Commands. This field is reset upon DL Down.	0x0
5:3	R/W	Margin Type [MRGTYP]	Margin Type for Margining Commands. This field is reset upon DL Down.	0x7
6	R/W	Usage Model [USGMOD]	Usage Model for Margining Commands. This field is reset upon DL Down.	0x0
7	R	Reserved [R0]	Reserved	0x0
15:8	R/W	Margin Payload [MRGPAY]	Margin Payload for Margining Commands. This field is reset upon DL Down.	0x9C
18:16	R	Receiver Number Status [RNSTS]	Receiver Number Status for Margining Commands. This field is reset upon DL Down.	0x0
21:19	R	Margin Type Status [MTSTS]	Margin Type Status for Margining Commands. This field is reset upon DL Down.	0x0
22	R	Usage Model Status [UMSTS]	Usage Model Status for Margining Commands. This field is reset upon DL Down.	0x0
23	R	Reserved [R1]	Reserved	0x0
31:24	R	Margin Payload Status [MPSTS]	Margin Payload Status for Margining Commands. This field is reset upon DL Down.	0x0

Margining Lane Control and Status Register for Lane 3 @0x934

Margining Lane Control and Status Register for Lane 3.

Table 144: i_margining_lane_control_status_reg3

Bits	SW	Name	Description	Reset
2:0	R/W	Receiver Number [RCVNUM]	Receiver Number for Margining Commands. This field is reset upon DL Down.	0x0
5:3	R/W	Margin Type [MRGTYP]	Margin Type for Margining Commands. This field is reset upon DL Down.	0x7
6	R/W	Usage Model [USGMOD]	Usage Model for Margining Commands. This field is reset upon DL Down.	0x0

Bits	SW	Name	Description	Reset
7	R	Reserved [R0]	Reserved	0x0
15:8	R/W	Margin Payload [MRGPAY]	Margin Payload for Margining Commands. This field is reset upon DL Down.	0x9C
18:16	R	Receiver Number Status [RNSTS]	Receiver Number Status for Margining Commands. This field is reset upon DL Down.	0x0
21:19	R	Margin Type Status [MTSTS]	Margin Type Status for Margining Commands. This field is reset upon DL Down.	0x0
22	R	Usage Model Status [UMSTS]	Usage Model Status for Margining Commands. This field is reset upon DL Down.	0x0
23	R	Reserved [R1]	Reserved	0x0
31:24	R	Margin Payload Status [MPSTS]	Margin Payload Status for Margining Commands. This field is reset upon DL Down.	0x0

Physical Layer 16 GT/s Extended Capability Header Register @0x9c0

Physical Layer 16 GT/s Extended Capability Structure is used to configure the device for Gen4 Equalization and Gen4 Lane Error Reporting.

Table 145: i_pl_16gts_extended_capability_header_reg

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PL16CAPID]	Indicates that the associated extended capability structure is for Physical layer 16 GT/s. This field returns a Capability ID of 0026h.	0x0026
19:16	R	Capability Version [PL16CAPVER]	This field is a PCI SIG defined version number that indicates the version of the Capability structure present.	0x1
31:20	R	Next Capability Offset [PL16NXCAP]	The offset to the next PCI Extended Capability structure.	12'h0

Physical Layer 16GTs Status Register @0x9cc

Physical Layer 16GTs Status Register.

Table 146: i_pl_16gts_status_reg

Bits	SW	Name	Description	Reset
0	R	Equalization 16.0 GT/s Complete [EQC16]	This bit, when set to 1, indicates that the Transmitter Equalization procedure has completed for 16.0 GT/s. STICKY.	0x0
1	R	Equalization 16.0 GT/ s Phase 1 Successful [EP1S16]	This bit, when set to 1, indicates that the Phase 1 of the Transmitter Equalization procedure has completed successfully for 16.0 GT/s. STICKY.	0x0
2	R	Equalization 16.0 GT/ s Phase 2 Successful [EP2S16]	This bit, when set to 1, indicates that the Phase 2 of the Transmitter Equalization procedure has completed successfully for 16.0 GT/s. STICKY.	0x0
3	R	Equalization 16.0 GT/ s Phase 3 Successful [EP3S16]	This bit, when set to 1, indicates that the Phase 3 of the Transmitter Equalization procedure has completed successfully for 16.0 GT/s. STICKY.	0x0
4	R/WOCLR	Link Equalization Request 16.0 GT/s [LE16]	This bit is Set by Controller hardware to request the 16.0 GT/s Link equalization process to be performed on the Link. Controller hardware sets this bit if a link equalization problem is detected at the end of equalization at 16GT/s. Additionally, the Client Firmware may set this bit while requesting equalization through Local Management EP 16GTs Request Equalization Retrain Link bit. This bit is cleared by writing a 1 to this bit position by the host, or writing a 0 from the LMI. STICKY.	0x0

Bits	SW	Name	Description	Reset
31:5	R	R0	Reserved.	0x0

Physical Layer 16GTs Local Data Parity Mismatch Status Register @0x9d0

Physical Layer 16GTs Local Data Parity Mismatch Status Register.

Table 147: i_pl_16gts_local_data_parity_mismatch_status_reg

Bits	SW	Name	Description	Reset
3:0	R/WOCLR	Local Data Parity Mismatch Status [LDPMS16]	Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number.	0x0
31:4	R	Reserved [R0]	Reserved.	0x0

Physical Layer 16GTs First Retimer Data Parity Mismatch Status Register @0x9d4

Physical Layer 16GTs First Retimer Data Parity Mismatch Status Register.

Table 148: i_pl_16gts_first_retimer_data_parity_mismatch_status_reg

Bits	SW	Name	Description	Reset
3:0	R/WOCLR	First Retimer Data Parity Mismatch Status [FRDPMS16]	Each bit indicates if the first retimer in the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. The value of this field is undefined when no Retimers are present.	0x0
31:4	R	Reserved [R0]	Reserved.	0x0

Physical Layer 16GTs Second Retimer Data Parity Mismatch Status Register @0x9d8

Physical Layer 16GTs Second Retimer Data Parity Mismatch Status Register.

Table 149: i_pl_16gts_second_retimer_data_parity_mismatch_status_reg

Bits	SW	Name	Description	Reset
3:0	R/WOCLR	Second Retimer Data Parity Mismatch Status [SRDPMS16]	Each bit indicates if the second retimer in the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. The value of this field is undefined when no Retimers are present.	0x0
31:4	R	Reserved [R0]	Reserved.	0x0

Physical Layer 16GTs Reserved Register @0x9dc

Register at offset 1Ch in this capability is Reserved.

Table 150: i_pl_16gts_reserved_reg

Bits	SW	Name	Description	Reset
31:0	R	Reserved [R0]	Reserved.	0x0

16 GT/s Lane Equalization Control Register 0 @0x9e0

This register contains the Upstream Port 16.0GT/s Transmitter Preset for lanes 0, 1, 2, and 3, received from the Downstream Port during the 16GT/s Link Equalization procedure.

Table 151: i_pl_16gts_lane_equalization_control_reg0

Bits	SW	Name	Description	Reset
3:0	R	Reserved [R0]	Reserved	0x0
7:4	R	Lane 0 Upstream Port 16.0GT/s Transmitter Preset [UPTP016]	16.0GT/s Lane 0 Transmitter Preset value received from the downstream port during 16GT/s Link Equalization.	0xf
11:8	R	Reserved [R8]	Reserved	0x0
15:12	R	Lane 1 Upstream Port 16.0GT/s Transmitter Preset [UPTP116]	16.0GT/s Lane 1 Transmitter Preset value received from the upstream device.	0xf
19:16	R	Reserved [R16]	Reserved	0x0
23:20	R	Lane 2 Upstream Port 16.0GT/s Transmitter Preset [UPTP216]	16.0GT/s Lane 2 Transmitter Preset value received from the upstream device.	0xf
27:24	R	Reserved [R24]	Reserved	0x0
31:28	R	Lane 3 Upstream Port 16.0GT/s Transmitter Preset [UPTP316]	16.0GT/s Lane 3 Transmitter Preset value received from the upstream device.	0xf

Virtual Function Configuration Register Set

This version of the core supports a total of 64 Virtual Functions, which may be assigned among the four Physical Functions. The VFs occupy the address range 64–127 in the Function address space. The core automatically sets the offset and stride values for each Physical Functions based on the setting of the VF mode. The following sections describe the registers in detail below.

Vendor ID and Device ID @0x0

Hardwired to all 1s.

Table 152: i_vendor_id_device_id

Bits	SW	Name	Description	Reset
15:0	R	Vendor ID [VID]	A read to this register returns FFFFh for VFs.	0xffff
31:16	R	Device ID [DID]	Device ID assigned by the manufacturer of the device. This field can be written independently for each Function from the local management bus.	0xffff

Command and Status Register @0x4

This location contains the 16-bit Command Register and the 16-bit Status Register defined in PCI Specifications 3.0.

Table 153: i_command_status

Bits	SW	Name	Description	Reset
0	R	I/O-Space Enable [IOSE]	Reserved	0x0
1	R	Mem-Space Enable [MSE]	Reserved	0x0
2	R/W	Bus-Master Enable [BME]	Enables the device to issue memory requests from this Function. This field can be written from the local management bus.	0x0
5:3	R	Reserved [R0]	Reserved	0x0
6	R	Parity Error Response Enable [PERE]	Reserved	0x0
7	R	Reserved [R1]	Reserved	0x0
8	R	SERR Enable [SE]	Reserved	0x0
9	R	Reserved [R2]	Reserved	0x0
10	R	INTx Message Disable [IMD]	Reserved	0x0
18:11	R	Reserved [R3]	Reserved	0x0
19	R	Interrupt Status [IS]	Reserved	0x0
20	R	Capabilities List [CL]	Indicates the presence of PCI Extended Capabilities registers. This bit is hardwired to 1.	0x1
23:21	R	Reserved [R4]	Reserved	0x0

Bits	SW	Name	Description	Reset
24	R/WOCLR	Master Data Parity Error [MDPE]	When the Parity Error Response enable bit in the PCI Command Register of the associated Physical Function is set, the core sets this bit when it detects the following error conditions: **1.** The core receives a Poisoned Completion TLP from the link in response to a request from this VF. **2.** The core sends out a poisoned write request on the link from this VF. (This bit remains 0 when the Parity Error Response enable bit in the PCI Command Register of the associated Physical Function is 0). This field can also be cleared from the local management bus by writing a 1 into this bit position. STICKY.	0x0
26:25	R	Reserved [R5]	Reserved	0x0
27	R/WOCLR	Signaled Target Abort [STA]	This bit is set when the core has sent a completion from this VF to the link with the Completer Abort status. This field can also be cleared from the local management bus by writing a 1 into this bit position. STICKY.	0x0
28	R/WOCLR	Received Target Abort [RTA]	This bit is set when this Virtual Function has received a completion from the link with the Completer Abort status. This field can also be cleared from the local management bus by writing a 1 into this bit position. STICKY.	0x0
29	R/WOCLR	Received Master Abort [RMA]	This bit is set when this VF has received a completion from the link with the Unsupported Request status. This field can also be cleared from the local management bus by writing a 1 into this bit position. STICKY.	0x0
30	R/WOCLR	Signaled System Error [SSE]	If the SERR enable bit in the PCI Command Register of the associated Physical Function is 1, this bit is set when this VF has sent out a fatal or non-fatal error message on the link to the Root Complex. If the SERR enable bit is 0, this bit remains 0. This field can also be cleared from the local management bus by writing a 1 into this bit position. STICKY.	0x0
31	R/WOCLR	Detected Parity Error [DPE]	This bit is set when the core has received a Poisoned TLP targeted at this VF. The Parity Error Response enable bit (bit 6) in the PCI Command Register of the associated PF has no effect on the setting of this bit. STICKY.	0x0

Revision ID and Class Code Register @0x8

This register contains the Revision ID and Class Code associated with the device incorporating the PCIe core.

Table 154: i_revision_id_class_code

Bits	SW	Name	Description	Reset
7:0	R	Revision ID [RID]	Assigned by the manufacturer of the device to identify the revision RO setting of this field. This field reflects the setting of the corresponding register in the configuration space of the associated Physical Function.	8'h0
15:8	R	Programming Interface Byte [PIB]	Identifies the register set layout of the device. This field reflects the setting of the corresponding register in the configuration space of the associated Physical Function.	0x0
23:16	R	Sub-Class Code [SCC]	Identifies a sub-category within the selected function. This field reflects the setting of the corresponding register in the configuration space of the associated Physical Function.	8'h0
31:24	R	Class Code [CC]	Identifies the function of the device. This field reflects the setting of the corresponding register in the configuration space of the associated Physical Function.	8'h0

BIST, Header Type, Latency Timer and Cache Line Size Registers @0xc

This location contains the BIST, header-type, Latency Timer and Cache Line Size Registers.

Table 155: i_bist_header_latency_cache_line

Bits	SW	Name	Description	Reset
7:0	R	Cache Line Size [CLS]	Reserved	0x0
15:8	R	Latency Timer [LT]	Reserved	0x0
22:16	R	Header Type [HT]	Reserved	0x0
23	R	Device Type [DT]	Identifies whether the device supports a single Function or multiple Functions. This bit is read as 0 when only Function 0 has been enabled in the Physical Function Configuration Register (in the local management block). Reserved for VFs.	0x0
31:24	R	BIST Register [BR]	Reserved	0x0

Base Address Register 0 @0x10

Not Implemented

Table 156: i_bar_0_reg

Bits	SW	Name	Description	Reset
31:0	R	Not Implemented [NI]	(no description)	0x0

Base Address Register 1 @0x14

Not Implemented

Table 157: i_bar_1_reg

Bits	SW	Name	Description	Reset
31:0	R	Not Implemented [NI]	(no description)	0x0

Base Address Register 2 @0x18

Not Implemented

Table 158: i_bar_2_reg

Bits	SW	Name	Description	Reset
31:0	R	Not Implemented [NI]	(no description)	0x0

Base Address Register 3 @0x1c

Not Implemented

Table 159: i_bar_3_reg

Bits	SW	Name	Description	Reset
31:0	R	Not Implemented [NI]	(no description)	0x0

Base Address Register 4 @0x20

Not Implemented

Table 160: i_bar_4_reg

Bits	SW	Name	Description	Reset
31:0	R	Not Implemented [NI]	(no description)	0x0

Base Address Register 5 @0x24

Not Implemented

Table 161: i_bar_5_reg

Bits	SW	Name	Description	Reset
31:0	R	Not Implemented [NI]	(no description)	0x0

Subsystem Vendor ID and Subsystem ID Register @0x2c

This register contains the Subsystem Vendor ID and Subsystem ID associated with the device incorporating the PCIe core.

Bits	SW	Name	Description	Reset
15:0	R	Subsystem Vendor ID [SVID]	Specifies the Subsystem Vendor ID assigned by the PCI SIG to the manufacturer of the device. Its value comes from the Subsystem Vendor ID Register in the local management register block.	16'h17cd
31:16	R	Subsystem ID [SID]	Specifies the Subsystem ID assigned by the manufacturer of the device. This field reflects the setting of the corresponding register in the configuration space of the associated Physical Function.	16'h0

Expansion ROM Base Address Register @0x30

Not Implemented

Table 162: i_expansn_rom_bar_reg

Bits	SW	Name	Description	Reset
31:0	R	Not Implemented [NI]	(no description)	0x0

Capabilities Pointer @0x34

This location contains the pointer to the first PCI Capability Structure.

Table 163: i_capabilities_pointer

Bits	SW	Name	Description	Reset
7:0	R	Capabilities Pointer [CP]	Contains pointer to the first PCI Capability Structure. This field is set by default to point to the Power Management Capability Structure. It can be modified by writing to VF 0 from the local management bus, and the setting is common across all VFs.	0x80
31:8	R	Reserved [R6]	Reserved	0x0

Reserved @0x40 + [0..15 * 0x4]

Reserved

Table 164: rsvd_010_01F

Bits	SW	Name	Description	Reset
31:0	R	Reserved [RSVD]	Reserved	0x0

Interrupt Line and Interrupt Pin Register @0x3c

Not Implemented

Table 165: i_intrpt_line_intrpt_pin_reg

Bits	SW	Name	Description	Reset
31:0	R	Not Implemented [NI]	(no description)	0x0

Power Management Capabilities Register @0x80

This location contains the Power Management Capabilities Register, its Capability ID, and a pointer to the next capability. This version of the core supports the PCI power states D0 ,D1 and D3.

Table 166: i_pwr_mgmt_cap

Bits	SW	Name	Description	Reset
7:0	R	Capability ID [CID]	Identifies that the capability structure is for Power Management. This field is set by default to 01 hex. It can be re-written independently for each Function from the local management bus.	0x01
15:8	R	Capabilities Pointer [CP]	Contains pointer to the next PCI Capability Structure. By default, this points to the MSI Capability Structure. This field can be re-written independently for each Function from the local management bus.	8'h90
18:16	R	Version ID [VID]	Indicates the version of the PCI Bus Power Management Specifications that the Function implements. This field is set by default to 011 (Version 1.2). It can be re-written independently for each Function from the local management bus.	0x03
19	R	PME Clock [PC]	Not applicable to PCI Express. This bit is hardwired to 0.	0x0
20	R	Reserved [R0]	Reserved	0x0

Bits	SW	Name	Description	Reset
21	R	Device Specific Initialization Bit [DSI]	This bit, when set, indicates that the device requires additional configuration steps beyond setting up its PCI configuration space, to bring it to the D0active state from the D0uninitialized state. This bit is hardwired to 0.	0x0
24:22	R	Max Current Required from Aux Power Supply [MCRAPS]	Specifies the maximum current drawn by the device from the aux power source in the D3cold state. This field is not implemented in devices not supporting PME notification when in the D3cold state, and is therefore hardwired to 0.	0x0
25	R	D1 Support [D1S]	Set if the Function supports the D1 power state. This bit can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.	0x1
26	R	D2 Support [D2S]	Set if the Function supports the D2 power state. Currently hardwired to 0.	0x0
27	R	PME Support for D0 State [PSD0S]	Indicates whether the Function is capable of sending PME messages when in the D0 state. This bit is set to 1 by default, but can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.	0x01
28	R	PME Support for D1 State [PSD1S]	Indicates whether the Function is capable of sending PME messages when in the D1 state. This bit is set to 1 by default, but can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.	0x1
29	R	PME Support for D2 State [PSD2S]	Indicates whether the Function is capable of sending PME messages when in the D2 state. This bit is hardwired to 0 because D2 state is not supported.	0x0
30	R	PME Support for D3(hot) State [PSDHS]	Indicates whether the Function is capable of sending PME messages when in the D3hot state. This bit is set to 1 by default, but can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.	0x01
31	R	PME Support for D3(cold) State [PSDCS]	Indicates whether the Function is capable of sending PME messages when in the D3cold state. Because the device does not have aux power, this bit is hardwired to 0.	0x0

Power Management Control/Status Report @0x84

This location contains the 16-bit Power Management Control/Status Register.

Table 167: i_pwr_mgmt_ctrl_stat_rep

Bits	SW	Name	Description	Reset
1:0	R/W	Power State [PS]	Indicates the power state this Function is currently in. This field can be read by the software to monitor the current power state, or can be written to cause a transition to a new state. The valid settings are 00 (state D0), 01 (state D1) and 11 (state D3hot). The software should not write any other value into this field. This field can also be written from the local management bus independently for each VF Function.	0x0
2	R	Reserved [R4]	Reserved	0x0
3	R	No Soft Reset [NSR]	When this bit is set to 1, the Function will maintain all its state in the PM state D3hot. The software is not required to re-initialize the Function registers on the transition back to D0. This bit is set to 1 by default, but can be modified independently for each VF from the local management bus.	0x01
7:4	R	Reserved [R3]	Reserved	0x0
8	R/W	PME Enable [PE]	Setting this bit enables the notification of PME events from the associated Function. This bit can be set also by writing into this register from the local management bus.	0x0

Bits	SW	Name	Description	Reset
14:9	R	Reserved [R2]	Reserved	0x0
15	R/WOCLR	PME Status [PMES]	When PME notification is enabled, writing a 1 into this bit position from the local management bus sets this bit and causes the core to send a PME message from the associated Function. When the Root Complex processes this message, it will turn off this bit by writing a 1 into this bit position though a Config Write. This bit can be set or cleared from the local management bus, by writing a 1 or 0, respectively. It can only be cleared from the configuration path (by writing a 1).	0x0
23:16	R	Reserved [R1]	Reserved	0x0
31:24	R	Data Register [DR]	This optional register is not implemented in the PCIe core. This field is hardwired to 0.	0x0

Reserved @0x88 + [0..1 * 0x4]

Reserved

Table 168: rsvd_022_023

Bits	SW	Name	Description	Reset
31:0	R	Reserved [RSVD]	Reserved	0x0

MSI Control Register @0x90

This register is used only when the core is configured to support Message Signaled Interrupts (MSIs). In addition to the MSI control bits, this location also contains the MSI Capability ID and the pointer to the next PCI Capability Structure.

Table 169: i_msi_ctrl_reg

Bits	SW	Name	Description	Reset
7:0	R	Capability ID [CID]	Specifies that the capability structure is for MSI. Hardwired to 05 hex.	0x05
15:8	R	Capabilities Pointer [CP]	Pointer to the next PCI Capability Structure. The value read from this read-only field is the corresponding pointer in the MSI Capability Structure of the Physical Function this VF is attached to. The setting is common across all the Virtual Functions.	8'hb0
16	R/W	MSI Enable [ME]	Set by the configuration program to enable the MSI feature. This field can also be written from the local management bus.	0x0
19:17	R	Multiple Message Capable [MMC]	Encodes the number of distinct messages that the core is capable of generating for this Function (000 = 1, 001 = 2, 010 = 4, 011 = 8, 100 = 16, 101 = 32). Thus, this field defines the number of the interrupt vectors for this Function. The core allows up to 32 distinct messages, but the setting of this field must be based on the number of interrupt inputs of the core that are actually used by the client. For example, if the client logic uses eight of the 32 distinct MSI interrupt inputs of the core for this Function, then the value of this field must be set to 011. This field can be written from the local management bus.	0x0
22:20	R/W	Multiple Message Enable [MME]	Encodes the number of distinct messages that the core is programmed to generate for this Function (000 = 1, 001 = 2, 010 = 4, 011 = 8, 100 = 16, 101 = 32). This setting must be based on the number of interrupt inputs of the core that are actually used by this Function. This field can be written from the local management bus.	0x0
23	R	64-Bit Address Capable [AC64]	Set to 1 to indicate that the device is capable of generating 64-bit addresses for MSI messages.	0x1
24	R	MSI masking capable [MC]	Can be modified using localmanagement interface	0x1
31:25	R	Reserved [R0]	Reserved	0x0

MSI Message Low Address Register @0x94

This register contains the first 32 bits of the address to be used in the MSI messages generated by the core for this Function. This address is taken as a 32-bit address if the value programmed in the MSI Message High Address Register is 0. Otherwise, this address is taken as the least significant 32 bits of the 64-bit address sent in MSI messages.

Table 170: i_msi_msg_low_addr

Bits	SW	Name	Description	Reset
1:0	R	Reserved [R1]	The two lower bits of the address are hardwired to 0 to align the address on a double-word boundary.	0x0
31:2	R/W	Message Address Low [MAL]	Lower bits of the address to be used in MSI messages. This field can also be written from the local management bus.	0x0

MSI Message High Address Register @0x98

This register contains the 32 most significant bits of the 64-bit address sent by the core in MSI messages. A value of all zeroes in thei register is taken to mean that the core should use 32-bit addresses in the messages.

Table 171: i_msi_msg_hi_addr

Bits	SW	Name	Description	Reset
31:0	R/W	Message Address High [MAH]	Contains bits 63:32 of the 64-bit address to be used in MSI Messages. A value of 0 specifies that 32-bit addresses are to be used in the messages. This field can also be written from the local management bus.	0x0

MSI Message Data Register @0x9c

This register contains the write data to be used in the MSI messages to be generated for the associated PCI Function. When the number of distinct messages programmed in the MSI Control Register is 1, the 32-bit value from this register is used as the data value in the MSI packets generated by the core for this Function. If the number of distinct messages is more than 1, the least significant bits of the programmed value are replaced with the encoded interrupt vector [31:0] of the specific message to generate the write data value for the message.

Table 172: i_msi_msg_data

Bits	SW	Name	Description	Reset
15:0	R/W	Message Data [MD]	Message data to be used for this Function. This field can also be written from the local management bus.	0x0
31:16	R	Reserved [R2]	Hardwired to 0.	0x0

MSI Mask Register @0xa0

This register contains the MSI mask bits, one for each of the interrupt levels.

Table 173: i_msi_mask

Bits	SW	Name	Description	Reset
0	R/W	MSI Mask [MM]	Mask bits for MSI interrupts. The Multiple Message Capable field of the MSI Control Register specifies the number of distinct interrupts for the Function, which determines the number of valid mask bits. Please note that if the Multiple Message Capable field is changed from the local management APBbus then the width of the MSI Mask field also changes correspondingly	0x0
31:1	R	Reserved [R0]	Please note that if the Multiple Message Capable field is changed from the local management APBbus then the width of this field also changes correspondingly	0x0

MSI Pending Bits Register @0xa4

This register contains the MSI pending interrupt bits, one for each of the interrupt levels. This field can be written from the local management APBbus.

Table 174: i_msi_pending_bits

Bits	SW	Name	Description	Reset
0	R	MSI Pending Bits [MP]	Pending bits for MSI interrupts. This register contains the MSI pending interrupt bits, one for each of the interrupt levels. This field can be written from the local management APBbus. The Multiple Message Capable field of the MSI Control Register specifies the number of distinct interrupts for the Function, which determines the number of valid pending bits. Please note that if the Multiple Message Capable field is changed from the local management APBbus then the width of the MSI Pending Bits field also changes accordingly.	0x0
31:1	R	Reserved [R0]	Please note that if the Multiple Message Capable field is changed from the local management APBbus then the width of this field also changes accordingly.	0x0

MSI-X Control Register @0xb0

This register contains the MSI-X configuration bits, the Capability ID for MSI-X, and the pointer to the next PCI Capability structure.

Table 175: i_msix_ctrl

Bits	SW	Name	Description	Reset
7:0	R	Capability ID [CID]	Identifies that the capability structure is for MSI-X. This field is set by default to 11 hex. It can be re-written independently for each Function from the local management bus.	0x11
15:8	R	Capabilities Pointer [CP]	Contains a pointer to the next PCI Capability Structure. The value read from this read-only field is the corresponding pointer in the MSI-X Capability Structure of the Physical Function this VF is attached to.	8'hc0
26:16	R	MSI-X Table Size [MSIXTS]	Specifies the size of the MSI-X Table, that is, the number of interrupt vectors defined for the Function. The programmed value is 1 minus the size of the table (that is, this field is set to 0 if the table size is 1). It can be re-written independently for each Function from the local management bus.	11'h0
29:27	R	Reserved [R0]	Reserved	0x0
30	R/W	Function Mask [FM]	This bit serves as a global mask to all the interrupt conditions associated with this Function. When this bit is set, the core will not send out MSI messages from this Function. This field can also be written from the local management bus.	0x0
31	R/W	MSI-X Enable [MSIXE]	Set by the configuration program to enable the MSI-X feature. This field can also be written from the local management bus.	0x0

MSI-X Table Offset Register @0xb4

This register is used to specify the location of the MSI-X Table in memory. All of the 32 bits of this register can be re-written independently for each Virtual Function from the local management bus.

Table 176: i_msix_tbl_offset

Bits	SW	Name	Description	Reset
2:0	R	BAR Indicator Register [BARI]	Identifies the BAR corresponding to the memory address range where the MSI-X Table is located (000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5).	3'd0
31:3	R	Table Offset [TO]	Offset of the memory address where the MSI- X Table is located, relative to the selected BAR. The three least significant bits of the address are omitted as the addresses are QWORD aligned.	29'h0

MSI-X Pending Interrupt Register @0xb8

This register is used to specify the location of the MSI-X Pending Bit Array (PBA). The PBA is a structure in memory containing the pending interrupt bits. All the 32 bits of this register can be re-written independently for each Virtual Function from the local management bus.

Table 177: i_msix_pending_intrpt

Bits	SW	Name	Description	Reset
2:0	R	BAR Indicator Register [BARI]	Identifies the BAR corresponding to the memory address range where the PBA Structure is located (000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5). The value programmed must be the same as the BAR Indicator configured in the MSI-X Table Offset Register. Identifies the BAR corresponding to the memory address range where the PBA Structure is located (000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5). The value programmed must be the same as the BAR Indicator configured in the MSI-X Table Offset Register.	3'd0
31:3	R	PBA Offset [PO]	Offset of the memory address where the PBA is located, relative to the selected BAR. The three least significant bits of the address are omitted as the addresses are QWORD aligned.	29'h1

PCI Express Capability List Register @0xc0

This location identifies the PCI Express device type and its capabilities. It also contains the Capability ID for the PCI Express Structure and the pointer to the next capability structure.

Table 178: i_pcie_cap_list

Bits	SW	Name	Description	Reset
7:0	R	Capability ID [CID]	Specifies Capability ID assigned by PCI SIG for this structure. This field is hardwired to 10 hex.	0x010
15:8	R	Next Capability Pointer [NCP]	Points to the next PCI capability structure. Set to 0 because this is the last capability structure.	0x0
19:16	R	Capability Version [CV]	Identifies the version number of the capability structure. This field is set to 2 by default to indicate that the Controller is compatible to PCI Express Base Specification Revision 3.0.	0x02
23:20	R	Device Type [DT]	Indicates the type of device implementing this Function. This field is hardwired to 0 in the EP mode.	0x0
24	R	Slot Status [SS]	Set to 1 when the link connected to a slot. Hardwired to 0.	0x0

Bits	SW	Name	Description	Reset
29:25	R	Interrupt Message Number [IMN]	Identifies the MSI or MSI-X interrupt vector for the interrupt message generated corresponding to the status bits in the Slot Status Register, Root Status Register, or this capability structure. This field must be defined based on the chosen interrupt mode - MSI or MSI-X. This field is hardwired to 0.	0x0
30	R	TCS Routing Supported [TRS]	When set to 1, this bit indicates that the device supports routing of Trusted Configuration Requests. Not valid for Endpoints. Hardwired to 0.	0x0
31	R	Reserved [R0]	Reserved	0x0

PCI Express Device Capabilities Register @0xc4

This register advertises the capabilities of the PCI Express device encompassing this Function.

Table 179: i_pcie_dev_cap

Bits	SW	Name	Description	Reset
2:0	R	Max Payload Size [MPS]	Specifies maximum payload size supported by the device. This field reflects the setting of the corresponding field in the PCIe Device Capability Register of PF 0.	3'b011
4:3	R	Phantom Functions Supported [PFS]	This field is used to extend the tag field by combining unused Function bits with the tag bits. This field is hardwired to 00 to disable this feature.	0x0
5	R	Extended Tag Field Supported [ETFS]	Set when device allows the tag field to be extended from 5 to 8 bits. This field reflects the setting of the corresponding field in the PCIe Device Capability Register of PF 0.	0x1
8:6	R	Acceptable L0S Latency [AL0SL]	Specifies acceptable latency that the Endpoint can tolerate while transitioning from L0S to L0. This field reflects the setting of the corresponding field in the PCIe Device Capability Register of PF 0.	0x4
11:9	R	Acceptable L1 Latency [AL1SL]	Specifies acceptable latency that the Endpoint can tolerate while transitioning from L1 to L0. This field reflects the setting of the corresponding field in the PCIe Device Capability Register of PF 0.	0x0
14:12	R	Reserved [R1]	Reserved	0x0
15	R	Role-Based Error Reporting [RBER]	This field reflects the setting of the corresponding field in the PCIe Device Capability Register of PF 0.	0x01
17:16	R	Reserved [R2]	Reserved	0x0
25:18	R	Captured Slot Power Limit Value [CSPLV]	This field reflects the setting of the corresponding field in the PCIe Device Capability Register of PF 0.	0x0
27:26	R	Captured Power Limit Scale [CPLS]	This field reflects the setting of the corresponding field in the PCIe Device Capability Register of PF 0.	0x0
28	R	FLR Capable [FLRC]	Set when device has Function-Level Reset capability. Hardwired to 1.	0x01
31:29	R	Reserved [R3]	Reserved	0x0

PCI Express Device Control and Status Register @0xc8

This register contains control and status bits associated with the device implementing this Function. All the read-write bits in this register can also be written from the local management bus. Likewise, bits designated as RW1C can also be cleared by writing a 1 from the local management bus.

Table 180: i_pcie_dev_ctrl_status

Bits	SW	Name	Description	Reset
0	R	Enable Correctable Error Reporting [ECER]	Reserved	0x0
1	R	Enable Non- Fatal Error Reporting [ENFER]	Reserved	0x0
2	R	Enable Fatal Error Reporting [EFER]	Reserved	0x0
3	R	Enable Unsupported Request Reporting [EURR]	Reserved	0x0
4	R	Enable Relaxed Ordering [ERO]	Reserved	0x0
7:5	R	Max Payload Size [MPS]	Reserved	0x0
8	R	Extended Tag Field Enable [ETFE]	Reserved	0x0
9	R	Enable Phantom Functions [EPF]	Reserved	0x0
10	R	Enable Aux Power [EAP]	Reserved	0x0
11	R	Enable No Snoop [EBS]	Reserved	0x0
14:12	R	Max Read Request Size [MRRS]	Reserved	0x0
15	R/W	Function-Level Reset [FLR]	Writing a 1 into this bit position generated a Function-Level Reset for the selected VF. This bit reads as 0.	0x0
16	R/WOCLR	Correctable Error Detected [CED]	Set to 1 by the core when it detects a correctable error, regardless of whether error reporting is enabled or not, and regardless of whether the error is masked	0x0
17	R/WOCLR	Non-Fatal Error Detected [NFER]	Set to 1 by the core when it detects a non-fatal error, regardless of whether error reporting is enabled or not, and regardless of whether the error is masked.	0x0
18	R/WOCLR	Fatal Error Detected [FED]	Set to 1 by the core when it detects a fatal error, regardless of whether error reporting is enabled or not, and regardless of whether the error is masked.	0x0
19	R/WOCLR	Unsupported Request Detected [URD]	Set to 1 by the core when it receives an unsupported request, regardless of whether its reporting is enabled or not.	0x0
20	R	Aux Power Detected [APD]	Reserved	0x0
21	R	Transaction Pending [TP]	Indicates if any of the Non-Posted requests issued by the VF are still pending.	0x0
31:22	R	Reserved [R4]	Reserved	0x0

Link Capabilities Register @0xcc

This register advertises the link-specific capabilities of the device incorporating the PCIe core. There are no writable bits at this location. A read to this address returns the Link Capability Register fields of Physical Function 0.

Table 181: i_link_cap

Bits	SW	Name	Description	Reset
3:0	R	Maximum Link Speed [MLS]	Indicates the maximum speed supported by the link (2.5 GT/s, 5 GT/s, 8 GT/s, 16 GT/s per lane). This field is hardwired to 0001 (2.5GT/s) when the strap input PCIE_GENERATION_SEL is set to 0, to 0010 (5 GT/s) when the strap is set to 1, to 0011 (8 GT/s) when the strap input is set to 10, and to 0100 (16 GT/s) when the strap input is set to 11.	0x4
9:4	R	Maximum Link Width [MLW]	Indicates the maximum number of lanes supported by the device. This field is hardwired based on the setting of the LANE_COUNT_IN strap input.	6'd4

Bits	SW	Name	Description	Reset
11:10	R	Active State Power Management [ASPM]	Indicates the level of ASPM support provided by the device. This field can be re-written independently for each Function from the local management bus. When SRIS is enabled in local management register bit, L0s capability is not supported and is forced low.	0x3
14:12	R	L0S Exit Latency [L0SEL]	Specifies the time required for the device to transition from L0S to L0. This parameter is dependent on the Physical Layer implementation. It can be re-written independently for each Function from the local management bus.	0x2
17:15	R	L1 Exit Latency [L1EL]	Specifies the exit latency from L1 state. This parameter is dependent on the Physical Layer implementation. It can be re-written independently for each Function from the local management bus.	0x3
18	R	Clock Power Management [CPM]	Indicates that the device supports removal of referenc clocks. It can be re-written independently for each function from the local management bus.	0x0
19	R	Surprise Down Error Reporting Capability [SDERC]	Indicates the capability of the device to report a Surprise Down error condition. This bit is hardwired to 0 as this version of the core does not support the feature.	0x0
20	R	Data Link Layer Active Reporting Capability [DLLARC]	Set to 1 if the device is capable of reporting that the DL Control and Management State Machine has reached the DL_Active state. This bit is hardwired to 0 as this version of the core does not support the feature.	0x0
21	R	Link Bandwidth Notification Capability [LBNC]	A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms. Reserved for Endpoint.	0x0
22	R	ASPM Optionality Compliance [AOC]	Setting this bit indicates that the device supports the ASPM Optionality feature. It can be turned off by writing a 0 to this bit position through the local management bus.	0x1
23	R	Reserved [R5]	Reserved	0x0
31:24	R	Port Number [PN]	Specifies the port number assigned to the PCI Express link connected to this device.	8'h0

PCI Express Device Capabilities Register 2 @0xe4

This register is not implemented for Virtual Functions. A read to this address returns the Device Capabilities 2 Register fields of Physical Function 0.

Table 182: i_pcie_dev_cap_2

Bits	SW	Name	Description	Reset
3:0	R	Completion Timeout Ranges [CTR]	Specifies the Completion Timeout values supported by the device. This field is set by default to 0010 (10 ms – 250 ms). The actual timeout values are in two programmable local management registers, which allow the timeout settings of the two sub-ranges within Range B to be programmed independently.	0x02
4	R	Completion Timeout Disable Supported [CTDS]	A 1 in this field indicates that the associated Function supports the capability to turn off its Completion timeout. This bit is set to 1 by default, but can be re-written independently for each Function from the local management bus.	0x01
5	R	ARI forwarding support [AFS]	ARI forwarding supported.	0x0
6	R	OP routing supported [OPRS]	Atomic OP routing supported.	0x0
7	R	32-Bit Atomic Op Completer Supported [BAOCS32]	Hardwired to 0.	0x0
8	R	64-Bit Atomic Op Completer Supported [BAOCS64]	Hardwired to 0.	0x0
9	R	128-Bit CAS Atomic Op Completer Supported [BAOCS128]	Hardwired to 0.	0x0
10	R	Reserved [R12]	Reserved	0x0

Bits	SW	Name	Description	Reset
11	R	LTR Mechanism Supported [LMS]	A 1 in this bit position indicates that the Function supports the Latency Tolerance Reporting (LTR) Capability. This bit is set to 1 by default, but can be turned off for all Physical Functions by writing into PF 0.	0x01
13:12	R	TPH Completer Supported [TCS]	These bits, when set, indicate that the Function is capable of serving as a completer for requests with Transaction Processing Hints (TPH). It can be turned off for all Physical Functions by writing into PF 0. Defined Encodings are: 00b TPH and Extended TPH Completer not supported. 01b TPH Completer supported; Extended TPH Completer not supported. 10b Reserved. 11b Both TPH and Extended TPH Completer supported.	0x01
15:14	R	Reserved [R13]	Reserved	0x0
16	R	10-Bit Tag completer supported. [T10CS]	If set function supports 10-bit completer capability; otherwise, the function does not. This field is identical to the PF value.	0x1
17	R	10-Bit Tag Requester supported. [T10RS]	If set function supports 10-bit requester capability; otherwise, the function does not. This field reflects the value in SRIOV capability register	0x0
19:18	R	OBFF Supported [OPFFS]	A 1 in this bit position indicates that the Function supports the Optimized Buffer Flush/Fill (OBFF) capability using message signaling.	0x1
20	R	Extended Format Field Supported [EXFS]	Indicates that the Function supports the 3-bit definition of the Fmt field in the TLP header. This bit is hardwired to 1 for all Physical Functions.	0x1
21	R	End-End TLP Prefix Supported [EEPS]	Indicates whether the Function supports End-End TLP Prefixes. A 1 in this field indicates that the Function supports receiving TLPs containing End-End TLP Prefixes.	0x1
23:22	R	Max End-End TLP Prefixes [MEEP]	Indicates the maximum number of End-End TLP Prefixes supported by the Function. The supported values are: 01b 1 End-End TLP Prefix, 10b 2 End-End TLP Prefixes	0x1
31:24	R	Reserved [R14]	Reserved	0x0

Link Capabilities Register 2 @0xec

This register is not implemented for Virtual Functions. A read to this address returns the Device Capabilities 2 Register fields of Physical Function 0.

Table 183: i_link_cap_2_reg

Bits	SW	Name	Description	Reset
0	R	RSVD	RSVD	1'h0
4:1	R	Supported Link Speeds Vector [SLSV]	This field indicates the supported link speeds of the Controller. For each bit, a value of 1 indicates that the corresponding link speed is supported, while a value of 0 indicates that the corresponding speed is not supported. The bits corresponding to various link speeds are: • Bit 1 = Link Speed 2.5 GT/s • Bit 2 = Link Speed 5 GT/s • Bit 3 = Link Speed 8 GT/s • Bit 4 = Link Speed 16 GT/s This field is hardwired to 00001 (2.5 GT/s) when the PCIE_GENERATION_SEL strap pins of the Controller are set to 000 , 00011 (2.5 and 5 GT/s) when the strap is set to 001 , and 00111 (2.5, 5, and 8 GT/s) when the strap pin is set to 010 , and 01111 (2.5, 5, 8 GT/s and 16 GT/s) when the strap pin is set to 011. For PF0, this field can be written through the LM interface.	0xf
5	R	RSVD	RSVD	1'h0
8:6	R	Reserved [R1]	Reserved	0x0
12:9	R	Lower SKP OS Generation Supported Speeds Vector [LSOGSSV]	If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate.	0x0
15:13	R	Reserved [R2]	Reserved	0x0

Bits	SW	Name	Description	Reset
19:16	R	Lower SKP OS Reception Supported Speeds Vector [LSORSSV]	If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS.	0x0
20	R	RSVD	RSVD	1'h0
22:21	R	Reserved [R3]	Reserved	0x0
23	R	Retimer Presence Detect Supported [RTPDS]	When set to 1b, this bit indicates that the associated Port supports detection and reporting of Retimer presence. This bit is valid for both Downstream Ports and Upstream Ports.	0x1
24	R	Two Retimers Presence Detect Supported [TWRTPDS]	When set to 1b, this bit indicates that the associated Port supports detection and reporting of two Retimers presence. This bit is valid for both Downstream Ports and Upstream Ports.	0x1
30:25	R	Reserved [R25]	Reserved	0x0
31	R	DRS Supported [R31]	Indicates support for the optional Device Readiness Status (DRS) capability. This capability is currently not supported in the Controller.	0x0

Advanced Error Reporting (AER) Enhanced Capability Header Register @0x100

This is the first register in the PCI Express Advanced Error Reporting Capability Structure of a Virtual Function. This register contains the PCI Express Extended Capability ID, the capability version, and the pointer to the next capability structure.

Table 184: i_AER_enhanced_cap_hdr

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECID]	This field is hardwired to the Capability ID assigned by PCI SIG to the PCI Express AER Extended Capability Structure (0001 hex).	0x01
19:16	R	Capability Version [CV]	Specifies the SIG assigned value for the version of the capability structure. This field reflects the setting of the corresponding field in the AER Enhanced Capability Header Register of PF 0.	4'h2
31:20	R	Next Capability Offset [NCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h140

Uncorrectable Error Status Register @0x104

This register provides the status of the various uncorrectable errors detected by the PCI Express core. Software may clear any error bit by writing a 1 into the corresponding bit position. The states of the bits in the Uncorrectable Error Mask Register have no effect on the status bits of this register. The setting of an uncorrectable error status bit causes the core to generate an ERR_FATAL message if the corresponding severity bit of the Uncorrectable Error Severity Register is 1. If the severity bit is 0, however, there are two separate ways the error could be processed:

- In certain cases, the uncorrectable error is treated as an Advisory Non-Fatal Error. These cases are treated as similar to correctable errors, causing the core to generate an ERR_COR message instead of an ERR_NONFATL message. For details on these special cases, refer to Section 6.2.3.2.4 of the PCI Express Base Specifications, Version 1.1.
- In all other cases, the core sends an ERR_NONFATAL message when the error is detected. In all cases, the sending of the error message can be suppressed by setting the bit corresponding to the error type in the Uncorrectable Error Mask Register.

For errors that are not Function-specific, the error status bus is set in the registers belonging to all the Functions associated with the link, but only a single message is generated for the entire link. In the case of certain errors detected by the Transaction Layer, the associated TLP header

is logged in the Shared VF Header Log Registers. All the RW1C bits can also be cleared from the local management bus by writing a 1 into the bit position.If error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted, f/w will be allowed to write into AER uncorrectable Error status register).

Table 185: i_uncorr_err_status

Bits	SW	Name	Description	Reset
3:0	R	Reserved [R0]	Reserved	0x0
4	R	Data Link Protocol Error Status [DLPER]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0
11:5	R	Reserved [R1]	Reserved	0x0
12	R/WOCLR	Poisoned TLP Status [PTS]	This bit is set when the core receives a poisoned TLP from the link, targeted at this VF. This error is Function-specific. This error is considered non-fatal by default. The error is reported by sending an ERR_NONFATAL message. The header of the received TLP with error is logged in the Shared VF Header Log Registers associated with the VF. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).	0x0
13	R	Flow Control Protocol Error Status [FCPES]	This bit is is not implemented for Virtual Functions. Hardwired to 0.	0x0
14	R/WOCLR	Completion Timeout Status [CTS]	This bit is set when the completion timer associated with an outstanding request times out. This error is Function-specific. This error is considered non-fatal by default. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).	0x0
15	R/WOCLR	Completer Abort Status [CAS]	This bit is set when the core has returned the Completer Abort (CA) status to a request received from the link. This error is Function-specific. The header of the received request that caused the error is logged in the Shared VF Header Log Registers. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).	0x0
16	R/WOCLR	Unexpected Completion Status [UCS]	This bit is set when the core has received an unexpected Completion packet from the link. This error is not Function-specific. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).	0x0
17	R	Receiver Overflow Status [Rcvr_Overflow_Status]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0
18	R	Malformed TLP Status [Malformed_TLP_Status]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0
19	R	ECRC Error Status [ECRC_Err_Status]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0
20	R/WOCLR	Unsupported Request Error Status [URES]	This bit is set when the core has received a request from the link that it does not support. This error is not Function-specific. This error is considered non-fatal by default. In the special case described in Sections 6.2.3.2.4.1 of the PCI Express Specifications, the error is reported by sending an ERR_COR message. In all other cases, the error is reported by sending an ERR_NONFATAL message. The header of the received request that caused the error is logged in the Shared VF Header Log Registers. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted.	0x0
21	R	Reserved [R2]	Reserved	0x0
22	R	Uncorrectable Internal Error Status [Uncorr_Int_Err_Status]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0
31:23	R	Reserved [R3]	Reserved	0x0

Uncorrectable Error Mask Register @0x108

This register is not implemented for Virtual Functions. The setting of the mask bits in the Uncorrectable Error Mask Register of the Physical Function apply to all associated VFs.

Table 186: i_uncorr_err_mask

Bits	SW	Name	Description	Reset
31:0	R	Reserved [R4]	(no description)	0x0

Uncorrectable Error Severity Register @0x10c

This register is not implemented for Virtual Functions. The settings of the severity bits in the Uncorrectable Error Severity Register of the Physical Function apply to all associated VFs.

Table 187: i_uncorr_err_severity

Bits	SW	Name	Description	Reset
31:0	R	Reserved [R8]	(no description)	0x0

Correctable Error Status Register @0x110

This register provides the status of the various correctable errors detected by the PCI Express core. Software may clear any error bit by writing a 1 into the corresponding bit position. The states of the bits in the Correctable Error Mask Register have no effect on the status bits of this register. The setting of a correctable error status bit causes the core to generate an ERR_COR error message to the Root Complex if the error is not masked in the Correctable Error Mask Register. For errors that are not Function-specific, the error status bus is set in the registers belonging to all the Functions associated with the link, but only a single message is generated for the entire link. Header logging of received TLPs does not apply to correctable errors. All the RW1C bits can also be cleared from the local management bus by writing a 1 into the bit position.

Table 188: i_corr_err_status

Bits	SW	Name	Description	Reset
0	R	Receiver Error Status [RES]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0
5:1	R	Reserved [R12]	Reserved	0x0
6	R	Bad TP Status [BTPS]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0
7	R	Bad DLLP Status [BDS]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0
8	R	Replay Number Rollover Status [RNRS]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0
11:9	R	Reserved [R13]	Reserved	0x0
12	R	Replay Timer Timeout Status [RTTS]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0
13	R/WOCLR	Advisory Non- Fatal Error Status [ANFES]	This bit is set when an uncorrectable error occurs, which is determined to belong to one of the special cases described in Section 6.2.3.2.4 of the PCI Express 2.0 Specifications. This causes the coreto generate an ERR_COR message in place of an ERR_NONFATAL message. STICKY. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).	0x0
14	R	Corrected Internal Error Status [CIES]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0

Bits	SW	Name	Description	Reset
15	R/WOCLR	Header Log Overflow Status [HLOS]	This bit is set on a Header Log Register overflow, that is, when the header could not be logged in the Header Log Register because it is occupied by a previous header. As per SR-IOV specification, this bit is hardwired to 0 since the Header Log is Shared among VFs. F/w will be allowed to write into this error status field when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).	0x0
31:16	R	Reserved [R14]	Reserved	0x0

Correctable Error Mask Register @0x114

The mask bits in this register control the reporting of correctable errors. For each error type in the Correctable Error Status Register, there is a corresponding bit in this register to mask its reporting. When a mask bit is set, the occurrence of the error is not reported (by asserting the CORRECTABLE_ERROR_OUT output).

Table 189: i_corr_err_mask

Bits	SW	Name	Description	Reset
0	R	Receiver Error Mask [REM]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0
5:1	R	Reserved [R15]	Reserved	0x0
6	R	Bad TLP Mask [BTM]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0
7	R	Bad DLLP Mask [BDM]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0
8	R	Replay Number Rollover Mask [RNRM]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0
11:9	R	Reserved [R16]	Reserved	0x0
12	R	Replay Timer Timeout Mask [RTTM]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0
13	R	Advisory Non-Fatal Error Mask [ANFEM]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0
14	R	Corrected Internal Error Mask [CIEM]	This bit is not implemented for Virtual Functions. Hardwired to 0.	0x0
15	R	Header Log Overflow Mask [HLOM]	This bit, when set, masks the generation of error messages in response to a Header Log register overflow. STICKY. Header logs are shared across Vfs hence this field is reserved. This field is reserved since Header log sharing is selected for this configuration.	0x0
31:16	R	Reserved [R17]	(no description)	0x0

Advanced Error Capabilities and Control Register @0x118

This location contains a pointer to the first error that is reported in the Uncorrectable Error Status Register.

Table 190: i_advcd_err_cap_ctrl

Bits	SW	Name	Description	Reset
4:0	R	First Error Pointer [FER]	This is a 5-bit pointer to the bit position in the Uncorrectable Error Status Register corresponding to the error that was detected first. When there are multiple bits set in the Uncorrectable Error Status Register, this field informs the software which error was observed first. To prevent the field from being overwritten before software was able to read it, this field is not updated while the status bit pointed by it in the Uncorrectable Error Status Register remains set. After the software clears this status bit, a subsequent error condition that sets any bit in the Uncorrectable Error Status Register will update the First Error Pointer. Any uncorrectable error type, including the special cases where the error is reported using an ERR_COR message, will set the First Error Pointer (assuming the software has reset the error pointed by it in the Uncorrectable Error Status Register). STICKY. F/w will be allowed to write into this first error pointer when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).	0x0
5	R	ECRC Generation Capability [EGC]	This read-only bit indicates to the software that the device is capable of generating ECRC in packets transmitted on the link. This bit is hardwired to 0. The setting of the corresponding bit in the Advanced Error Capabilities and Control Register of PF 0 applies to all Virtual Functions.	0x0
6	R	Enable ECRC Generation [EEG]	Enables the ECRC generation on the transmit side of the core. This bit is hardwired to 0. The setting of the corresponding bit in the Advanced Error Capabilities and Control Register of PF 0 applies to all Virtual Functions.	0x0
7	R	ECRC Check Capability [ECCAP]	This read-only bit indicates to the software that the device is capable of checking ECRC in packets received from the link. This bit is hardwired to 0. This setting of the corresponding bit in the Advanced Error Capabilities and Control Register of PF 0 applies to all Virtual Functions.	0x0
8	R	Enable ECRC Check [ECC]	Setting this bit enables ECRC checking on the receive side of the core. This bit is hardwired to 0. The setting of the corresponding bit in the Advanced Error Capabilities and Control Register of PF 0 applies to all Virtual Functions.	0x0
9	R	Multiple Header Recording Capable [MHRC]	This bit is set when the Function has the capability to log more than one error header in its Header Log Registers. It is hardwired to 0.	0x0
10	R	Multiple Header Recording Enable [MHRE]	Setting this bit enables the Function to log multiple error headers in its Header Log Registers. It is hardwired to 0	0x0
31:11	R	Reserved [R18]	Reserved	0x0

Header Log Register 0 @0x11c

This is the first of a set of four registers used to capture the header of a TLP received by the core from the link upon detection of an uncorrectable error. The Controller implements Shared Header Log for VFs. All Virtual Functions associated with the same PF share the same Header Log. When multiple bits are set in the Uncorrectable Error Status Registers of the VFs, the captured header corresponds to the error that was detected first, that is, the error pointed by the First Error Pointer, of the associated VF. To prevent the captured header from being over-written before the software is able to read it, this register is not updated while the status bit pointed by the First Error Pointer in the Uncorrectable Error Status Register remains set. After the software clears this status bit, a subsequent error condition that sets any bit in the Uncorrectable Error Status Register will also cause the Header Log Registers to be updated. The doublewords of the TLP header are stored in the Header Log Registers with their bytes transposed. That is the byte containing the Type/Format fields of the header is stored at bit positions 31:24 of the Header Log Register 0. F/w will be allowed to write Header log info when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).

Table 191: i_hdr_log_0

Bits	SW	Name	Description	Reset
31:0	R	Header DWORD 0 [HD0]	First DWORD of captured TLP header STICKY.	0x0

Header Log Register 1 @0x120

This location contains the second Dword of the captured header of a TLP received from the link. The bytes are stored in transposed order.

Table 192: i_hdr_log_1

Bits	SW	Name	Description	Reset
31:0	R	Header DWORD 1 [HD1]	Second DWORD of captured TLP header STICKY.	0x0

Header Log Register 2 @0x124

This location contains the third Dword of the captured header of a TLP received from the link. The bytes are stored in transposed order.

Table 193: i_hdr_log_2

Bits	SW	Name	Description	Reset
31:0	R	Header DWORD 2 [HD2]	Third DWORD of captured TLP header STICKY.	0x0

Header Log Register 3 @0x128

If the captured TLP header is four Dwords long, this location contains the last Dword of the captured header of a TLP received from the link. If the captured header is a three-Dword header, this register is unused. The bytes of the Dword are stored in this register in transposed order.

Table 194: i_hdr_log_3

Bits	SW	Name	Description	Reset
31:0	R	Header DWORD 3 [HD3]	Fourth DWORD of captured TLP header STICKY.	0x0

TLP Prefix Log Register 0 @0x138

First TLP Prefix (if present) associated with the TLP whose header is in the Header Log Register. The bytes are in transposed order. F/w will be allowed to TLP prefix log info when error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).

Table 195: i_tlp_pre_log_0

Bits	SW	Name	Description	Reset
31:0	R	TLP Prefix 0 [HD1]	First TLP Prefix of captured TLP STICKY.	0x0

TLP Prefix Log Register 1 @0x13c

Second TLP Prefix (if present) associated with the TLP whose header is in the Header Log Register. The bytes are in transposed order. F/w will be allowed to write TLP prefix log info when

error emulation emulation feature is enabled (i.e., if bit12 of Debug MUX Control 3 register is asserted).

Table 196: i_tlp_pre_log_1

Bits	SW	Name	Description	Reset
31:0	R	TLP Prefix 1 [HD1]	Second TLP Prefix of captured TLP STICKY.	0x0

ARI Extended Capability Header Register @0x140

This register is used to enable the Alternate Routing ID interpretation. This register contains the PCI Express Extended Capability ID, the capability version, and the pointer to the next capability structure.

Table 197: i_ARI_ext_cap_hdr

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PCCID]	This field is hardwired to the Capability ID assigned by PCI SIG to the ARI Extended Capability (000E hex).	0x0E
19:16	R	Capability Version [CV]	Specifies the SIG-assigned value for the version of the capability structure. This field is taken from the setting of the corresponding field in the ARI Extended Capability Header Register of PF 0.	0x01
31:20	R	Next Capability Offset [NCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h274

ARI Capability Register and ARI Control Register @0x144

This location contains the ARI Capability Register and the ARI Control Register. All the fields in this register are hardwired to 0.

Table 198: i_ARI_cap_and_ctrl

Bits	SW	Name	Description	Reset
31:0	R	Reserved [R13]	Reserved	0x0

TPH Requester Enhanced Capability Header Register @0x274

This register contains the PCI Express Extended Capability ID for Transaction Processing Hints (TPH) Requester Capability, its capability version, and the pointer to the next capability structure.

Table 199: i_TPH_req_ext_cap_header_reg

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECID]	This field is hardwired to the Capability ID assigned by PCI SIG to the TPH Requester Capability.	0x0017
19:16	R	Capability Version [CV]	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified for all VFs by writing into this register field of Physical Function 0 from the local management bus.	0x1

Bits	SW	Name	Description	Reset
31:20	R	Next Capability Offset [NCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h0

TPH Requester Capability Register @0x278

This is a read-only register that specifies the capabilities associated with the implementation of the TPH in the device. All fields in this register, except the reserved ones, can be modified from the local management bus.

Table 200: i_TPH_req_cap_reg

Bits	SW	Name	Description	Reset
0	R	No ST Mode Supported [NSTM]	When set to 1, indicates that this Function supports the 'No ST Mode' for the generation of TPH Steering Tags. In the No ST Mode, the device must use a Steering Tag value of 0 for all requests. This bit is hardwired to 1 as all TPH Requesters are required to support the No ST Mode of operation.	0x1
1	R	Interrupt Vector Mode Supported [IVMS]	A setting of 1 indicates that the Function supports the Interrupt Vector Mode for TPH Steering Tag generation. In the Interrupt Vector Mode, Steering Tags are attached to MSI/MSI-X interrupt requests. The Steering Tag for each interrupt request is selected by the MSI/MSI-X interrupt vector number. This bit is set to 1 by default, but can be modified from the local management bus.	0x1
2	R	Device- Specific Mode Supported [DSMS]	A setting of 1 indicates that the Function supports the Device- Specific Mode for TPH Steering Tag generation. In this mode, the Steering Tags are supplied by the client for each request through the HAL master interface. The client typically chooses the Steering Tag values from the ST Table, but is not required to do so. This bit is set to 1 by default, but can be modified from the local management bus.	0x1
7:3	R	Reserved [R0]	Reserved	0x0
8	R	Extended TPH Requester Supported [ERS]	When set to 1, indicates that the Function is capable of generating requests with a TPH TLP Prefix.	0x0
10:9	R	ST Table Location [STTL]	The setting of this field indicates if a Steering Tag Table is implemented for this Function, and its location if present. Values are: • 00 = ST Table not present • 01 = ST Table in the TPH Requester Capability Structure • 10 = ST values stored in the MSI-X Table in client RAM • 11 = Reserved This field can be modified from the local management bus.	0x1
15:11	R	Reserved [R1]	Reserved	0x0
26:16	R	ST Table Size [STTS]	Specifies the number of entries in the Steering Tag Table (0 = 1 entry, 1 = 2 entries, and so on). Max limit is 64 entries when the ST Table is located in the TPH Requester Capability Structure, and 2048 entries when located in the MSI-X table. Each entry is 16 bits long. This field can be modified from the local management bus.	11'd7
31:27	R	Reserved [R2]	Reserved	0x0

TPH Requester Control Register @0x27c

This register can be used by the software to enable the TPH Request capability of the Function, and to select the mode of generation of Steering Tags.

Table 201: i_TPH_req_ctrl_reg

Bits	SW	Name	Description	Reset
2:0	R/W	ST Mode [STM]	This field selects the ST mode (000 = No Steering Tag Mode, 001 = Interrupt Vector Mode, 010 = Device-Specific Mode, other values are reserved). The VF_TPH_ST_MODE output of the core reflects the setting of this register field (bits 3:0 for VF 0 and so on). This field can also be written from the local management bus.	0x0
7:3	R	RSVD	RSVD	5'h00
9:8	R/W	TPH Requester Enable [TRE]	When set, the Function is allowed to generate requests with Transaction Processing Hints. Defined Encodings are: • 00b - Function operating as a Requester is not permitted to issue Requests with TPH or Extended TPH. • 01b - Function operating as a Requester is permitted to issue Requests with TPH and is not permitted to issue Requests with Extended TPH. • 10b - Reserved • 11b - Function operating as a Requester is permitted to issue Requests with TPH and Extended TPH.	0x00
31:10	R	Reserved [R10]	Reserved	0x0

TPH ST Table @0x280

This table stores the Steering Tags for the TPH Capability. This table has eight entries per Function, each 16 bits long. Two of these entries occupy each 32-bit word of the table. Each of the entries can be read/written through the link (by a Configuration transaction) or through the local management bus. The format of each register is shown below.

Table 202: i_TPH_tab_0

Bits	SW	Name	Description	Reset
7:0	R/W	ST 0 Lower [ST0L]	Lower eight bits of the first Steering Tag. This is the 8-bit Steering Tag sent out in requests.	0x0
15:8	R	ST 0 Upper [ST0U]	This field is used for the upper eight bits of the first Steering Tag when Extended TPH Requester support is enabled.	0x0
23:16	R/W	ST 1 Lower [ST1L]	Lower eight bits of the second Steering Tag. This is the 8-bit Steering Tag sent out in requests.	0x0
31:24	R	ST 1 Upper [ST1U]	This field is used for the upper eight bits of the second Steering Tag when Extended TPH Requester support is enabled.	0x0

TPH ST Table @0x284

This table stores the Steering Tags for the TPH Capability. This table has eight entries per Function, each 16 bits long. Two of these entries occupy each 32-bit word of the table. Each of the entries can be read/written through the link (by a Configuration transaction) or through the local management bus. The format of each register is shown below.

Table 203: i_TPH_tab_1

Bits	SW	Name	Description	Reset
7:0	R/W	ST 0 Lower [ST0L]	Lower eight bits of the first Steering Tag. This is the 8- bit Steering Tag sent out in requests.	0x0
15:8	R	ST 0 Upper [ST0U]	This field is used for the upper eight bits of the first Steering Tag when Extended TPH Requester support is enabled.	0x0
23:16	R/W	ST 1 Lower [ST1L]	Lower eight bits of the second Steering Tag. This is the 8-bit Steering Tag sent out in requests.	0x0

Bits	SW	Name	Description	Reset
31:24	R	ST 1 Upper [ST1U]	This field is used for the upper eight bits of the second Steering Tag when Extended TPH Requester support is enabled.	0x0

TPH ST Table @0x288

This table stores the Steering Tags for the TPH Capability. This table has eight entries per Function, each 16 bits long. Two of these entries occupy each 32-bit word of the table. Each of the entries can be read/written through the link (by a Configuration transaction) or through the local management bus. The format of each register is shown below.

Table 204: i_TPH_tab_2

Bits	SW	Name	Description	Reset
7:0	R/W	ST 0 Lower [ST0L]	Lower eight bits of the first Steering Tag. This is the 8- bit Steering Tag sent out in requests.	0x0
15:8	R	ST 0 Upper [ST0U]	This field is used for the upper eight bits of the first Steering Tag when Extended TPH Requester support is enabled.	0x0
23:16	R/W	ST 1 Lower [ST1L]	Lower eight bits of the second Steering Tag. This is the 8-bit Steering Tag sent out in requests.	0x0
31:24	R	ST 1 Upper [ST1U]	This field is used for the upper eight bits of the second Steering Tag when Extended TPH Requester support is enabled.	0x0

TPH ST Table @0x28c

This table stores the Steering Tags for the TPH Capability. This table has eight entries per Function, each 16 bits long. Two of these entries occupy each 32-bit word of the table. Each of the entries can be read/written through the link (by a Configuration transaction) or through the local management bus. The format of each register is shown below.

Table 205: i_TPH_tab_3

Bits	SW	Name	Description	Reset
7:0	R/W	ST 0 Lower [ST0L]	Lower eight bits of the first Steering Tag. This is the 8- bit Steering Tag sent out in requests.	0x0
15:8	R	ST 0 Upper [ST0U]	This field is used for the upper eight bits of the first Steering Tag when Extended TPH Requester support is enabled.	0x0
23:16	R/W	ST 1 Lower [ST1L]	Lower eight bits of the second Steering Tag. This is the 8-bit Steering Tag sent out in requests.	0x0
31:24	R	ST 1 Upper [ST1U]	This field is used for the upper eight bits of the second Steering Tag when Extended TPH Requester support is enabled.	0x0

ATS Capability Header Register @0x5c0

This location contains the ATS Extended Capabilities Register, its Capability ID, Version, and a pointer to the next capability.

Table 206: ats_cap_header

Bits	SW	Name	Description	Reset
15:0	R	ATS Extended Capability ID [ATSCAPID]	Indicates the ATS Extended Capability structure. This field must return a Capability ID of 000Fh indicating that this is an ATS Extended Capability structure.	0x0F
19:16	R	ats_cap_version_ [ATSCAPVER]	Specifies the SIG assigned value for the version of the capability structure.	0x1

Bits	SW	Name	Description	Reset
31:20	R	Next Capability Offset [ATSNXTCAP]	Indicates offset to the next PCI Express capability structure.	0x0

ATS Capability Control Register @0x5c4

ATS Capability and Control Register.

Table 207: ats_cap_control

Bits	SW	Name	Description	Reset
4:0	R	ATS Invalidate Queue Depth [ATSINVQD]	The number of Invalidate Requests that the Function can accept before putting backpressure on the upstream connection. If 0 0000b, the Function can accept 32 Invalidate Requests.	0x1
5	R	ATS Page Aligned Req [ATSPGALNREQ]	If Set, indicates the Untranslated Address is always aligned to a 4096 byte boundary.	0x1
6	R	Global invalidate supported [ATSGIS]	If Set, the Function supports InvalidationRequests that have the Global Invalidate bit Set. If Clear, the Function ignores the Global Invalidate bit in all Invalidate Requests.	0x1
15:7	R	RSVD	RSVD	9'h000
20:16	R/W	ATS Smallest Translation Unit [ATSSTU]	This value indicates to the Function the minimum number of 4096-byte blocks that is indicated in a Translation Completions or Invalidate Requests. This is a power of 2 multiplier and the number of blocks is 2STU. A value of 0 0000b indicates one block and a value of 1 1111b indicates 2^31 blocks.	0x0
30:21	R	Reserved [R30]	Reserved	0x0
31	R/W	ATS Enable [ATSEN]	When Set, the Function is enabled to cache translations. Default value is 0b.	0x0

Root Port Configuration Register Set

The Root Port register set is accessible only when the core is strapped in the Root Port mode. These registers are accessible only from the local management bus, and are selected when the address bits MGMT_ADDR[18:10] are all zeroes.

The Root Port registers are described in detail below.

Vendor ID and Device ID @0x0

16-bit Vendor ID register and 16-bit Device ID register.

Table 208: i_vendor_id_device_id

Bits	SW	Name	Description	Reset
15:0	R	Vendor ID [VID]	This is the Vendor ID assigned by PCI SIG to the manufacturer of the device. The Vendor ID is set in the Vendor ID Register within the local management register block.	16'h17cd
31:16	R	Device ID [DID]	Device ID assigned by the manufacturer of the device. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	16'h100

Command and Status Register @0x4

16-bit Command Register and 16-bit Status Register.

Table 209: i_command_status

Bits	SW	Name	Description	Reset
0	R/W	I/O-Space Enable [ISE]	For a Function with a Type 1 Configuration Space header (Controller in RP Mode), this bit controls the response to I/O Space accesses received on its Primary Side. *Note:* The Controller does not generate any response based on this bit. Client must check that this bit is set to '1' before initiating any I/O requests on the pcie_master_AXI interface.	0x0
1	R/W	Mem-Space Enable [MSE]	For a Function with a Type 1 Configuration Space header (Controller in RP Mode), this bit controls the response to Memory Space accesses received on its Primary Side. *Note:* The Controller does not generate any response based on this bit. Client must check that this bit is set to '1' before initiating any Memory requests on the pcie_master_AXI interface.	0x0
2	R/W	Bus-Master Enable [BE]	For a Function with a Type 1 Configurations Space header (Controller in RP Mode), this bit controls forwarding of Memory or I/O Requests by a Port in the Upstream direction. *Note:* The Controller does not generate any response based on this bit. Client application logic must use this bit and respond to requests appropriately: • When this bit is '1', Client logic can process the Memory and I/O Requests received from PCIe Link normally. • When this bit is '0', Client logic must handle Memory and I/O Requests received from PCIe Link as Unsupported Requests.	0x0
5:3	R	Reserved [R0]	Reserved	0x0

Bits	SW	Name	Description	Reset
6	R/W	Parity Error Response Enable [PERE]	When this bit is 1, the Controller sets the Master Data Parity Error status bit when it detects the following error conditions: **1.** The Controller receives a poisoned completion from the link in response to a request. **2.** The Controller sends out a poisoned write request on the link (this may be because an underflow occurred during the packet transfer at the host interface of the Controller). When this bit is 0, the Master Data Parity Error status bit is never set.	0x0
7	R	Reserved [R1]	Reserved	0x0
8	R/W	SERR Enable [SE]	Enables the reporting of fatal and non-fatal errors detected by the Controller to the Root Complex.	0x0
9	R	Reserved [R2]	Reserved	0x0
10	R/W	INTx Message Disabled [IMD]	Enables or disables the transmission of INTx Assert and De-assert messages from the Controller. The setting of this bit has no effect on the operation of the Controller in the RC mode.	0x0
15:11	R	Reserved [R3]	Reserved	0x0
18:16	R	Reserved [R4]	Reserved	0x0
19	R	Interrupt Status [IS]	This bit is valid only when the Controller is configured to support legacy interrupts. Indicates that the Controller has a pending interrupt; that is, the Controller has sent an Assert_INTx message but has not transmitted a corresponding Deassert_INTx message.	0x0
20	R	Capabilities List [CL]	Indicates the presence of PCI Extended Capabilities registers. This bit is hardwired to 1.	0x1
23:21	R	Reserved [R5]	Reserved	0x0
24	R/WOCLR	Master Data Parity Error [MDPE]	When the Parity Error Response enable bit is 1, the Controller sets this bit when it detects the following error conditions: **1.** The Controller receives a poisoned request from the link. **2.** The Controller has sent a Poisoned Completion downstream to the link This bit remains 0 when the Parity Error Response enable bit is 0. This field can be forced to 1 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0
26:25	R	Reserved [R6]	Reserved	0x0
27	R/WOCLR	Signaled Target Abort [STA]	This bit is set when the Controller has sent a completion to the link with the Completer Abort status. This field can also be cleared from the local management APB bus by writing a 1 into this bit position. This field can be forced to 1 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0
28	R/WOCLR	Received Target Abort [RTA]	This bit is set when the Controller has received a completion from the link with the Completer Abort status. This field can also be cleared from the local management APB bus by writing a 1 into this bit position. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0
29	R/WOCLR	Received Master Abort [RMA]	This bit is set when the Controller has received a completion from the link with the Unsupported Request status. This field can also be cleared from the local management APB bus by writing a 1 into this bit position This field can be forced to 1 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0

Bits	SW	Name	Description	Reset
30	R/WOCLR	Signaled System Error [SSE]	The Controller sets this bit: • On receiving an error message from the link, if SERR-Enable in PCI Command Register is 1 and SERR-Enable in the Bridge Control Register is also 1. • On any internal Fatal/Non-Fatal error detected, if SERR-Enable in PCI Command Register is 1. This field can also be cleared from the local management APB bus by writing a 1 into this bit position. This field can be forced to 1 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0
31	R/WOCLR	Detected Parity Error [DPE]	This bit is set when the Controller has received a poisoned TLP. The Parity Error Response enable bit (bit 6) has no effect on the setting of this bit. This field can also be cleared from the local management bus APB by writing a 1 into this bit position. This field can be forced to 1 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0

Revision ID and Class Code Register @0x8

This register contains the Revision ID and Class Code associated with the device incorporating the PCIe Controller.

Table 210: i_revision_id_class_code

Bits	SW	Name	Description	Reset
7:0	R	Revision ID [RID]	Assigned by the manufacturer of the device to identify the revision number of the device. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	8'h0
15:8	R	Programming Interface Byte [PIB]	Identifies the register set layout of the device. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0
23:16	R	Sub-Class Code [SCC]	Identifies a sub-category within the selected function. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	8'h0
31:24	R	Class Code [CC]	Identifies the function of the device. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	8'h0

BIST, Header Type, Latency Timer and Cache Line Size Registers @0xc

This location contains the BIST, header-type, Latency Timer, and Cache Line Size Registers.

Table 211: i_bist_header_latency_cache_line

Bits	SW	Name	Description	Reset
7:0	R/W	Cache Line Size [CLS]	Cache Line Size Register defined in PCI Specifications 3.0. This field can be read or written, both from the link and from the local management bus, but its value is not used.	0x0
15:8	R	Latency Timer [LT]	This is an unused field and is hardwired to 0.	0x0
22:16	R	Header Type [HT]	Identifies format of header. This field is hardwired to 1.	0x1
23	R	Device Type [DT]	Identifies whether the device supports a single Function or multiple Functions. Hardwired to zero	0x0
31:24	R	BIST Register [BR]	BIST control register. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0

Root Complex Base Address Register 0 @0x10

This is the Base Address Register 0 in the Type-1 Config Space. It can be configured as a 32-bit memory BAR, a 32-bit I/O BAR, or it can be paired with RC BAR 1 to form a 64-bit memory BAR. The parameters of this BAR are configured in the local management register Root Complex BAR Configuration Register.

Table 212: i_RC_BAR_0

Bits	SW	Name	Description	Reset
0	R	BAR Type [MSI0]	Specifies whether this BAR defines a memory address range or an I/O address range (0 = memory, 1 = I/O). The value read in this field is determined by the setting of Root Complex BAR Configuration Register.	0x0
1	R	Reserved [R7]	This bit is hardwired to 0 for both memory and I/O BARs.	0x0
2	R	Size [S0]	For memory BAR, this bit reads as 0 when BAR 0 is configured as a 32-bit BAR, and as 1 when configured as a 64-bit BAR. For I/O BAR, this is bit 3 of the base address. The value read in this field is determined by the setting of Root Complex BAR Configuration Register.	0x0
3	R	Prefetchability [P0]	For memory BAR, this bit reads as 1 when BAR 0 is configured as a prefetchable BAR, and as 0 when configured as a non-prefetchable BAR. For I/O BAR, his is bit 3 of the base address. The value read in this field is determined by the setting of Root Complex BAR Configuration Register.	0x0
21:4	R	Base Address - RO part [BAMR0]	This field defines the base address of the memory address range. The number of implemented bits in this field determines the BAR aperture configured in Root Complex BAR Configuration Register. All other bits are not writeable and are read as 0's.	0x0
31:22	R/W	Base Address - RW part [BAMRW]	This field defines the base address of the memory address range. The number of implemented bits in this field determines the BAR aperture configured in Root Complex BAR Configuration Register. All other bits are not writeable and are read as 0's.	0x0

Root Complex Base Address Register 1 @0x14

This is the Base Address Register 1 in the Type-1 Config Space. It can be configured as a 32-bit memory BAR, a 32-bit I/O BAR, or it can be paired with RC BAR 0 to form a 64-bit memory BAR. The parameters of this BAR are configured in the local management register Root Complex BAR Configuration Register.

Table 213: i_RC_BAR_1

Bits	SW	Name	Description	Reset
31:0	R	Reserved [R7]	This field is reserved at power-on. This can be changed using BAR configuration register in LM space.	0x0

Primary Bus Number, Secondary Bus Number, Subordinate Bus Number, Secondary Latency Timer @0x18

This location contains the 8-bit fields: Primary Bus Number, Secondary Bus Number,Subordinate Bus Number, Secondary Latency Timer.

Table 214: i_pcie_bus_numbers

Bits	SW	Name	Description	Reset
7:0	R/W	Primary Bus Number [PBN]	This field can be read and written from the local management bus, but its value is not used within the Controller.	0x0
15:8	R/W	Secondary Bus Number [SBN]	This field can be read and written from the local management bus, but its value is not used within the Controller.	0x0
23:16	R/W	Subordinate Bus Number [SUBN]	This field can be read and written from the local management bus, but its value is not used within the Controller.	0x0
31:24	R	Secondary Latency Timer [SLTN]	This field is not implemented.	0x0

I/O Base, I/O Limit, Secondary Status Register @0x1c

This location contains the 8-bit I/O Base Register, the 8-bit I/O Limit Register, and the 16-bit Secondary Status Registers.

Table 215: i_pcie_io_base_limit

Bits	SW	Name	Description	Reset
0	R	Type1 cfg I/O bar size [IOBS1]	Value set in Type1 cfg I/O bar size (bit 20 of RC BAR CONFIG register). If Type1 cfg I/O bar enable bit (bit 19 in RC BAR CONFIG register) is not set, then this field will be hard coded to 0.	0x0
3:1	R	Reserved [R1]	Reserved	0x0
7:4	R	I/O Base Register [IBR]	This field can be read and written from the local management bus if I/O BAR is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.	0x0
8	R	Type1 cfg I/O bar size [IOBS2]	Value set in Type1 cfg I/O bar size (bit 20 of RC BAR CONFIG register). If Type1 cfg I/O bar enable bit (bit 19 in RC BAR CONFIG register) is not set, then this field will be hard coded to 0.	0x0
11:9	R	Reserved [R2]	Reserved	0x0
15:12	R	I/O Limit Register [ILR]	This field can be read and written from the local management bus if I/O BAR is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.	0x0
23:16	R	Reserved [R3]	Reserved	0x0
24	R/WOCLR	Master Data Parity Error [MPE]	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write. Note that this bit can be set only when the Parity Error Response Enable bit is set in the Bridge Control Register	0x0
26:25	R	Reserved [R4]	Reserved	0x0
27	R/WOCLR	Signaled Target Abort [STA]	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0
28	R/WOCLR	Recieved Target Abort [RTA]	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0

Bits	SW	Name	Description	Reset
29	R/WOCLR	Received Master Abort [RMA]	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0
30	R/WOCLR	Received System Error [RSE]	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0
31	R/WOCLR	Detected Parity Error [DPE]	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0

Memory Base, Memory Limit @0x20

This location contains the 16-bit Memory Base Register and the 16-bit Memory Limit Register.

Table 216: i_pcie_mem_base_limit

Bits	SW	Name	Description	Reset
3:0	R	Reserved [R1]	Reserved	0x0
15:4	R/W	Memory Base Register [MBR]	This field can be read and written from the local management APB bus, but its value is not used within the Controller.	12'h0
19:16	R	Reserved [R2]	Reserved	0x0
31:20	R/W	Memory Limit Register [MLR]	This field can be read and written from the local management APB bus, but its value is not used within the Controller.	12'h0

Prefetchable Memory Base,Prefetchable Memory Limit @0x24

This location contains the Prefetchable Memory Base Register and the Prefetchable Memory Limit Register. This register is enabled by programming the Root Complex BAR configuration register in the Local Management space.

Table 217: i_pcie_prefetch_base_limit

Bits	SW	Name	Description	Reset
15:0	R	Prefetchable Memory Base Register [PMBR]	This field can be read and written from the local management APB bus if prefetchable memory is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.	16'h0
31:16	R	Prefetchable Memory Limit Register [PMLR]	This field can be read and written from the local management APB bus if prefetchable memory is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.	16'h0

Prefetchable Base Upper @0x28

This location contains the upper 32 bits of the Prefetchable Base Register. This register is enabled by programming the Root Complex BAR configuration register in the Local Management space.

Table 218: i_pcie_prefetch_base_upper

Bits	SW	Name	Description	Reset
31:0	R	Prefetchable Base Register Upper [PBRU]	This field can be read and written from the local management APB bus if 64-bit prefetchable memory is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.	32'h0

Prefetchable Limit Upper @0x2c

This location contains the upper 32 bits of the Prefetchable Limit Register. This register is enabled by programming the Root Complex BAR configuration register in the Local Management space.

Table 219: i_pcie_prefetch_limit_upper

Bits	SW	Name	Description	Reset
31:0	R	Prefetchable Limit Register Upper [PLRU]	This field can be read and written from the local management APB bus if 64-bit prefetchable memory is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.	32'h0

I/O Base Upper, I/O Limit Upper @0x30

This location contains the upper 16 bits of the I/O Base and I/O Limit Registers.

Table 220: i_pcie_io_base_limit_upper

Bits	SW	Name	Description	Reset
15:0	R	I/O Base Register Upper [IBRU]	This field can be read and written from the local management bus if 32-bit I/O BAR is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.	0x0
31:16	R	I/O Limit Register Upper [ILR]	This field can be read and written from the local management bus if 32-bit I/O BAR is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.	0x0

Capabilities Pointer @0x34

This location contains the pointer to the first PCI Capabilities Structure.

Table 221: i_capabilities_pointer

Bits	SW	Name	Description	Reset
7:0	R	Capabilities Pointer [CP]	Contains pointer to the first PCI Capability Structure. It can be re-written independently for every Function from the local management APB bus.	0x80
31:8	R	Reserved [R15]	Reserved	0x0

Expansion ROM Base Address Register @0x38

This register is used to define the base address and range of an optional expansion ROM. The address bits [10:0] of the Expansion ROM Base Address are always set to 0. Thus, the ROM address space always starts at a 2 Kbyte boundary. The maximum allowed size of the expansion ROM address space is 16 Mbytes. The aperture of the Expansion ROM BAR can be

set to any power of 2 in the range from 2 Kbytes to 16 Mbytes by programming the Expansion ROM BAR control field in the Root Complex BAR configuration register.

Table 222: i_expan_rom_base_addr

Bits	SW	Name	Description	Reset
0	R/W	Address Decode Enable [ADE]	This bit must be set to 1 by the configuration software to enable the expansion ROM.	0x0
10:1	R	Reserved [R1]	Reserved	0x0
11	R	ROM Base Address [RBARO]	Defines the base address and range of the expansion ROM address space. The number of writeable bits in this field determines the size of the range (BAR aperture). All other bits are not writeable, and are read as 0's.	0x0
31:12	R/W	ROM Base Address [RBARW]	Defines the base address and range of the expansion ROM address space. The number of writeable bits in this field determines the size of the range (BAR aperture). All other bits are not writeable, and are read as 0's.	0x0

Interrupt Line, Interrupt Pin Register and Bridge Control Register @0x3c

This location contains the Interrupt Line Register, the Interrupt Pin Register, and the Bridge Control Register.

Table 223: i_intrpt_line_intrpt_pin

Bits	SW	Name	Description	Reset
7:0	R/W	Interrupt Line Register [ILR]	This field can be read and written from the local management bus, but its value is not used within the Controller. The given reset value is for PF0.	8'hff
10:8	R	Interrupt Pin Register [IPR]	Identifies the interrupt input (A, B, C, D) to which this Functions interrupt output is connected to (01 = INTA, 02 = INTB, 03 = INTC, 04 = INTD). The assignment of interrupt inputs to Functions is fixed when the Controller is configured. This field can be re-written independently for each Function from the local management bus. Default values - PF0: 01 (INTA), PF1: 02 (INTB).	0x01
15:11	R	Reserved [R5]	Reserved	0x0
16	R/W	Parity Error Response Enable [PERE]	This field can be read and written from the local management APB bus. It is used only to enable the Master Data Parity Error bit in the Secondary Status Register.	0x0
17	R/W	Bridge Control SERR Enable [BCSE]	This field can be read and written from the local management APB bus, but its value is not used within the Controller.	0x0
18	R/W	ISA Enable [ISAE]	This field can be read and written from the local management APB bus, but its value is not used within the Controller.	0x0
19	R/W	VGA Enable [VGAE]	This field can be read and written from the local management APB bus, but its value is not used within the Controller.	0x0
20	R/W	VGA 16 DEcode [VGA16D]	This field can be read and written from the local management APB bus, but its value is not used within the Controller.	0x0
21	R	Reserved [R21]	Reserved	0x0
22	R/W	Bridge Control Register Secondary Bus Reset [BCRSBR]	This field can be read and written from the local management APB bus. When set, it initiates a hot reset on the link.	0x0
31:23	R	Reserved [R23]	Reserved	0x0

Power Management Capabilities Register @0x80

This location contains the Power Management Capabilities Register, its Capability ID, and a pointer to the next capability. In the RC mode, the settings of the fields of this register have no effect on the operation of the Controller

Table 224: i_pwr_mgmt_cap

Bits	SW	Name	Description	Reset
7:0	R	Capability ID [CID]	Identifies that the capability structure is for Power Management. This field is set by default to 01 hex. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x01
15:8	R	Capabilities Pointer [CP]	Contains pointer to the next PCI Capability Structure. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	8'h90
18:16	R	Version ID [VID]	Indicates the version of the PCI Bus Power Management Specifications that the Function implements. This field is set by default to 011 (Version 1.2). This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x3
19	R	PME Clock [PC]	Not applicable to PCI Express. This bit is hardwired to 0.	0x0
20	R	Reserved [R0]	Reserved	0x0
21	R	Device Specific Initialization Bit [DSI]	This bit, when set, indicates that the device requires additional configuration steps beyond setting up its PCI configuration space, to bring it to the D0 active state from the D0 uninitialized state. This bit is hardwired to 0.	0x0
24:22	R	Max Current Required from Aux Power Supply [MCRAPS]	Specifies the maximum current drawn by the device from the aux power source in the D3cold state. This field is not implemented in devices not supporting PME notification when in the D3cold state, and is therefore hardwired to 0.	0x0
25	R	D1 Support [D1S]	Set if the Function supports the D1 power state. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x1
26	R	D2 Support [D2S]	Set if the Function supports the D2 power state. Currently hardwired to 0.	0x0
27	R	PME Support for D0 State [PSD0S]	Indicates whether the Function is capable of sending PME messages when in the D0 state. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x01
28	R	PME Support for D1 State [PSD1S]	Indicates whether the Function is capable of sending PME messages when in the D1 state. This bit is set to 1 by default, but can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.	0x1
29	R	PME Support for D2 State [PSD2S]	Indicates whether the Function is capable of sending PME messages when in the D2 state. This bit is hardwired to 0 because D2 state is not supported.	0x0
30	R	PME Support for D3(hot) State [PSDHS]	Indicates whether the Function is capable of sending PME messages when in the D3hot state. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x01
31	R	PME Support for D3(cold) State [PSDCS]	Indicates whether the Function is capable of sending PME messages when in the D3cold state. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0

Power Management Control/Status Report @0x84

This location contains the Power Management Control/Status and Data Registers.

Table 225: i_pwr_mgmt_ctrl_stat_rep

Bits	SW	Name	Description	Reset
1:0	R/W	Power State [PS]	This field can also be read or written from the local management APBbus.	0x0
2	R	Reserved [R4]	Reserved	0x0
3	R	No Soft Reset [NSR]	This bit is set to 1 by default. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x01
7:4	R	Reserved [R3]	Reserved	0x0
8	R/W	PME Enable [PE]	This bit can be set or cleared from the local management APB bus by writing a 1 or 0, respectively.	0x0
14:9	R	Reserved [R2]	Reserved	0x0
15	R/ WOCLR	PME Status [PMES]	This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0
23:16	R	Reserved [R1]	Reserved	0x0
31:24	R	Data Register [DR]	This optional register is not implemented in the PCIe Controller. This field is hardwired to 0.	0x0

MSI Control Register @0x90

This register is used only when the Controller is configured to support Message Signaled Interrupts (MSIs). In addition to the MSI control bits, this location also contains the Capability ID for MSI and the pointer to the next PCI Capability Structure.

Table 226: i_msi_ctrl_reg

Bits	SW	Name	Description	Reset
7:0	R	Capability ID [CID1]	Specifies that the capability structure is for MSI. Hardwired to 05 hex.	0x05
15:8	R	Capabilities Pointer [CP1]	Pointer to the next PCI Capability Structure. This can be modified from the local management bus. This field can be written from the local management bus.	8'hb0
16	R/W	MSI Enable [ME]	Set by the configuration program to enable the MSI feature. This field can also be written from the local management bus.	0x0
19:17	R	Multiple Message Capable [MMC]	Encodes the number of distinct messages that the Controller is capable of generating for this Function (000 = 1, 001 = 2, 010 = 4, 011 = 8, 100 = 16, 101 = 32). Thus, this field defines the number of the interrupt vectors for this Function. The Controller allows up to 32 distinct messages, but the setting of this field must be based on the number of interrupt inputs of the Controller that are actually used by the client. For example, if the client logic uses 8 of the 32 distinct MSI interrupt inputs of the Controller for this Function, then the value of this field must be set to 011. This field can be written from the local management bus.	0x0
22:20	R/W	Multiple Message Enable [MME]	Encodes the number of distinct messages that the Controller is programmed to generate for this Function (000 = 1, 001 = 2, 010 = 4, 011 = 8, 100 = 16, 101 = 32). This setting must be based on the number of interrupt inputs of the Controller that are actually used by this Function. This field can be written from the local management bus.	0x0
23	R	64-Bit Address Capable [BAC64]	Set to 1 to indicate that the device is capable of generating 64-bit addresses for MSI messages.Can be modified using local management interface	0x01
24	R	MSI masking capable [MC]	can be modified using localmanagement interface	0x01
31:25	R	Reserved [R0]	Reserved	0x0

MSI Message Low Address Register @0x94

This register contains the first 32 bits of the address to be used in the MSI messages generated by the Controller for this Function. This address is taken as a 32-bit address if the value programmed in the MSI Message High Address Register is 0. Otherwise, this address is taken as the least significant 32 bits of the 64-bit address sent in MSI messages.

Table 227: i_msi_msg_low_addr

Bits	SW	Name	Description	Reset
1:0	R	Reserved [R1]	The two lower bits of the address are hardwired to 0 to align the address on a double-word boundary.	0x0
31:2	R/W	Message Address Low [MAL]	Lower bits of the address to be used in MSI messages. This field can also be written from the local management bus.	0x0

MSI Message High Address Register @0x98

This register contains the most significant 32 bits of the 64-bit address sent by the Controller in MSI messages. A value of all zeroes in this register is taken to mean that the Controller should use 32-bit addresses in the messages.

Table 228: i_msi_msg_hi_addr

Bits	SW	Name	Description	Reset
31:0	R/W	Message Address High [MAH]	Contains bits 63:32 of the 64-bit address to be used in MSI Messages. A value of 0 specifies that 32-bit addresses are to be used in the messages. This field can also be written from the local management bus.	0x0

MSI Message Data Register @0x9c

This register contains the write data to be used in the MSI messages to be generated for the associated PCI Function. When the number of distinct messages programmed in the MSI Control Register is 1, the 32-bit value from this register is used as the data value in the MSI packets generated by the Controller for this Function. If the number of distinct messages is more than 1, the least significant bits of the programmed value are replaced with the encoded interrupt vector [31:0] of the specific message to generate the write data value for the message.

Table 229: i_msi_msg_data

Bits	SW	Name	Description	Reset
15:0	R/W	Message Data [MD]	Message data to be used for this Function. This field can also be written from the local management bus.	0x0
31:16	R	Reserved [R2]	Hardwired to 0.	0x0

MSI Mask Register @0xa0

This register contains the MSI mask bits, one for each of the interrupt levels.

Table 230: i_msi_mask

Bits	SW	Name	Description	Reset
0	R/W	MSI Mask [MM]	Mask bits for MSI interrupts. The Multiple Message Capable field of the MSI Control Register specifies the number of distinct interrupts for the Function, which determines the number of valid mask bits.	0x0

Bits	SW	Name	Description	Reset
31:1	R	RSVD	RSVD	31'h00000000

MSI Pending Bits Register @0xa4

This register contains the MSI pending interrupt bits, one for each of the interrupt levels.

Table 231: i_msi_pending_bits

Bits	SW	Name	Description	Reset
0	R	MSI Pending Bits [MP]	Pending bits for MSI interrupts. This field can be written from the APB interface to refelct the current pending status.	0x0
31:1	R	RSVD	RSVD	31'h00000000

MSI-X Control Register @0xb0

This register contains the MSI-X configuration bits, the Capability ID for MSI-X and the pointer to the next PCI Capability Structure.

Table 232: i_msix_ctrl

Bits	SW	Name	Description	Reset
7:0	R	Capability ID [CID]	Identifies that the capability structure is for MSI-X. This field is set by default to 11 hex. It can be re-written independently for each Function from the local management bus.	0x11
15:8	R	Capabilities Pointer [CP]	Contains pointer to the next PCI Capability Structure. This is set to point to the PCI Express Capability Structure at 30 hex. This can be re-written independently for each Function from the local management bus.	8'hc0
26:16	R	MSI-X Table Size [MSIXTS]	Specifies the size of the MSI-X Table, that is, the number of interrupt vectors defined for the Function. The programmed value is 1 minus the size of the table (that is, this field is set to 0 if the table size is 1). It can be re- written independently for each Function from the local management bus.	11'h0
29:27	R	Reserved [R0]	Reserved	0x0
30	R/W	Function Mask [FM]	This bit serves as a global mask to all the interrupt conditions associated with this Function. When this bit is set, the Controller will not send out MSI-X messages from this Function. This field can also be written from the local management bus.	0x0
31	R/W	MSI-X Enable [MSIXE]	Set by the configuration program to enable the MSI-X feature. This field can also be written from the local management bus.	0x0

MSI-X Table Offset Register @0xb4

This register is used to specify the location of the MSI-X Table in memory. All the 32 bits of this register can be re-written independently for each Function from the local management bus.

Table 233: i_msix_tbl_offset

Bits	SW	Name	Description	Reset
2:0	R	BAR Indicator Register [BARI]	Identifies the BAR corresponding to the memory address range where the MSI-X Table is located (000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5).	3'd0

Bits	SW	Name	Description	Reset
31:3	R	Table Offset [TO]	Offset of the memory address where the MSI-X Table is located, relative to the selected BAR. The three least significant bits of the address are omitted as the addresses are QWORD aligned.	29'h0

MSI-X Pending Interrupt Register @0xb8

This register is used to specify the location of the MSI-X Pending Bit Array (PBA). The PBA is a structure in memory containing the pending interrupt bits. All the 32 bits of this register can be re-written independently for each Function from the local management bus.

Table 234: i_msix_pending_intrpt

Bits	SW	Name	Description	Reset
2:0	R	BAR Indicator Register [BARI1]	Identifies the BAR corresponding to the memory address range where the PBA Structure is located (000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5). The value programmed must be the same as the BAR Indicator configured in the MSI-X Table Offset Register. Identifies the BAR corresponding to the memory address range where the PBA Structure is located (000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5). The value programmed must be the same as the BAR Indicator configured in the MSI-X Table Offset Register.	3'd0
31:3	R	PBA Offset [PBAO]	Offset of the memory address where the PBA is located, relative to the selected BAR. The three least significant bits of the address are omitted as the addresses are QWORD aligned.	29'h1

PCI Express Capability List Register @0xc0

This location identifies the PCI Express device type and its capabilities. It also contains the Capability ID for the PCI Express Structure and the pointer to the next capability structure.

Table 235: i_pcie_cap_list

Bits	SW	Name	Description	Reset
7:0	R	Capability ID [CID]	Specifies Capability ID assigned by PCI SIG for this structure. This field is hardwired to 10 hex.	0x010
15:8	R	Next Capability Pointer [NCP]	Points to the next PCI capability structure. Set to 0 because this is the last capability structure.	0x0
19:16	R	Capability Version [PCV]	Identifies the version number of the capability structure. This field is set to 2 by default to indicate that the Controller is compatible to PCI Express Base Specification Revision 3.0. Can be modified using local management interface after asserting input signal MGMT_TYPE1_CONFIG_REG_ACCESS high.	0x2
23:20	R	Device Type [DT]	Indicates the type of device implementing this Function. This field is hardwired to 4 in the RP mode.	0x4
24	R	Slot Implemented [SI]	When Set, this bit indicates that the Link associated with this Port is connected to a slot	1'b1
29:25	R	Interrupt Message Number [IMN]	Identifies the MSI or MSI-X interrupt vector for the interrupt message generated corresponding to the status bits in the Slot Status Register, Root Status Register, or this capability structure. This field must be defined based on the chosen interrupt mode - MSI or MSI-X. This field is hardwired to 0.	0x0
30	R	TCS Routing Supported [TRS]	When set to 1, this bit indicates that the device supports routing of Trusted Configuration Requests. Not valid for Endpoints. Hardwired to 0.	0x0
31	R	Reserved [R0]	Reserved	0x0

PCI Express Device Capabilities Register @0xc4

This register advertises the capabilities of the PCI Express device.

Table 236: i_pcie_cap

Bits	SW	Name	Description	Reset
2:0	R	Max Payload Size [MP]	Specifies maximum payload size supported by the device. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	3'b011
4:3	R	Phantom Functions Supported [PFS]	This field is used to extend the tag field by combining unused Function bits with the tag bits. This field is hardwired to 00 to disable this feature.	0x0
5	R	Extended Tag Field Supported [ETFS]	Set when device allows the tag field to be extended from 5 to 8 bits. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x1
8:6	R	Acceptable L0S Latency [AL0L]	Specifies acceptable latency that the Endpoint can tolerate while transitioning from L0S to L0. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0
11:9	R	Acceptable L1 Latency [AL1L]	Specifies acceptable latency that the Endpoint can tolerate while transitioning from L1 to L0. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0
14:12	R	Reserved [R3]	Reserved	0x0
15	R	Role-Based Error Reporting [RER]	Enables role-based errer reporting. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	1'b1
17:16	R	Reserved [R4]	Reserved	0x0
25:18	R	Captured Slot Power Limit Value [CSP]	Specifies upper limit on power supplied by slot. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write. .	0x0
27:26	R	Captured Power Limit Scale [CPLS]	Specifies the scale used by Slot Power Limit Value. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write. .	0x0
28	R	Function level reset capability [FLRC]	A value of 1b indicates the Function supports the optional Function Level Reset mechanism	0x0
31:29	R	Reserved [R5]	Reserved	0x0

PCI Express Device Control and Status Register @0xc8

This register contains control and status bits associated with the device.

Table 237: i_pcie_dev_ctrl_status

Bits	SW	Name	Description	Reset
0	R/W	Enable Correctable Error Reporting [ECER]	This bit is used to gate the CORRECTABLE_ERROR_OUT output of the Controller in Root Port mode. When a Correctable and Unmasked Error is detected Internally or when a ERR_CORR message is received by the Controller, in Root Port mode, this bit gates the assertion of CORRECTABLE_ERROR_OUT output.	0x0

Bits	SW	Name	Description	Reset
1	R/W	Enable Non- Fatal Error Reporting [ENFER]	This bit is used to gate the NON_FATAL_ERROR_OUT output of the Controller in Root Port mode. When an Uncorrectable, Unmasked Error with Uncorrectable Error Severity set to 0 is detected Internally or when a ERR_NON_FATAL message is received by the Controller, in Root Port mode, this bit gates the assertion of NON_FATAL_ERROR_OUT output. *Note:* Alternately, the SERR Enable bit in the Command Register can also be set to enable assertion of NON_FATAL_ERROR_OUT.	0x0
2	R/W	Enable Fatal Error Reporting [EFER]	This bit is used to gate the FATAL_ERROR_OUT output of the Controller in Root Port mode. When an Uncorrectable, Unmasked Error with Uncorrectable Error Severity set to 1 is detected Internally or when a ERR_FATAL message is received by the Controller, in Root Port mode, this bit gates the assertion of FATAL_ERROR_OUT output. *Note:* Alternately, the SERR Enable bit in the Command Register can also be set to enable assertion of FATAL_ERROR_OUT.	0x0
3	R/W	Enable Unsupported Request Reporting [EURR]	This bit is used to gate the CORRECTABLE_ERROR_OUT, NON_FATAL_ERROR_OUT, FATAL_ERROR_OUT output in Root Port mode on receiving unsupported requests. *Note:* Alternately, the SERR Enable bit in the Command Register can also be set to enable assertion of FATAL_ERROR_OUT on receiving uncorrectable unsupported requests.	0x0
4	R/W	Enable Relaxed Ordering [ERO]	When set, this bit indicates that the device is allowed to set the Relaxed Ordering bit in the Attributes field of transactions initiated from it when the transactions do not require Strong Ordering.	0x1
7:5	R/W	Max Payload Size [MP]	Specifies the maximum TLP payload size configured. The device must be able to receive a TLP of this maximum size, and should not generate TLP's larger than this value. Software must set this field based on the maximum payload size in the Device Capabilities Register, and the capability of the other side.	0x0
8	R/W	Extended Tag Enable [ETE]	When Set, this bit enables a Function to use an 8- bit Tag field as a Requester. If the bit is Clear, the Function is restricted to a 5-bit Tag field.	0x1
9	R	phantum functions enable [PFE]	Hardwired to 0.	0x0
10	R	aux power PM enable [APPME]	Hardwired to 0.	0x0
11	R/W	Enable no snoop [ENS]	If this bit is Set, the Function is permitted to Set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency.	0x1
14:12	R/W	Max Read Request Size [MRR]	Specifies the maximum size allowed in read requests generated by the device.	3'b010
15	R	Reserved [R7]	Hardwired to 0.	0x0
16	R/WOCLR	Correctable Error Detected [CED]	Set to 1 by the Controller when it detects a correctable error, regardless of whether the error is masked.	0x0
17	R/WOCLR	Non-Fatal Error Detected [NFED]	Set to 1 by the Controller when it detects a non- fatal error, regardless of whether the error is masked.	0x0
18	R/WOCLR	Fatal Error Detected [FED]	Set to 1 by the Controller when it detects a fatal error, regardless of whether the error is masked.	0x0
19	R/WOCLR	Unsupported Request Detected [URD]	Set to 1 by the Controller when it receives an unsupported request.	0x0
20	R	Aux Power Detected [APD]	Set when auxiliary power is detected by the device. This is an unused field.	0x0
21	R	Transaction Pending [TP]	Indicates if any of the Non-Posted requests issued by the RC are still pending.	0x0
31:22	R	Reserved [R8]	(no description)	0x0

Link Capabilities Register @0xcc

This register advertises the link-specific capabilities of the device incorporating the PCIe Controller.

Table 238: i_link_cap

Bits	SW	Name	Description	Reset
3:0	R	Max Link Speed [MLS]	Indicates the speeds supported by the link (2.5 GT/s, 5 GT/s, 8 GT/s, 16 GT/s). This field is hardwired to 0001 (2.5GT/s) when the strap input PCIE_GENERATION_SEL is set to 0, to 0010 (5 GT/s) when the strap is set to 1 , to 0011 (8 GT/s) when the strap input is set to 10, and to 0100 (16 GT/s) when the strap input is set to 11.	0x4
9:4	R	Max Link Width [MLW]	Indicates the maximum number of lanes supported by the device. This field is hardwired based on the setting of the LANE_COUNT_IN strap input.	0x4
11:10	R	Active State Power Management [ASPM]	Indicates the level of ASPM support provided by the device. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x3
14:12	R	L0S Exit Latency [L0EL]	Specifies the time required for the device to transition from L0S to L0. This parameter is dependent on the Physical Layer implementation. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x2
17:15	R	L1 Exit Latency [L1EL]	Specifies the exit latency from L1 state. This parameter is dependent on the Physical Layer implementation. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x3
18	R	Clock Power Management [CPM]	Indicates that the device supports removal of reference clocks. Not supported in this version of the Controller. Hardwired to 0.	0x0
19	R	Surprise Down Error Reporting Capability [SERC]	Indicates the capability of the device to report a Surprise Down error condition. It can be re-written in RC mode from local management bus.	0x0
20	R	Data Link Layer Active Reporting Capability [DARC]	Set to 1 if the device is capable of reporting that the DL Control and Management State Machine has reached the DL_Active state. This bit is hardwired to 0 as this version of the Controller does not support the feature.	0x0
21	R	Link Bandwidth Notification Capability [LBNC]	A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x1
22	R	ASPM Optionality Compliance [ASPMOC]	A 1 in this position indicates the device supports the ASPM Optionality feature. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x1
23	R	Reserved [R9]	Reserved	0x0
31:24	R	Port Number [PN]	Specifies the port number assigned to the PCI Express link connected to this device. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0

Link Control and Status Register @0xd0

This register contains control and status bits specific to the PCI Express link.

Table 239: i_link_ctrl_status

Bits	SW	Name	Description	Reset
1:0	R/W	Active State Power Management Control [ASPMC]	Controls the level of ASPM support on the PCI Express link associated with the function. The valid setting are: • 00: ASPM disabled • 01: L0s entry enabled, L1 disabled • 10: L1 entry enabled, L0s disabled • 11: Both L0s and L1 enabled Note that the ASPM Control bits can be enabled only if the corresponding ASPM Support[1:0] bit is 1 in the Link Capabilities Register.	0x0

Bits	SW	Name	Description	Reset
2	R	Reserved [R10]	Reserved	0x0
3	R	Read Completion Boundary [RCB]	Indicates the Read Completion Boundary of the Root Port (0 = 64 bytes, 1 = 128 bytes). This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0
4	R/W	Link Disable [LD]	Writing a 1 to this bit position causes the LTSSM to go to the Disable Link state. The LTSSM stays in the Disable Link state while this bit is set.	0x0
5	R	Retrain Link [RL]	Setting this bit to 1 causes the LTSSM to initiate link training. This bit always reads as 0. This bit can be set by Host SW at any time independent of the LTSSM state. If the LTSSM is not in L0 state, the Controller will internally register the retrain command and initiate the link retrain immediately after the LTSSM reaches L0. For example, if the LTSSM is already in Recovery, the Controller will initiate Retrain Link after the LTSSM transitions back to L0 state.	0x0
6	R/W	Common Clock Configuration [CCC]	A value of 0 indicates that the reference clock of this device is asynchronous to that of the upstream device. A value of 1 indicates that the reference clock is common.	0x0
7	R/W	Extended Synch [ES]	Set to 1 to extend the sequence of ordered sets transmitted while exiting from the L0S state.	0x0
8	R	Enable Clock Power Management [ECPM]	This field is hardwired to 0 when the Controller is in the RC mode.	0x0
9	R/W	Hardware Autonomous Width Disable [HAWD]	When this bit is set, the local application must not request to change the operating width of the link, other than attempting to correct unreliable Link operation by reducing Link width.	0x0
10	R/W	Link Bandwidth Management Interrupt Enable [LBMIE]	When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This enables an interrupt to be generated through PHY_INTERRUPT_OUT if triggered. Hardwired to 0 if Link Bandwidth Notification Capability is 0.	0x0
11	R/W	Link Autonomous Bandwidth Interrupt Enable [LABIE]	When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set. This enables an interrupt to be generated through PHY_INTERRUPT_OUT if triggered. Hardwired to 0 if Link Bandwidth Notification Capability is 0.	0x0
15:12	R	Reserved [R11]	Reserved	0x0
19:16	R	Negotiated Link Speed [NLS]	Negotiated link speed of the device. The only supported speed IDs are 2.5 GT/s per lane (0001), 5.0 GT/s per lane (0010), 8.0 GT/s per lane (0011), and 16.0 GT/s per lane (0100).	0x1
25:20	R	Negotiated Link Width [NLW]	Set at the end of link training to the actual link width negotiated between the two sides.	0x4
26	R	Reserved [R12]	Reserved	0x0
27	R	Link Training Status [LTS]	This bit is set to 1 when the LTSSM is in the Recovery or Configuration states, or if a 1 has been written to the Retrain Link bit but the link training has not yet begun.	0x0
28	R	Slot Clock Configuration [SCC]	Indicates that the device uses the reference clock provided by the connector. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0
29	R	Data Link Layer Active [DA]	Indicates the status of the Data Link Layer. Set to 1 when the DL Control and Management State Machine has reached the DL_Active state. This bit is hardwired to 0 in this version of the Controller.	0x0
30	R/WOCLR	Link Bandwidth Management Status [LBMS]	This bit is Set by hardware to indicate that either link training has completed following write to retrain link bit, or when HW has changed link speed or width to attempt to correct unreliable link operation. This triggers an interrupt to be generated through PHY_INTERRUPT_OUT if enabled. Hardwired to 0 if Link Bandwidth Notification Capability is 0.	0x0

Bits	SW	Name	Description	Reset
31	R/WOCLR	Link Autonomous Bandwidth Status [LABS]	This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This triggers an interrupt to be generated through PHY_INTERRUPT_OUT if enabled. Hardwired to 0 if Link Bandwidth Notification Capability is 0.	0x0

Slot Capability Register @0xd4

The Slot Capabilities register identifies PCI Express slot specific capabilities.

Table 240: i_slot_capability

Bits	SW	Name	Description	Reset
0	R	Attention Button Present [ABPRSNT]	When Set, this bit indicates that an Attention Button for this slot is electrically controlled by the chassis.	1'b0
1	R	Power Controller Present [PCP]	When Set, this bit indicates that a software programmable Power Controller is implemented for this slot/adapter (depending on form factor).	1'b0
2	R	MRL Sensor Present [MRLSP]	When Set, this bit indicates that an MRL Sensor is implemented on the chassis for this slot.	1'b0
3	R	Attention Indicator Present [AIP]	When Set, this bit indicates that an Attention Indicator is electrically controlled by the chassis.	1'b0
4	R	Power Indicator Present [PIP]	When Set, this bit indicates that a Power Indicator is electrically controlled by the chassis for this slot.	1'b0
5	R	Hot-Plug Surprise [HPS]	When Set, this bit indicates that an adapter present in this slot might be removed from the system without any prior notification. This is a form factor specific capability. This bit is an indication to the operating system to allow for such removal without impacting continued software operation.	1'b0
6	R	Hot-Plug Capable [HPC]	When Set, this bit indicates that this slot is capable of supporting hot-plug operations.	1'b0
14:7	R	Slot Power Limit Value [SPLV]	In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by the slot (se6.9) or by other means to the adapter. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field except when the Slot Power Limit Scale field equals 00b (1.0x) and Slot Power Limit Value exceeds EFh, the following alternative encodings are used: • F0h = 250 W Slot Power Limit • F1h = 275 W Slot Power Limit • F2h = 300 W Slot Power Limit • F3h to FFh = Reserved for Slot Power Limit values above 300 W. This register must be implemented if the Slot Implemented bit is Set. Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/ firmware initialization is 0000 0000b.	8'b00000000
16:15	R	Slot Power Limit Scale [SPLS]	Specifies the scale used for the Slot Power Limit Value. Range of Values: • 00b = 1.0x • 01b = 0.1x • 10b = 0.01x • 11b = 0.001x This register must be implemented if the Slot Implemented bit is Set. Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/ firmware initialization is 00b.	2'b00
17	R	Electromechanic Interlock Present [EIP]	When Set, this bit indicates that an Electromechanical Interlock is implemented on the chassis for this slot.	1'b0

Bits	SW	Name	Description	Reset
18	R	No Command Completed Support [NCCS]	When Set, this bit indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug Controller. This bit is only permitted to be Set if the hot-plug capable Port is able to accept writes to all fields of the Slot Control register without delay between successive writes.	1'b0
31:19	R	Physical Slot Number [PSN]	This field indicates the physical slot number attached to this Port. This field must be hardware initialized to a value that assigns a slot number that is unique within the chassis, regardless of the form factor associated with the slot. This field must be initialized to zero for Ports connected to devices that are either integrated on the system board or integrated within the same silicon as the Switch device or Root Port.	13'd0

Slot Control and Status Register @0xd8

This register contains control bits specific to PCI Express slot parameters and status bits specific to the PCI Express Slot. All the read-write bits in this register can also be written from the local management APB bus.

Table 241: i_slot_ctrl_status

Bits	SW	Name	Description	Reset
0	R/W	Attention Button Pressed Enable [ABPE]	When Set to 1b, this bit enables software notification on an attention button pressed event. If the Attention Button Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.	1'b0
1	R/W	Power Fault Detected Enable [PFDE]	When Set, this bit enables software notification on a power fault event If a Power Controller that supports power fault detection is not implemented, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.	1'b0
2	R/W	MRL Sensor Changed Enable [MSCE]	When Set, this bit enables software notification on a MRL sensor changed event If the MRL Sensor Present bit in the Slot Capabilities register is Clear, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.	1'b0
3	R/W	Presence Detect Changed Enable [PDCE]	When Set, this bit enables software notification on a presence detect changed event. If the Hot-Plug Capable bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.	1'b0
4	R/W	Command Completed Interrupt Enable [CCIE]	If Command Completed notification is supported (if the No Command Completed Support bit in the Slot Capabilities register is 0b), when Set, this bit enables software notification when a hot- plug command is completed by the Hot-Plug Controller. If Command Completed notification is not supported, this bit must be hardwired to 0b. Default value of this bit is 0b.	1'b0
5	R/W	Hot-Plug Interrupt Enable [HPIE]	When Set, this bit enables generation of an interrupt on enabled hot-plug events. If the Hot Plug Capable bit in the Slot Capabilities register is Clear, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.	1'b0
7:6	R/W	Attention Indicator Control [AIC]	If an Attention Indicator is implemented, writes to this field set the Attention Indicator to the written state. Reads of this field must reflect the value from the latest write. Defined encodings are: • 00b Reserved • 01b On • 10b Blink • 11b Off	2'b11
9:8	R/W	Power Indicator Control [PIC]	If a Power Indicator is implemented, writes to this field set the Power Indicator to the written state. Reads of this field must reflect the value from the latest write. Defined encodings are: • 00b Reserved • 01b On • 10b Blink • 11b Off	2'b11

Bits	SW	Name	Description	Reset
10	R/W	Power Controller Control [PCC]	If a Power Controller is implemented, this bit when written sets the power state of the slot per the defined encodings. Reads of this bit must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write, if required to, without waiting for the previous command to complete in which case the read value is undefined. The defined encodings are: • 0b Power On • 1b Power Off	1'b1
11	R	Electromechanic Interlock Control [EMIC]	If an Electromechanical Interlock is implemented, a write of 1b to this bit causes the state of the interlock to toggle. A write of 0b to this bit has no effect. A read of this bit always returns a 0b.	1'b0
12	R/W	Data Link Layer State Changed Enable [DLLSCE]	If the Data Link Layer Link Active Reporting capability is 1b, this bit enables software notification when Data Link Layer Link Active bit is changed. If the Data Link Layer Link Active Reporting Capable bit is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.	1'b0
15:13	R	Reserved [RSCS1]	Reserved	0x0
16	R/WOCLR	Attention Button Pressed [ABPRSD]	If an Attention Button is implemented, this bit is Set when the attention button is pressed. If an Attention Button is not supported, this bit must not be Set.	0x0
17	R/WOCLR	Power Fault Detected [PFD]	If a Power Controller that supports power fault detection is implemented, this bit is Set when the Power Controller detects a power fault at this slot. Note that, depending on hardware capability, it is possible that a power fault can be detected at any time, independent of the Power Controller Control setting or the occupancy of the slot. If power fault detection is not supported, this bit must not be Set.	0x0
18	R/WOCLR	MRL Sensor Changed [MRLSC]	If an MRL sensor is implemented, this bit is Set when a MRL Sensor state change is detected. If an MRL sensor is not implemented, this bit must not be Set.	0x0
19	R/WOCLR	Presence Detect Changed [PDC]	This bit is set when the value reported in the Presence Detect State bit is changed.	0x0
20	R/WOCLR	Command Completed [CMDCMPL]	If Command Completed notification is supported (if the No Command Completed Support bit in the Slot Capabilities register is 0b), this bit is Set when a hot-plug command has completed and the Hot-Plug Controller is ready to accept a subsequent command. The Command Completed status bit is Set as an indication to host software that the Hot-Plug Controller has processed the previous command and is ready to receive the next command; it provides no guarantee that the action corresponding to the command is complete. If Command Completed notification is not supported, this bit must be hardwired to 0b.	0x0
21	R	MRL Sensor State [MRLSS]	This bit reports the status of the MRL sensor if implemented. Defined encodings are: • 0b MRL Closed • 1b MRL Open	1'b1
22	R	Presence Detect State [PDS]	This bit indicates the presence of an adapter in the slot, reflected by the logical 'OR' of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot's corresponding form factor. Note that the in-band presence detect mechanism requires that power be applied to an adapter for its presence to be detected. Consequently, form factors that require a power controller for hot-plug must implement a physical pin presence detect mechanism. Defined encodings are: • 0b Slot Empty • 1b Card Present in slot	0x0
23	R	Electromechanic Interlock Status [EMIS]	If an Electromechanical Interlock is implemented, this bit indicates the status of the Electromechanical Interlock. Defined encodings are: • 0b Electromechanical Interlock Disengaged • 1b Electromechanical Interlock Engaged	0x0

Bits	SW	Name	Description	Reset
24	R/WOCLR	Data Link Layer State Changed [DLLSC]	This bit is Set when the value reported in the Data Link Layer Link Active bit of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read the Data Link Layer Link Active bit of the Link Status register to determine if the Link is active before initiating configuration cycles to the hot plugged device.	0x0
31:25	R	Reserved [RSCS2]	Reserved	0x0

Root Control and Capability Register @0xdc

This register controls and identifies PCI Express Root Complex specific parameters.

Table 242: i_root_ctrl_cap

Bits	SW	Name	Description	Reset
0	R/W	System Error on Correctable Error Enable [SECEE]	This field can be read and written from the local management APB bus, but its value is not used within the Controller.	0x0
1	R/W	System Error on Non-Fatal Error Enable [SENFEE]	This field can be read and written from the local management APB bus, but its value is not used within the Controller.	0x0
2	R/W	System Error on Fatal Error Enable [SEFEE]	This field can be read and written from the local management APB bus, but its value is not used within the Controller.	0x0
3	R/W	PME Interrupt Enable [PMEIE]	This field can be read and written from the local management APB bus, but its value is not used within the Controller.	0x0
4	R	CRS Software Visibility Enable [CRSSVE]	This capability is not implemented and this bit is hardwired to 0b.	0x0
31:5	R	Reserved [R27]	Reserved	0x0

Root Status Register @0xe0

This register controls and identifies PCI Express Root Complex specific parameters.

Table 243: i_root_status

Bits	SW	Name	Description	Reset
15:0	R	PME Requester ID [PMERID]	This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0
16	R/WOCLR	PME Status [PMES]	This field is not set by the Controller but can be cleared by writing a 1 from the local management APB bus. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0
17	R	PME Pending [PMEP]	This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0
31:18	R	Reserved [R18]	Reserved	0x0

PCI Express Device Capabilities 2 Register @0xe4

This register advertises the capabilities of the PCI Express device.

Table 244: i_pcie_cap_2

Bits	SW	Name	Description	Reset
3:0	R	Completion Timeout Ranges [CTR]	Specifies the Completion Timeout values supported by the device. This field is set by default to 0010 (10 ms – 250 ms), but can be modified from the local management APB bus. The actual timeout values are in two programmable local management registers, which allow the timeout settings of the two sub-ranges within Range B to be programmed independently. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	4'b0010
4	R	Completion Timeout Disable Supported [CTDS]	A 1 in this field indicates that the associated Function supports the capability to turn off its Completion timeout. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	1'b1
5	R	ARI Forwarding Supported [AFS]	A 1 in this bit indicates that the device is able to forward TLPs with function number greater than eight. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x1
6	R	Atomic OP routing supported [AOPRS]	Applicable only to Switch Upstream Ports, Switch Downstream Ports, and Root Ports; must be 0b for other Function types. This bit must be set to 1b if the Port supports this optional capability. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0
7	R	32-Bit Atomic Op Completer Supported [ACS32]	Hardwired to 0.	0x0
8	R	64-bit Atomic Op Completer Supported [ACS64]	Hardwired to 0.	0x0
9	R	128-bit CAS Atomic Op Completer Supported [ACS128]	Hardwired to 0.	0x0
10	R	Reserved [R14]	Reserved	0x0
11	R	LTR mechanism supported [LMS]	A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x1
12	R	TPH Completer Supported [TPHC]	These bits, when set, indicate that the Function is capable of serving as a completer for requests with Transaction Processing Hints (TPH). It can be turned off for all Physical Functions by writing into PF 0. Defined Encodings are: • 00b TPH and Extended TPH Completer not supported • 01b TPH Completer supported; Extended TPH Completer not supported • 10b Reserved • 11b Both TPH and Extended TPH Completer supported	0x01
13	R	RSVD	RSVD	1'h0
15:14	R	Reserved [R15]	Reserved	0x0
16	R	10-Bit Tag completer supported. [T10CS]	If set function supports 1-bit completer capability; otherwise, the function does not. This field can be modified using local management interface.	0x1
17	R	10-Bit Tag Requester supported. [T10RS]	If set function supports 1-bit requester capability; otherwise, the function does not. This bit can be disabled using local the management register.	0x0
19:18	R	OBFF Supported [OBFF]	A 1 in this bit position indicates that the Function supports the Optimized Buffer Flush/Fill (OBFF) capability using message signaling. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x1
20	R	Extended Format Field Supported [EXFS]	Indicates that the Function supports the 3-bit definition of the Fmt field in the TLP header. This bit is hardwired to 1 for all physical functions.	0x1

Bits	SW	Name	Description	Reset
21	R	End-End TLP Prefix Supported [EEPS]	Indicates whether the Function supports End-End TLP Prefixes. A 1 in this field indicates that the Function supports receiving TLPs containing End-End TLP Prefixes. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x1
23:22	R	Max End-End TLP Prefixes [MEEP]	Indicates the maximum number of End-End TLP Prefixes supported by the Function. The supported values are: • 01b 1 End-End TLP Prefix • 10b 2 End-End TLP Prefixes. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x1
31:24	R	Reserved [R16]	Reserved	0x0

PCI Express Device Control and Status 2 Register @0xe8

This register contains control and status bits associated with the device.

Table 245: i_pcie_dev_ctrl_status_2

Bits	SW	Name	Description	Reset
3:0	R/W	Completion Timeout Value [CTV]	Specifies the Completion Timeout value for the device. Allowable values are 0101 (sub-range 1) and 0110 (sub-range 2). The corresponding timeout values are stored in the local management register's Completion Timeout Interval Registers 0 and 1, respectively. Value of 0 selects completion timeout from Completion-Timeout-Interval-Registers-0 in local management register.	0x0
4	R/W	Completion Timeout Disable [CTD]	Setting this bit disables the Completion Timeout in the device.	0x0
5	R/W	ARI Forwarding Enable [AFE]	A 1 in this filed indicates that the port treats fields 7:0 of the ID as function number while converting a Type 1 config packet to type 0 config packet.	0x0
6	R	Atomic Op Requester Enable [AORE]	This bit must be set to enable the generation of Atomic Op Requests. If the client logic attempts to send an Atomic Op when this bit is not set, logic in the Controller will nullify the TLP on its way to the link.	0x0
7	R	Reserved [R18]	Reserved	0x0
8	R	IDO Request Enable [IRE]	When this bit is 1, the RC is allowed to set the ID- based Ordering (IDO) Attribute bit in the requests it generates.	0x0
9	R	IDO Completion Enable [ICE]	When this bit is 1, the RC is allowed to set the ID-based Ordering (IDO) Attribute bit in the Completions it generates.	0x0
10	R/W	LTR Mechanism Enable [LTRME]	This must be set to 1 to enable the Latency Tolerance Reporting Mechanism. This bit is implemented only in PF 0. Its default value is 1, but can be modified from the local management bus. This bit is read-only in PF 1.	0x0
11	R	Reserved [R19]	Reserved	0x0
12	R	10-Bit Tag Requester Enable [T10RE]	10bit TAGs generation are not supported in this configuration.	0x0
14:13	R/W	OBFF Enable [OBFFE]	Enables the Optimized Buffer Flush/Fill (OBFF) capability in the device. Valid settings are 00 (disabled), 01 (Variation A), and 10 (Variation B).	0x0
31:15	R	Reserved [R20]	(no description)	0x0

Link Capabilities Register 2 @0xec

This register advertises the supported link speeds of the Controller.

Table 246: i_link_cap_2

Bits	SW	Name	Description	Reset
0	R	RSVD	RSVD	1'h0
4:1	R	Supported Link Speeds Vector [SLSV]	This field indicates the supported link speeds of the Controller. For each bit, a value of 1 indicates that the corresponding link speed is supported, while a value of 0 indicates that the corresponding speed is not supported. The bits corresponding to various link speeds are: • Bit 1 = Link Speed 2.5 GT/s, • Bit 2 = Link Speed 5 GT/s, • Bit 3 = Link Speed 8 GT/s, • Bit 4 = Link Speed 16 GT/s. This field is hardwired to 0001 (2.5 GT/s) when the PCIE_GENERATION_SEL strap pins of the Controller are set to 0, to 0011 (2.5 and 5 GT/s) when the strap is set to 1, to 0111 (2.5, 5, and 8 GT/s) when the strap pin is set to 10, and to 1111 (2.5, 5, 8 and 16 GT/s) when the strap pin is set to 11.	0xf
5	R	RSVD	RSVD	1'h0
8:6	R	Reserved [R1]	Reserved	0x0
12:9	R	Lower SKP OS Generation Supported Speeds Vector [LSOGSSV]	If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate.	0x0
15:13	R	Reserved [R2]	Reserved	0x0
19:16	R	Lower SKP OS Reception Supported Speeds Vector [LSORSSV]	If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS.	0x0
20	R	RSVD	RSVD	1'h0
22:21	R	Reserved [R3]	Reserved	0x0
23	R	Retimer Presence Detect Supported [RTPDS]	When set to 1b, this bit indicates that the associated Port supports detection and reporting of Retimer presence. This bit is valid for both Downstream Ports and Upstream Ports.	0x1
24	R	Two Retimers Presence Detect Supported [TWRTPDS]	When set to 1b, this bit indicates that the associated Port supports detection and reporting of two Retimers presence. This bit is valid for both Downstream Ports and Upstream Ports.	0x1
30:25	R	Reserved [R25]	Reserved	0x0
31	R	DRS Supported [R31]	Indicates support for the optional Device Readiness Status (DRS) capability. This capability is currently not supported in the Controller.	0x0

Link Control and Status 2 Register @0xf0

This register contains control and status bits specific to the PCI Express link.

Table 247: i_link_ctrl_status_2

Bits	SW	Name	Description	Reset
3:0	R/W	Target Link Speed [TLS]	This field sets the target speed when the software forces the link into Compliance mode by setting the Enter Compliance bit in this register (0001 = 2.5 GT/s, 0010 = 5 GT/s, 0011 = 8 GT/s, 0100 = 16 GT/s). The default value of this field is 0001 (2.5 GT/s) when the PCIE_GENERATION_SEL[1:0] strap pins of the Controller are set to 000, 0010 (5 GT/s) when the strap is set to 001, and 0011 (8 GT/s) when the strap pin is set to 010 , and 0100 (16 GT/s) when the strap pin is set to 011. STICKY.	0x4
4	R/W	Enter Compliance [EC]	This bit is used to force the Endpoint device to enter the Compliance mode. Software sets this bit to 1 and initiates a hot reset to force the device into the Compliance mode. The target speed for the Compliance mode is determined by the Target Link Speed field of this register. STICKY.	0x0

Bits	SW	Name	Description	Reset
5	R/W	Hardware Autonomous Speed Disable [HASD]	When this bit is set, the LTSSM is prevented from changing the operating speed of the link, other than reducing the speed to correct unreliable operation of the link. STICKY.	0x0
6	R/W	Selectable De-Emphasis [SD]	This bit selects the de-emphasis level when the Controller is operating at 5 GT/s (0 = -6 dB, 1 = -3.5 dB).	0x0
9:7	R/W	Transmit Margin [TM]	This field is intended for debug and compliance testing purposes only. It controls the non-de-emphasized voltage level at the transmitter outputs. Its encodings are: 000 = Normal operating range, 001 = 800 – 1200 mV for full swing and 400 – 700 mV for half swing, 010 – 111 = See PCI Express Base Specification 2.0. This field is reset to 0 when th LTSSM enters the Polling.Configuration substate during link training. STICKY.	0x0
10	R/W	Enter Modified Compliance [EMC]	This field is intended for debug and compliance testing purposes only. If this bit is set to 1, the device will transmit the Modified Compliance Pattern when the LTSSM enters the Polling.Compliance substate. STICKY.	0x0
11	R/W	Compliance SOS [CS]	When this bit is set to 1, the device will transmit SKP ordered sets between compliance patterns. STICKY.	0x0
15:12	R/W	Compliance De-Emphasis [CD]	This bit sets the de-emphasis level (for 5 GT/s operation) or the Transmitter Preset level (for 8 GT/s or 16 GT/s operation) when the LTSSM enters the Polling.Compliance state because of software setting the Enter Compliance bit in this register. It is used only when the link is running at either 5 GT/s, 8 GT/s, or 16 GT/s. At 5 GT/s, the only valid settings are 0 (-6 dB) and 1 (-3.5 dB). STICKY.	0x0
16	R	Current De-Emphasis Level [CDEL]	This status bit indicates the current operating de-emphasis level of the transmitter (0 = -6dB, 1 = -3.5dB).	0x1
17	R	Equalization 8.0 GT/s Complete [EQC]	This bit, when set to 1, indicates that the Transmitter Equalization procedure has completed. STICKY.	0x0
18	R	Equalization 8.0 GT/s Phase 1 Successful [EP1S]	This bit, when set to 1, indicates that the Phase 1 of the Transmitter Equalization procedure has completed successfully. STICKY.	0x0
19	R	Equalization 8.0 GT/s Phase 2 Successful [EP2S]	This bit, when set to 1, indicates that the Phase 2 of the Transmitter Equalization procedure has completed successfully. STICKY.	0x0
20	R	Equalization 8.0 GT/s Phase 3 Successful [EP3S]	This bit, when set to 1, indicates that the Phase 3 of the Transmitter Equalization procedure has completed successfully. STICKY.	0x0
21	R/WOCLR	Link Equalization Request 8.0 GT/s [LE]	When the Controller (RP) receives an 8 GTs equalization request from an Upstream Port the Controller internally sets this bit to 1 (i.e., when RP is in the Recovery.RcvrCfg state and receives eight consecutive TS2 Ordered Sets with the Request Equalization bit set to 1b). The LOCAL_INTERRUPT output is also asserted if Link Equalization Request Interrupt Enable is enabled.	0x0
22	R	Retimer Presence Detected [RTP]	When set to 1b, this bit indicates that a Retimer was present during the most recent Link negotiation.	0x0
23	R	Two Retimers Presence Detected [TWRTP]	When set to 1b, this bit indicates that two Retimers were present during the most recent Link negotiation.	0x0
27:24	R	Reserved [R21]	Reserved	0x0
30:28	R	Downstream Component Presence [DCP]	DRS is not supported by the Controller, hence this field is not implemented.	0x0
31	R	DRS Message Received [DMR]	DRS is not supported by the Controller, hence this field is not implemented.	0x0

Advanced Error Reporting (AER) Enhanced Capability Header Register @0x100

This is the first register in the PCI Express Advanced Error Reporting Capability Structure. This register contains the PCI Express Extended Capability ID, the capability version , and the pointer to the next capability structure.

Table 248: i_AER_enhncd_cap

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECID]	This field is hardwired to the Capability ID assigned by PCI SIG to the PCI Express AER Extended Capability Structure (0001 hex).	16'b0000000000000001
19:16	R	Capability Version [CV]	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 4'h2.	0x2
31:20	R	Next Capability Offset [NCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h150

Uncorrectable Error Status Register @0x104

This register provides the status of the various uncorrectable errors detected by the PCI Express Controller. Software may clear any error bit by writing a 1 into the corresponding bit position. The states of the bits in the Uncorrectable Error Mask Register have no effect on the status bits of this register. In the case of certain errors detected by the Transaction Layer, the associated TLP header is logged in the Header Log Registers.

Table 249: i_uncorr_err_status

Bits	SW	Name	Description	Reset
0	R/WOCLR	Link Training Error status [LTE]	This error indicates that link training is not successful and transition back to detect state. This Status bit is set on any LTSSM transition from Configuration to Detect or Recovery to Detect.	0x0
3:1	R	Reserved [R25]	(no description)	0x0
4	R/WOCLR	Data Link Protocol Error Status [DLPE]	This bit is set when the Controller receives an Ack or Nak DLLP whose sequence does not correspond to that of an unacknowledged TLP or that of the last acknowledged TLP (for details, refer to the PCI Express Base Specifications).	0x0
5	R/WOCLR	Surprise down error status [SDES]	This error status indicates Link up to Link down event. So Status bit is set upon LINK_DOWN_RESET_OUT event and if Surprise down Cap is enabled.	0x0
11:6	R	Reserved [R26]	Reserved	0x0
12	R/WOCLR	Poisoned TLP Status [PT]	This bit is set when the Controller receives a poisoned TLP from the link. This error is considered non-fatal by default. The header of the received TLP with error is logged in the Header Log Registers.	0x0
13	R/WOCLR	Flow Control Protocol Error Status [FCPE]	This bit is set when certain violations of the flow control protocol are detected by the Controller.	0x0
14	R/WOCLR	Completion Timeout Status [CT]	This bit is set when the completion timer associated with an outstanding request times out. This error is considered non-fatal by default.	0x0
15	R/WOCLR	Completer Abort Status [CA]	This bit is set when the Controller has returned the Completer Abort (CA) status to a request received from the link. This error is considered non-fatal by default, except for the special cases outlined in PCI Express Base Specification 2.0. The header of the received request that caused the error is logged in the Header Log Registers.	0x0

Bits	SW	Name	Description	Reset
16	R/WOCLR	Unexpected Completion Status [UC]	This bit is set when the Controller has received an unexpected Completion packet from the link.	0x0
17	R/WOCLR	Receiver Overflow Status [RO]	This bit is set when the Controller receives a TLP in violation of the receive credit currently available.	0x0
18	R/WOCLR	Malformed TLP Status [MT]	This bit is set when the Controller receives a malformed TLP from the link. This error is considered fatal by default. The header of the received TLP with error is logged in the Header Log Registers.	0x0
19	R/WOCLR	ECRC Error Status [EE]	This bit is set when the Controller has detected an ECRC error in a received TLP.	0x0
20	R/WOCLR	Unsupported Request Error Status [URE]	This bit is set when the Controller has received a request from the link that it does not support. This error is not Function-specific. This error is considered non-fatal by default, except for the special case outlined in PCI Express Base Specification 2.0. The header of the received request that caused the error is logged in the Header Log Registers.	0x0
21	R	Reserved [R27]	Reserved	0x0
22	R/WOCLR	Uncorrectable Internal Error Status [UIE]	This bit is set when the Controller has detected an internal uncorrectable error (HAL parity error or an uncorrectable ECC error while reading from any of the RAMs). This bit is also set in response to the client signaling an internal error through the input UNCORRECTABLE_ERROR_IN. This error is considered fatal by default.	0x0
31:23	R	Reserved [R28]	Reserved	0x0

Uncorrectable Error Mask Register @0x108

The mask bits in this register control the reporting of uncorrectable errors. For each error type in the Uncorrectable Error Status Register, there is a corresponding bit in this register to mask its reporting. Setting the mask bit has the following effects:

- The occurrence of the error does not cause activation of the FATAL_ERROR_OUT or NON_FATAL_ERROR_OUT output of the Controller, depending on the severity of the error.
- The header of the TLP in which the error was detected is not logged in the Header Log Registers.
- The First Error Pointer in the Advanced Error Capabilities and Control Register is not updated on the detection of the error. The individual bits of the mask register are described below.

Table 250: i_uncorr_err_mask

Bits	SW	Name	Description	Reset
0	R/W	Link Training Error Mask [LTEM]	This bit is set to mask the reporting of Link Training Error Mask. STICKY.	0x0
3:1	R	Reserved [R29]	Reserved	0x0
4	R/W	Data Link Protocol Error Mask [DLPER]	This bit is set to mask the reporting of Data Link Protocol Errors. STICKY.	0x0
5	R	Surprise Down Error Status Mask [SDESM]	This bit is set to mask the reporting of Surprise Down Error Status Mask. STICKY. If surprise down capability is enabled then it can be re-written else it is read only.	0x0
11:6	R	Reserved [R30]	Reserved	0x0
12	R/W	Poisoned TLP Mask [PTM]	This bit is set to mask the reporting of a Poisoned TLP. STICKY.	0x0
13	R/W	Flow Control Protocol Error Mask [FCPER]	This bit is set to mask the reporting of Flow Control Protocol Errors. STICKY.	0x0
14	R/W	Completion Timeout Mask [CTM]	This bit is set to mask the reporting of Completion Timeouts. STICKY.	0x0
15	R/W	Completer Abort Mask [CAM]	This bit is set to mask the reporting of the Controller sending a Completer Abort. STICKY.	0x0

Bits	SW	Name	Description	Reset
16	R/W	Unexpected Completion Mask [UCM]	This bit is set to mask the reporting of unexpected Completions received by the Controller. STICKY.	0x0
17	R/W	Receiver Overflow Mask [ROM]	This bit is set to mask the reporting of violations of receive credit. STICKY.	0x0
18	R/W	Malformed TLP Mask [MTM]	This bit is set to mask the reporting of malformed TLPs received from the link. STICKY.	0x0
19	R/W	ECRC Error Mask [EEM]	This bit is set to mask the reporting of ECRC errors. STICKY.	0x0
20	R/W	Unsupported Request Error Mask [UREM]	This bit is set to mask the reporting of unexpected requests received from the link. STICKY.	0x0
21	R	Reserved [R31]	Reserved	0x0
22	R/W	Uncorrectable Internal Error Mask [UIEM]	This bit is set to mask the reporting of internal errors. STICKY.	0x1
31:23	R	Reserved [R32]	Reserved	0x0

Uncorrectable Error Severity Register @0x10c

The setting of this register determines whether an uncorrectable error is reported as a fatal error or non-fatal; that is, whether the FATAL_ERROR_OUT or NON_FATAL_ERROR_OUT output of the Controller is activated. If a severity bit of this register is 0,the corresponding error is reported by the Controller by asserting NON_FATAL_ERROR_OUT. Otherwise, it is reported by asserting FATAL_ERROR_OUT.

Table 251: i_uncorr_err_severity

Bits	SW	Name	Description	Reset
0	R/W	Link Training Error Severity [LTES]	Severity of Link Training Error (0 = Non-Fatal, 1 = Fatal). STICKY.	0x0
3:1	R	Reserved [R33]	Reserved	0x0
4	R/W	Data Link Protocol Error Severity [DLPES]	Severity of Data Link Protocol Errors (0 = Non- Fatal, 1 = Fatal). STICKY.	1'b1
5	R	Surprise Down Error Severity [SDES]	Surprise down error severity (0 = Non-Fatal, 1 = Fatal). STICKY. If surprise down capability is enabled then it can be re-written else it is read only	1'b1
11:6	R	Reserved [R35]	Reserved	0x0
12	R/W	Poisoned TLP Severity [PTS]	Severity of a Poisoned TLP error (0 = Non-Fatal, 1 = Fatal). STICKY.	0x0
13	R/W	Flow Control Protocol Error Severity [FCPES]	Severity of a Flow Control Protocol Error (0 = Non-Fatal, 1 = Fatal). STICKY.	1'b1
14	R/W	Completion Timeout Severity [CTS]	Severity of Completion Timeouts (0 = Non-Fatal, 1 = Fatal). STICKY.	0x0
15	R/W	Completer Abort Severity [CAS]	Severity of sending a Completer Abort (0 = Non-Fatal, 1 = Fatal). STICKY.	0x0
16	R/W	Unexpected Completion Severity [UCS]	Severity of unexpected Completions received by the Controller (0 = Non-Fatal, 1 = Fatal). STICKY.	0x0
17	R/W	Receiver Overflow Severity [ROS]	Severity of receive credit violations (0 = Non-Fatal, 1 = Fatal). STICKY.	1'b1
18	R/W	Malformed TLP Severity [MTS]	Severity of malformed TLPs received from the link (0 = Non-Fatal, 1 = Fatal). STICKY.	1'b1
19	R/W	ECRC Error Severity [EES]	Severity of ECRC errors (0 = Non-Fatal, 1 = Fatal). STICKY.	0x0
20	R/W	Unsupported Request Error Severity [URES]	Severity of unexpected requests received from the link (0 = Non-Fatal, 1 = Fatal). STICKY.	0x0
21	R	Reserved [R36]	Reserved	0x0
22	R/W	Uncorrectable Internal Error Severity [Uncorr_Intrnl_Err_Svrty]	Severity of internal errors (0 = Non-Fatal, 1 = Fatal).	1'b1
31:23	R	Reserved [R37]	(no description)	0x0

Correctable Error Status Register @0x110

This register provides the status of the various correctable errors detected by the PCI Express Controller. Software may clear any error bit by writing a 1 into the corresponding bit position. The states of the bits in the Correctable Error Mask Register have no effect on the status bits of this register. The setting of a correctable error status bit causes the Controller to assert the CORRECTABLE_ERROR_OUT output if the error is not masked in the Correctable Error Mask Register. Header logging of received TLPs does not apply to correctable errors.

Table 252: i_corr_err_status

Bits	SW	Name	Description	Reset
0	R/WOCLR	Receiver Error Status [RES]	This bit is set when an error is detected in the receive side of the Physical Layer of the Controller (e.g., an 8b10b decode error).	0x0
5:1	R	Reserved [R37]	Reserved	0x0
6	R/WOCLR	Bad TP Status [BTS]	This bit is set when an error is detected in a received TLP by the Data Link Layer of the Controller. The conditions causing this error are: **1.** an LCRC error, **2.** the packet terminates with EDB symbol, but its LCRC field does not equal the inverted value of the calculated CRC.	0x0
7	R/WOCLR	Bad DLLP Status [BDS]	This bit is set when an LCRC error is detected in a received DLLP, and no errors were detected by the Physical Layer.	0x0
8	R/WOCLR	Replay Number Rollover Status [RNRS]	This bit is set when the replay count rolls over after three re-transmissions of a TLP at the Data Link Layer of the Controller.	0x0
11:9	R	Reserved [R38]	Reserved	0x0
12	R/WOCLR	Replay Timer Timeout Status [RTTS]	This bit is set when the replay timer in the Data Link Layer of the Controller times out, causing the Controller to re-transmit a TLP.	0x0
13	R/WOCLR	Advisory Non-Fatal Error Status [ANES]	This bit is set when an uncorrectable error occurs, which is determined to belong to one of the special cases described in the PCI Express Base Specification 2.0. This causes the Controller to assert the CORRECTABLE_ERROR_OUT output in place of NON_FATAL_ERROR_OUT.	0x0
14	R/WOCLR	Corrected Internal Error Status [CIES]	This bit is set when the Controller has detected an internal correctable error condition (a correctable ECC error while reading from any of the RAMs). This bit is also set in response to the client signaling an internal error through the input CORRECTABLE_ERROR_IN.	0x0
15	R/WOCLR	Header Log Overflow Status [HLOS]	This bit is set on a Header Log Register overflow, that is, when the header could not be logged in the Header Log Register because it is occupied by a previous header.	0x0
31:16	R	Reserved [R39]	Reserved	0x0

Correctable Error Mask Register @0x114

The mask bits in this register control the reporting of correctable errors. For each error type in the Correctable Error Status Register, there is a corresponding bit in this register to mask its reporting. When a mask bit is set the occurrence of the error is not reported (by asserting the CORRECTABLE_ERROR_OUT output).

Table 253: i_corr_err_mask

Bits	SW	Name	Description	Reset
0	R/W	Receiver Error Mask [REM]	This bit, when set, masks the reporting of Physical Layer errors. STICKY.	0x0
5:1	R	Reserved [R40]	Reserved	0x0

Bits	SW	Name	Description	Reset
6	R/W	Bad TP Mask [BTM]	This bit,when set, masks the reporting of an error in response to a 'Bad TLP' received. STICKY.	0x0
7	R/W	Bad DLLP Mask [BDM]	This bit, when set, masks the reporting of an error in response to a 'Bad DLLP' received. STICKY.	0x0
8	R/W	Replay Number Rollover Mask [RNRM]	This bit, when set, masks the reporting of an error in response to a Replay Number Rollover event. STICKY.	0x0
11:9	R	Reserved [R41]	Reserved	0x0
12	R/W	Replay Timer Timeout Mask [RTTM]	This bit, when set, masks the reporting of an error in response to a Replay Timer timeout event. STICKY.	0x0
13	R/W	Advisory Non-Fatal Error Mask [ANEM]	This bit, when set, masks the reporting of an error in response to an uncorrectable error occurence, which is determined to belong to one of the special cases in the PCI Express Base Specification 2.0. STICKY.	0x1
14	R/W	Corrected Internal Error Mask [CIEM]	This bit, when set, masks the reporting of an error in response to a corrected internal error condition. STICKY.	1'b1
15	R/W	Header Log Overflow Mask [HLOM]	This bit, when set, masks the reporting of an error in response to a Header Log register overflow. STICKY.	1'b1
31:16	R	Reserved [R42]	Reserved	0x0

Advanced Error Capabilities and Control Register @0x118

This register contains a pointer to the first error that is reported in the Uncorrectable Error Status Register, and bits to enable ECRC generation and checking.

Table 254: i_adv_err_cap_ctl

Bits	SW	Name	Description	Reset
4:0	R	First Error Pointer [FEP]	This is a 5-bit pointer to the bit position in the Uncorrectable Error Status Register corresponding to the error that was detected first. When there are multiple bits set in the Uncorrectable Error Status Register, this field informs the software which error was observed first. To prevent the field from being overwritten before the software is able to read it, this field is not updated while the status bit it points to in the Uncorrectable Error Status Register remains set. After the software clears this status bit, a subsequent error condition that sets any bit in the Uncorrectable Error Status Register will update the First Error Pointer. Any uncorrectable error type, including the special cases where the error is reported using an ERR_COR message, will set the First Error Pointer (assuming the software has reset the error pointed by it in the Uncorrectable Error Status Register). STICKY.	0x0
5	R	ECRC Generation Capability [EGC]	This read-only bit indicates to the software that the device is capable of generating ECRC in packets transmitted on the link.	0x1
6	R/W	Enable ECRC Generation [EEG]	Setting this bit enables the ECRC generation on the transmit side of the Controller. This bit is writable from the local management bus. STICKY.	0x0
7	R	ECRC Check Capability [ECC]	This read-only bit indicates to the software that the device is capable of checking ECRC in packets received from the link.	0x1
8	R/W	Enable ECRC Check [EEC]	Setting this bit enables ECRC checking on the receive side of the Controller. This bit is writable from the local management bus. STICKY.	0x0
9	R	Multiple Header Recording Capable [MHRC]	This bit is set when the RC has the capability to log more than one error header in its Header Log Registers. It is hardwired to 0.	0x0
10	R	Multiple Header Recording Enable [MHRE]	Setting this bit enables the RC to log multiple error headers in its Header Log Registers. It is hardwired to 0.	0x0

Bits	SW	Name	Description	Reset
11	R	Tlp Prefix Log Present [TPLP]	If Set and the First Error Pointer is valid, indicates that the TLP Prefix Log register contains valid information. If Clear or if First Error Pointer is invalid, the TLP Prefix Log register is undefined. Default value of this bit is 0. This bit is RsvdP if the End-End TLP Prefix Supported bit is ClF Set and the First Error Pointer is valid, indicates that the TLP Prefix Log register contains valid information. If Clear or if First Error Pointer is invalid, the TLP Prefix Log register is undefined.	0x0
31:12	R	Reserved [R43]	Reserved	0x0

Header Log Register 0 @0x11c

This is the first of a set of four registers used to capture the header of a TLP received by the Controller from the link upon detection of an uncorrectable error. When multiple bits are set in the Uncorrectable Error Status Register, the captured header corresponds the the error that was detected first, that is, the error pointed by the First Error Pointer. To prevent the captured header from being over-written before software is able to read it, this register is not updated while the status bit pointed to by the First Error Pointer in the Uncorrectable Error Status Register remains set. After the software clears this status bit, a subsequent error condition that sets any bit in the Uncorrectable Error Status Register will also cause the Header Log Registers to be updated. The doublewords of the TLP header are stored in the Header Log Registers with their bytes transposed. That is, the byte containing the Type/Format fields of the header is stored at bit positions 31:24 of the Header Log Register 0.

Table 255: i_hdr_log_0

Bits	SW	Name	Description	Reset
31:0	R	Header Dword 0 [HD0]	First Dword of captured TLP header. STICKY.	0x0

Header Log Register 1 @0x120

This register contains the second Dword of the captured TLP header. The bytes are stored in transposed order.

Table 256: i_hdr_log_1

Bits	SW	Name	Description	Reset
31:0	R	Header Dword 1 [HD1]	Second Dword of captured TLP header. STICKY.	0x0

Header Log Register 2 @0x124

This register contains the third Dword of the captured TLP header. The bytes are stored in transposed order.

Table 257: i_hdr_log_2

Bits	SW	Name	Description	Reset
31:0	R	Header Dword 2 [HD2]	Third Dword of captured TLP header. STICKY.	0x0

Header Log Register 3 @0x128

If the captured TLP header is four Dwords long, this register contains its fourth Dword. If the captured header is a three-Dword header, this register is unused. The bytes of the Dword are stored in this register in transposed order.

Table 258: i_hdr_log_3

Bits	SW	Name	Description	Reset
31:0	R	Header Dword 3 [HD3]	Fourth Dword of captured TLP header. STICKY.	0x0

Root Error Command Register @0x12c

This register contains bits that control how the RC responds to errors reported by remote devices.

Table 259: i_root_err_cmd

Bits	SW	Name	Description	Reset
0	R/W	Correctable Error Reporting Enable [CERE]	If this bit is set, the Controller will active its CORRECTABLE_ERROR_OUT output in response to an error message received from the link.	0x0
1	R/W	Non-Fatal Error Reporting Enable [NFERE]	If this bit is set, the Controller will active its NON_FATAL_ERROR_OUT output in response to an error message received from the link.	0x0
2	R/W	Fatal Error Reporting Enable [FERE]	If this bit is set, the Controller will active its FATAL_ERROR_OUT output in response to an error message received from the link.	0x0
31:3	R	Reserved [R44]	Reserved	0x0

Root Error Status Register @0x130

This register contains status information on error messages received from the link (that is, errors reported by remote devices attached to this Root Complex).

Table 260: i_root_err_stat

Bits	SW	Name	Description	Reset
0	R/WOCLR	Correctable Error Message Received [ECR]	This bit is set when the RC receives a Correctable error message from the link. STICKY	0x0
1	R/WOCLR	Multiple Correctable Error Messages Received [MECR]	This bit is set when the RC receives a Correctable error message from the link, if the ERR_COR received bit is already set. STICKY	0x0
2	R/WOCLR	Fatal/Non-Fatal Error Message Received [EFNR]	This bit is set when the RC receives either a Fatal or Non-Fatal error message from the link. STICKY	0x0
3	R/WOCLR	Multiple Fatal/ Non-Fatal Error Messages Received [MEFNR]	This bit is set when the RC receives either a Fatal or Non-Fatal error message from the link, and the ERR_FATAL/NONFATAL Received bit is already set. STICKY	0x0
4	R/WOCLR	First Uncorrectable Fatal [FUF]	This bit, when set, indicates that the first Uncorrectable error message received was for a Fatal error. STICKY	0x0
5	R/WOCLR	Non-Fatal Error Messages Received [NEMR]	This bit, when set, indicates that the RC has received one or more Non-Fatal error messages from the link. STICKY	0x0
6	R/WOCLR	Fatal Error Messages Received [FEMR]	This bit, when set, indicates that the RC has received one or more Fatal error messages from the link. STICKY	0x0
31:7	R	Reserved [R45]	Reserved	0x0

Error Source Identification Register @0x134

This register stores the Register IDs extracted from error messages received by the Root Complex from the link.

Table 261: i_err_src_id

Bits	SW	Name	Description	Reset
15:0	R	Correctable Error Message Source ID [ECSI]	This field captures and stores the Requester ID from an ERR_COR message received by the RC, if the ERR_COR bit was not set at the time the message was received. STICKY.	0x0
31:16	R	Fatal/Non-Fatal Error Message Source ID [EFNSI]	This field captures and stores the Requester ID from an ERR_FATAL or ERROR_NONFATAL message received by the RC, if the ERR_FATAL or NONFATAL Received bit was not set at the time the message was received. STICKY.	0x0

TLP Prefix Log Register 0 @0x138

First TLP Prefix (if present) associated with the TLP whose header is in the Header Log Register. The bytes are in transposed order.

Table 262: i_tlp_pre_log_0

Bits	SW	Name	Description	Reset
31:0	R	TLP Prefix 0 [HD1]	First TLP Prefix of captured TLP. STICKY.	0x0

Device Serial Number Capability Header Register @0x150

This register contains the PCI Express Extended Capability ID for Device Serial Number Capability, the capability version, and the pointer to the next capability structure.

Table 263: i_dev_ser_num_cap_hdr

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECID]	This field is hardwired to the Capability ID assigned by PCI SIG to the PCI Express Device Serial Number Capability (0001 hex).	0x03
19:16	R	Capability Version [DSNCV]	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus by writing into Function 0 from the local management bus.	0x01
31:20	R	Next Capability Offset [SNNCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h274

Device Serial Number Register 0 @0x154

This read-only register stored the first 32 bits of the device's serial number.

Table 264: i_dev_ser_num_0

Bits	SW	Name	Description	Reset
31:0	R	Device Serial Number, Doubleword 0 [DSND0]	This field contains the first 32 bits of the device's serial number. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0

Device Serial Number Register 1 @0x158

This read-only register stored the last 32 bits of the device's serial number.

Table 265: i_dev_ser_num_1

Bits	SW	Name	Description	Reset
31:0	R	Device Serial Number, Doubleword 1 [DSND1]	This field contains the last 32 bits of the device's serial number. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.	0x0

Secondary PCI Express Extended Capability Header Register @0x300

This register contains the PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability, its capability version, and the pointer to the next capability structure. This register is implemented only in the configuration space of PF 0 or RC.

Table 266: i_sec_pcie_cap_hdr_reg

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECI]	This field is hardwired to the Capability ID assigned by PCI SIG to the Secondary PCI Express Capability	0x019
19:16	R	Capability Version [CV]	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified independently for each PF from [the apb bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write].	0x1
31:20	R	Next Capability Offset [NCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h900

Link Control3 Register @0x304

This register is part of the Secondary PCI Express Extended Capability Structure. It contains bits to control the link equalization procedure at 8 GT/s or 16 GT/s speed.

Table 267: i_link_control3

Bits	SW	Name	Description	Reset
0	R/W	Perform Equaliztion [PE]	The state of this bit determines whether the Controller performs link equalization when the link is retrained by the local software. If this bit is set to 1 when the local software sets the Link Retrain bit in the Link Control Register, and the target link speed is 8 GT/s or 16 GT/s, the LTSSM of the Controller will go through the link equalization states during the retraining.	0x0
1	R/W	Link Equalization Request Interrupt Enable [LERIE]	This bit enables the activation of the LOCAL_INTERRUPT_OUT output of the Controller when the Link Equalization Request bit in the Link Status 2 Register Or the Link Equalization Request 16.0 GT/s in the 16GTs Status Register is set.	0x0
8:2	R	Reserved [R1]	Reserved	0x0
12:9	R/W	Enable Lower SKP OS Generation Vector [ELSOSGV]	When the Link is in L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture.	0x0
31:13	R	Reserved [R2]	Reserved	0x0

Lane Error Status Register @0x308

This register contains one bit per lane indicating the physical-layer error status of the corresponding lane. A 1 indicates that a physical-layer error was detected by the Controller

in the corresponding lane. The error can be cleared by writing a 1 into the bit position, either through a Configuration Write transaction from the link or from the local management APB bus.

Table 268: i_lane_error_status

Bits	SW	Name	Description	Reset
3:0	R/WOCLR	Lane Error Status [LES]	Each of these bits indicates the error status for the corresponding lane. STICKY.	0x0
31:4	R	Reserved [R0]	(no description)	0x0

Lane Equalization Control Register 0 @0x30c

This register contains the 8.0 GT/s Transmitter Preset and the Receiver Preset Hint values for lanes 0 and 1, for use during the Link Equalization procedure.

Table 269: i_lane_equalization_control_0

Bits	SW	Name	Description	Reset
3:0	R	Downstream Port 8.0 GT/s Transmitter Preset [DNTP0]	8.0 GT/s Transmitter Preset value to be used for the local transmitter associated with Lane 0. The Controller uses this value to set up the Lane 0 transmitter during link equalization.	0xF
6:4	R	Downstream Port 8.0 GT/s Receiver Preset Hint [DNRPH0]	8.0 GT/s Receiver Preset Hint value to be used for the local receiver associated with Lane 0. The Controller uses this value to set up the receiver attached to Lane 0.	0x7
7	R	Reserved [R0_1]	Reserved	0x0
11:8	R	Upstream Port 8.0 GT/s Transmitter Preset [UPTP0]	8.0 GT/s Value sent by the Controller as the Transmitter Preset for the remote transmitter associated with Lane 0. The remote node uses this value to set up its transmitter at the start of the link equalization procedure.	0xF
14:12	R	Upstream Port 8.0 GT/s Receiver Preset Hint [UPRPH0]	8.0 GT/s Value sent by the Controller as the Receiver Preset Hint for the remote receiver associated with Lane 0. The remote node may use this value to adapt its receiver at the start of the link equalization procedure.	0x7
15	R	Reserved [R1]	Reserved	0x0
19:16	R	Downstream Port 8.0 GT/s Transmitter Preset [DNTP1]	8.0 GT/s Transmitter Preset value to be used for the local transmitter associated with Lane 1. The Controller uses this value to set up the Lane 1 transmitter during link equalization.	0xF
22:20	R	Downstream Port 8.0 GT/s Receiver Preset Hint [DNRPH1]	8.0 GT/s Receiver Preset Hint value to be used for the local receiver associated with Lane 1. The Controller uses this value to set up the receiver attached to Lane 1	0x7
23	R	Reserved [R2_1]	Reserved	0x0
27:24	R	Upstream Port 8.0 GT/ s Transmitter Preset [UPTP1]	8.0 GT/s Value sent by the Controller as the Transmitter Preset for the remote transmitter associated with Lane 1. The remote node uses this value to set up its transmitter at the start of the link equalization procedure.	0xF
30:28	R	Upstream Port 8.0 GT/s Receiver Preset Hint [UPRPH1]	8.0 GT/s Value sent by the Controller as the Receiver Preset Hint for the remote receiver associated with Lane 1. The remote node may use this value to adapt its receiver at the start of the link equalization procedure.	0x7
31	R	Reserved [R3]	Reserved	0x0

Lane Equalization Control Register 1 @0x310

This register contains the 8.0GT/s Transmitter Preset and the Receiver Preset Hint values for lanes 2 and 3, for use during the Link Equalization procedure.

Table 270: i_lane_equalization_control_1

Bits	SW	Name	Description	Reset
3:0	R	Downstream Port 8.0 GT/s Transmitter Preset [DNTP0]	8.0 GT/s Transmitter Preset value to be used for the local transmitter associated with Lane 2. The Controller uses this value to set up the Lane 2 transmitter during link equalization.	0xF
6:4	R	Downstream Port 8.0 GT/s Receiver Preset Hint [DNRPH0]	8.0 GT/s Receiver Preset Hint value to be used for the local receiver associated with Lane 2. The Controller uses this value to set up the receiver attached to Lane 2	0x7
7	R	Reserved [R0_1]	Reserved	0x0
11:8	R	Upstream Port 8.0 GT/s Transmitter Preset [UPTP0]	8.0 GT/s Value sent by the Controller as the Transmitter Preset for the remote transmitter associated with Lane 2. The remote node uses this value to set up its transmitter at the start of the link equalization procedure.	0xF
14:12	R	Upstream Port 8.0 GT/s Receiver Preset Hint [UPRPH0]	8.0 GT/s Value sent by the Controller as the Receiver Preset Hint for the remote receiver associated with Lane 2. The remote node may use this value to adapt its receiver at the start of the link equalization procedure.	0x7
15	R	Reserved [R1]	Reserved	0x0
19:16	R	Downstream Port 8.0 GT/s Transmitter Preset [DNTP1]	8.0 GT/s Transmitter Preset value to be used for the local transmitter associated with Lane 3. The Controller uses this value to set up the Lane 3 transmitter during link equalization.	0xF
22:20	R	Downstream Port 8.0 GT/ s Receiver Preset Hint [DNRPH1]	8.0 GT/s Receiver Preset Hint value to be used for the local receiver associated with Lane 3. The Controller uses this value to set up the receiver attached to Lane 3	0x7
23	R	Reserved [R2_1]	Reserved	0x0
27:24	R	Upstream Port 8.0 GT/s Transmitter Preset [UPTP1]	8.0 GT/s Value sent by the Controller as the Transmitter Preset for the remote transmitter associated with Lane 3. The remote node uses this value to set up its transmitter at the start of the link equalization procedure.	0xF
30:28	R	Upstream Port 8.0 GT/s Receiver Preset Hint [UPRPH1]	8.0 GT/s Value sent by the Controller as the Receiver Preset Hint for the remote receiver associated with Lane 3. The remote node may use this value to adapt its receiver at the start of the link equalization procedure.	0x7
31	R	Reserved [R3]	Reserved	0x0

L1 PM Substates Extended Capability Header Register @0x900

L1 PM Substates Extended Capability Header Register.

Table 271: i_L1_PM_ext_cap_hdr

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PECID]	This field is hardwired to the Capability ID assigned by PCI SIG to the L1 PM Substates Extended Capability Structure (001E hex).	0x01e
19:16	R	Capability Version [CV]	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus.	0x01
31:20	R	Next Capability Offset [NCO]	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.	12'h910

L1 PM Substates Capabilities Register @0x904

This register advertises the L1 PM Substates Capabilities.

Table 272: i_L1_PM_cap

Bits	SW	Name	Description	Reset
0	R	PML1.2 Supported [L1PML12SUPP]	When Set this bit indicates that PCI-PM L1.2 is supported.	0x1
1	R	PML1.1 Supported [L1PML11SUPP]	When Set this bit indicates that PCI-PM L1.1 is supported.	0x1
2	R	ASPML1.2 Supported [L1ASPML12SUPP]	When Set this bit indicates that ASPM L1.2 is supported.	0x1
3	R	ASPML1.1 Supported [L1ASPML11SUPP]	When Set this bit indicates that ASPM L1.1 is supported.	0x1
4	R	L1 PM Substates Supported [L1PMSUPP]	When Set this bit indicates that this Port supports L1 PM Substates.	0x1
7:5	R	RSVD	RSVD	3'h0
15:8	R	Port Common Mode Restore Time [L1PrtCmMdReStrTime]	Time (in us) required for this Port to re-establish common mode during exit from PM or ASPM L1.2 substate.	8'hff
17:16	R	Port Power-On Time Scale [L1PrtPvrOnScale]	Specifies the scale used for the Port T_POWER_ON Value field in the L1 PM Substates Capabilities register. Range of Values: 00b = 2us, 01b = 10us, 10b = 100us, 11b = Reserved Default value is 00.	0x0
18	R	RSVD	RSVD	1'h0
23:19	R	Port Power-On Time Value [R0]	Along with the Port T_POWER_ON Scale field in the L1 PM Substates Capabilities register sets the time (in us) that this Port requires the port on the opposite side of Link to wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. The value of Port T_POWER_ON is calculated by multiplying the value in this field by the scale value in the Port T_POWER_ON Scale field in the L1 PM Substates Capabilities register. T Power On is the minimum amount of time that each component must wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. This is to ensure no device is ever actively driving into an unpowered component.	0xd
31:24	R	RSVD	RSVD	8'h00

L1 PM Substates Control 1 Register @0x908

L1 PM Substates Control 1 Register.

Table 273: i_L1_PM_ctrl_1

Bits	SW	Name	Description	Reset
0	R/W	PML1.2 Enable [L1PML12EN]	When Set this bit enables PCI-PM L1.2.	0x0
1	R/W	PML1.1 Enable [L1PML11EN]	When Set this bit enables PCI-PM L1.1.	0x0
2	R/W	ASPML1.2 Enable [L1ASPML12EN]	When Set this bit enables ASPM L1.2.	0x0
3	R/W	ASPML1.1 Enable [L1ASPML11EN]	When Set this bit enables ASPM L1.1.	0x0
7:4	R	RSVD	RSVD	4'h0
15:8	R/W	Common Mode Restore Time [L1CmMdReStrTtihmee]	Sets value of TCOMMONMODE (in us), which must be used by the Downstream Port for timing re-establishment of common mode. This field must only be modified when the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are both Clear. This field is reserved since both PCI-PM L1.2 and ASPM L1.2 are Not Supported in this configuration of the Controller.	0x0
25:16	R/W	LTR L1.2 Threshold Value [L1ThrshldVal]	Along with the LTR_L1.2_THRESHOLD_Scale, this field indicates the LTR threshold used to determine if entry into L1 results in L1.1 (if enabled) or L1.2 (if enabled).	0x0
28:26	R	RSVD	RSVD	3'h0

Bits	SW	Name	Description	Reset
31:29	R/W	LTR L1.2 Threshold Scale [L1ThrshldSc]	This field provides a scale for the value contained within the LTR_L1.2_THRESHOLD_Value. • 000 - Value times 1 ns • 001 - Value times 32 ns • 010 - Value times 1024 ns • 011 - Value times 32,768 ns • 100 - Value times 1,048,576 ns • 101 - Value times 33,554,422 ns • 110–111 - Not permitted.	0x0

L1 PM Substates Control 2 Register @0x90c

L1 PM Substates Control 2 Register.

Table 274: i_L1_PM_ctrl_2

Bits	SW	Name	Description	Reset
1:0	R/W	T_POWER_ON Scale [L1PwrOnSc]	Specifies the scale used for T_POWER_ON Value. Range of Values: • 00b = 2us • 01b = 10us • 10b = 100us • 11b = Reserved	0x0
2	R	RSVD	RSVD	1'h0
7:3	R/W	T_POWER_ON Value [L1PwrOnVal]	Along with the T_POWER_ON Scale sets the minimum amount of time (in us) that the Port must wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. T_POWER_ON is calculated by multiplying the value in this field by the value in the T_POWER_ON Scale field.	0x5
31:8	R	RSVD	RSVD	24'h000000

DL Feature Extended Capability Header Register @0x910

Data Link Feature Extended Capability Structure is used to configure the DL Feature mechanism.

Table 275: i_dl_feature_extended_capability_header_reg

Bits	SW	Name	Description	Reset
15:0	R	DL Feature Extended Capability ID [DLFCAPID]	Indicates that the associated extended capability structure is the DL Feature Extended Capability. This field returns a Capability ID of 0025h.	0x0025
19:16	R	DL Feature Capability Version [DLFCAPVER]	This field is a PCI SIG defined version number that indicates the version of the Capability structure present.	0x1
31:20	R	DL Feature Next Capability Offset [DLFNXCAP]	The offset to the next PCI Extended Capability structure.	12'h920

DL Feature Capabilities Register @0x914

Data Link Feature Capabilities Register.

Table 276: i_dl_feature_capabilities_reg

Bits	SW	Name	Description	Reset
0	R	Local Scaled Flow Control Supported [DLFCAPVER]	This bit indicates that this Port supports the Scaled Flow Control Feature.	0x1
30:1	R	Reserved [R0]	Reserved	0x0
31	R	DL Feature Exchange Enable [DLFEXEN]	If Set, this bit indicates that this Port will enter the DL_Feature negotiation state prior to Link Initialization.	0x1

DL Feature Status Register @0x918

Data Link Feature Status Register.

Table 277: i_dl_feature_status_reg

Bits	SW	Name	Description	Reset
0	R	Remote Scaled Flow Control Supported [RSFSUP]	This bit indicates that the Remote end Device supports the Scaled Flow Control Feature.	0x0
22:1	R	Reserved [R0]	Reserved	0x0
23	R	Reserved [R23]	Reserved	0x0
30:24	R	Reserved [R1]	Reserved	0x0
31	R	Remote Data Link Feature Supported Valid [RDLFSVAL]	This bit indicates that the Port has received a Data Link Feature DLLP in state DL_Feature (se3.2.1) and that the Remote Data Link Feature Supported and Remote Data Link Feature Ack fields are meaningful. This bit is Cleared on entry to state DL_Inactive. Default is 0b.	0x0

Margining Extended Capability Header Register @0x920

Margining Extended Capability Structure is used to configure the device for Receiver Margining.

Table 278: i_margining_extended_capability_header_reg

Bits	SW	Name	Description	Reset
15:0	R	Margining Extended Capability ID [MARCAPID]	Indicates that the associated extended capability structure is the Margining Extended Capability. This field returns a Capability ID of 0027h.	0x0027
19:16	R	Margining Capability Version [MARCAPVER]	This field is a PCI SIG defined version number that indicates the version of the Capability structure present.	0x1
31:20	R	Margining Next Capability Offset [MARNXCAP]	The offset to the next PCI Extended Capability structure.	12'h9c0

Margining Port Capabilities and Status Register @0x924

Margining Port Capabilities and Status Register.

Table 279: i_margining_port_capabilities_status_reg

Bits	SW	Name	Description	Reset
0	R	Margining uses Driver Software [MARUDS]	If Set, indicates that Margining is partially implemented using Device Driver software. Margining Software Ready indicates when this software is initialized. If Clear, Margining does not require device driver software. The Controller implementation requires driver software to initialize the Rx Margining parameter values in Local Management Registers for Lane Margining. Hence, the default value of this bit is set to 1.	0x1
15:1	R	Reserved [R0]	Reserved	0x0
16	R	Margining Ready [MRDY]	Indicates when the Margining feature is ready to accept margining commands. If the Margining uses Driver Software bit is 1, then the Controller sets this status bit when the Margining Software Ready bit is set and the Link is in Gen4 L0 state. If the Margining uses Driver Software bit is 0, then the Controller sets this status bit when the Link is in Gen4 L0 state.	0x0
17	R	Margining Software Ready [MSRDY]	When Margining uses Driver Software is Set, then this bit, when Set, indicates that the required software has performed the required initialization. The value of this bit is Undefined if Margining users Driver Software is Clear. The Controller implementation sets the default value of this bit to 0. The driver software must initialize the Rx Margining parameters in the Local Management Lane Margining Registers and then program this bit to 1.	0x0
31:18	R	Reserved [R1]	Reserved	0x0

Margining Lane Control and Status Register for Lane 0 @0x928

Margining Lane Control and Status Register for Lane 0.

Table 280: i_margining_lane_control_status_reg0

Bits	SW	Name	Description	Reset
2:0	R/W	Receiver Number [RCVNUM]	Receiver Number for Margining Commands. This field is reset upon DL Down.	0x0
5:3	R/W	Margin Type [MRGTYP]	Margin Type for Margining Commands. This field is reset upon DL Down.	0x7
6	R/W	Usage Model [USGMOD]	Usage Model for Margining Commands. This field is reset upon DL Down.	0x0
7	R	Reserved [R0]	Reserved	0x0
15:8	R/W	Margin Payload [MRGPAY]	Margin Payload for Margining Commands. This field is reset upon DL Down.	0x9C
18:16	R	Receiver Number Status [RNSTS]	Receiver Number Status for Margining Commands. This field is reset upon DL Down.	0x0
21:19	R	Margin Type Status [MTSTS]	Margin Type Status for Margining Commands. This field is reset upon DL Down.	0x0
22	R	Usage Model Status [UMSTS]	Usage Model Status for Margining Commands. This field is reset upon DL Down.	0x0
23	R	Reserved [R1]	Reserved	0x0
31:24	R	Margin Payload Status [MPSTS]	Margin Payload Status for Margining Commands. This field is reset upon DL Down.	0x0

Margining Lane Control and Status Register for Lane 1 @0x92c

Margining Lane Control and Status Register for Lane 1.

Table 281: i_margining_lane_control_status_reg1

Bits	SW	Name	Description	Reset
2:0	R/W	Receiver Number [RCVNUM]	Receiver Number for Margining Commands. This field is reset upon DL Down.	0x0
5:3	R/W	Margin Type [MRGTYP]	Margin Type for Margining Commands. This field is reset upon DL Down.	0x7
6	R/W	Usage Model [USGMOD]	Usage Model for Margining Commands. This field is reset upon DL Down.	0x0
7	R	Reserved [R0]	Reserved	0x0
15:8	R/W	Margin Payload [MRGPAY]	Margin Payload for Margining Commands. This field is reset upon DL Down.	0x9C
18:16	R	Receiver Number Status [RNSTS]	Receiver Number Status for Margining Commands. This field is reset upon DL Down.	0x0
21:19	R	Margin Type Status [MTSTS]	Margin Type Status for Margining Commands. This field is reset upon DL Down.	0x0
22	R	Usage Model Status [UMSTS]	Usage Model Status for Margining Commands. This field is reset upon DL Down.	0x0
23	R	Reserved [R1]	Reserved	0x0
31:24	R	Margin Payload Status [MPSTS]	Margin Payload Status for Margining Commands. This field is reset upon DL Down.	0x0

Margining Lane Control and Status Register for Lane 2 @0x930

Margining Lane Control and Status Register for Lane 2.

Table 282: i_margining_lane_control_status_reg2

Bits	SW	Name	Description	Reset
2:0	R/W	Receiver Number [RCVNUM]	Receiver Number for Margining Commands. This field is reset upon DL Down.	0x0
5:3	R/W	Margin Type [MRGTYP]	Margin Type for Margining Commands. This field is reset upon DL Down.	0x7
6	R/W	Usage Model [USGMOD]	Usage Model for Margining Commands. This field is reset upon DL Down.	0x0
7	R	Reserved [R0]	Reserved	0x0
15:8	R/W	Margin Payload [MRGPAY]	Margin Payload for Margining Commands. This field is reset upon DL Down.	0x9C
18:16	R	Receiver Number Status [RNSTS]	Receiver Number Status for Margining Commands. This field is reset upon DL Down.	0x0
21:19	R	Margin Type Status [MTSTS]	Margin Type Status for Margining Commands. This field is reset upon DL Down.	0x0
22	R	Usage Model Status [UMSTS]	Usage Model Status for Margining Commands. This field is reset upon DL Down.	0x0
23	R	Reserved [R1]	Reserved	0x0
31:24	R	Margin Payload Status [MPSTS]	Margin Payload Status for Margining Commands. This field is reset upon DL Down.	0x0

Margining Lane Control and Status Register for Lane 3 @0x934

Margining Lane Control and Status Register for Lane 3.

Table 283: i_margining_lane_control_status_reg3

Bits	SW	Name	Description	Reset
2:0	R/W	Receiver Number [RCVNUM]	Receiver Number for Margining Commands. This field is reset upon DL Down.	0x0
5:3	R/W	Margin Type [MRGTYP]	Margin Type for Margining Commands. This field is reset upon DL Down.	0x7
6	R/W	Usage Model [USGMOD]	Usage Model for Margining Commands. This field is reset upon DL Down.	0x0
7	R	Reserved [R0]	Reserved	0x0
15:8	R/W	Margin Payload [MRGPAY]	Margin Payload for Margining Commands. This field is reset upon DL Down.	0x9C
18:16	R	Receiver Number Status [RNSTS]	Receiver Number Status for Margining Commands. This field is reset upon DL Down.	0x0
21:19	R	Margin Type Status [MTSTS]	Margin Type Status for Margining Commands. This field is reset upon DL Down.	0x0
22	R	Usage Model Status [UMSTS]	Usage Model Status for Margining Commands. This field is reset upon DL Down.	0x0
23	R	Reserved [R1]	Reserved	0x0
31:24	R	Margin Payload Status [MPSTS]	Margin Payload Status for Margining Commands. This field is reset upon DL Down.	0x0

Physical Layer 16 GT/s Extended Capability Header Register @0x9c0

Physical Layer 16 GT/s Extended Capability Structure is used to configure the device for Gen4 Equalization and Gen4 Lane Error Reporting.

Table 284: i_pl_16gts_extended_capability_header_reg

Bits	SW	Name	Description	Reset
15:0	R	PCI Express Extended Capability ID [PL16CAPID]	Indicates that the associated extended capability structure is for Physical layer 16 GT/s. This field returns a Capability ID of 0026h.	0x0026
19:16	R	Capability Version [PL16CAPVER]	This field is a PCI SIG defined version number that indicates the version of the Capability structure present.	0x1
31:20	R	Next Capability Offset [PL16NXCAP]	The offset to the next PCI Extended Capability structure.	12'h0

Physical Layer 16GTs Capabilities Register @0x9c4

Physical Layer 16GTs Capabilities Register.

Table 285: i_pl_16gts_capabilities_reg

Bits	SW	Name	Description	Reset
31:0	R	Reserved [R0]	Reserved	0x0

Physical Layer 16GTs Control Register @0x9c8

Physical Layer 16GTs Control Register.

Table 286: i_pl_16gts_control_reg

Bits	SW	Name	Description	Reset
31:0	R	Reserved [R0]	Reserved	0x0

Physical Layer 16GTs Status Register @0x9cc

Physical Layer 16GTs Status Register.

Table 287: i_pl_16gts_status_reg

Bits	SW	Name	Description	Reset
0	R	Equalization 16.0 GT/s Complete [EQC16]	This bit, when set to 1, indicates that the Transmitter Equalization procedure has completed for 16.0 GT/s. STICKY.	0x0
1	R	Equalization 16.0 GT/s Phase 1 Successful [EP1S16]	This bit, when set to 1, indicates that the Phase 1 of the Transmitter Equalization procedure has completed successfully for 16.0 GT/s. STICKY.	0x0
2	R	Equalization 16.0 GT/s Phase 2 Successful [EP2S16]	This bit, when set to 1, indicates that the Phase 2 of the Transmitter Equalization procedure has completed successfully for 16.0 GT/s. STICKY.	0x0
3	R	Equalization 16.0 GT/s Phase 3 Successful [EP3S16]	This bit, when set to 1, indicates that the Phase 3 of the Transmitter Equalization procedure has completed successfully for 16.0 GT/s. STICKY.	0x0
4	R/WOCLR	Link Equalization Request 16.0 GT/s [LE16]	When the Controller (RP) receives an 16GTs equalization request from an Upstream Port the Controller internally sets this bit to 1 (i.e., when RP is in the Recovery.RcvrCfg state and receives eight consecutive TS2 Ordered Sets with the Request Equalization bit set to 1b). The LOCAL_INTERRUPT output is also asserted if Link Equalization Request Interrupt Enable is enabled.	0x0
31:5	R	R0	Reserved	0x0

Physical Layer 16GTs Local Data Parity Mismatch Status Register @0x9d0

Physical Layer 16GTs Local Data Parity Mismatch Status Register.

Table 288: i_pl_16gts_local_data_parity_mismatch_status_reg

Bits	SW	Name	Description	Reset
3:0	R/WOCLR	Local Data Parity Mismatch Status [LDPMS16]	Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number.	0x0
31:4	R	Reserved [R0]	(no description)	0x0

Physical Layer 16GTs First Retimer Data Parity Mismatch Status Register @0x9d4

Physical Layer 16GTs First Retimer Data Parity Mismatch Status Register.

Table 289: i_pl_16gts_first_retimer_data_parity_mismatch_status_reg

Bits	SW	Name	Description	Reset
3:0	R/WOCLR	First Retimer Data Parity Mismatch Status [FRDPMS16]	Each bit indicates if the first retimer in the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. The value of this field is undefined when no Retimers are present.	0x0
31:4	R	Reserved [R0]	(no description)	0x0

Physical Layer 16GTs Second Retimer Data Parity Mismatch Status Register @0x9d8

Physical Layer 16GTs Second Retimer Data Parity Mismatch Status Register.

Table 290: i_pl_16gts_second_retimer_data_parity_mismatch_status_reg

Bits	SW	Name	Description	Reset
3:0	R/WOCLR	Second Retimer Data Parity Mismatch Status [SRDPMS16]	Each bit indicates if the second retimer in the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. The value of this field is undefined when no Retimers are present.	0x0
31:4	R	Reserved [R0]	(no description)	0x0

Physical Layer 16GTs Reserved Register @0x9dc

Register at offset 1Ch in this capability is Reserved.

Table 291: i_pl_16gts_reserved_reg

Bits	SW	Name	Description	Reset
31:0	R	Reserved [R0]	Reserved	0x0

16 GT/s Lane Equalization Control Register 0 @0x9e0

This register contains the Downstream and Upstream Port 16.0 GT/s Transmitter Preset for lanes 0, 1, 2 and 3 that will be used for 16 GT/s Link Equalization procedure when this port is operating as a Downstream Port.

Table 292: i_pl_16gts_lane_equalization_control_reg0

Bits	SW	Name	Description	Reset
3:0	R	Lane 0 Downstream Port 16.0 GT/s Transmitter Preset [DPTP016]	Transmitter Preset used for 16.0 GT/s equalization by this Port when the Port is operating as a Downstream Port.	0xf
7:4	R	Lane 0 Upstream Port 16.0 GT/s Transmitter Preset [UPTP016]	16.0 GT/s Lane 0 Transmitter Preset value that the Downstream Port sends on the associated Lane to the Endpoint device during 16 GT/s Link Equalization.	0xf
11:8	R	Lane 1 Downstream Port 16.0 GT/s Transmitter Preset [DPTP116]	Transmitter Preset used for 16.0 GT/s equalization by this Port when the Port is operating as a Downstream Port.	0xf
15:12	R	Lane 1 Upstream Port 16.0 GT/s Transmitter Preset [UPTP116]	16.0 GT/s Lane 1 Transmitter Preset value that the Downstream Port sends on the associated Lane to the Endpoint device during 16 GT/s Link Equalization.	0xf
19:16	R	Lane 2 Downstream Port 16.0 GT/s Transmitter Preset [DPTP216]	Transmitter Preset used for 16.0 GT/s equalization by this Port when the Port is operating as a Downstream Port.	0xf

Bits	SW	Name	Description	Reset
23:20	R	Lane 2 Upstream Port 16.0 GT/s Transmitter Preset [UPTP216]	16.0 GT/s Lane 2 Transmitter Preset value that the Downstream Port sends on the associated Lane to the Endpoint device during 16 GT/s Link Equalization.	0xf
27:24	R	Lane 3 Downstream Port 16.0 GT/s Transmitter Preset [DPTP316]	Transmitter Preset used for 16.0 GT/s equalization by this Port when the Port is operating as a Downstream Port.	0xf
31:28	R	Lane 3 Upstream Port 16.0 GT/s Transmitter Preset [UPTP316]	16.0 GT/s Lane 3 Transmitter Preset value that the Downstream Port sends on the associated Lane to the Endpoint device during 16 GT/s Link Equalization.	0xf

Local Management Registers

The local management registers are used to configure various operational parameters associated with the core, and for a local processor to monitor its status. These registers are accessible only from the local management bus. The Local Management registers are listed in the sections below.

Physical Layer Configuration Register 0 @0x0

This register contains the configured parameters at the Physical Layer of the link, and status information from the Physical Layer.

Table 293: i_pl_config_0_reg

Bits	SW	Name	Description	Reset
0	R	Link Status [LS]	Current state of link (1 = link training complete, 0 = link training not complete).	0x0
2:1	R	Negotiated Lane Count [NLC]	Lane count negotiated with other side during link training (00 = x1, 01 = x2, 10 = x4, 11 = x8).	0x2
4:3	R	Negotiated Speed [NS]	Current operating speed of link (00 = 2.5G, 01 = 5G, 10 = 8G, 11 = 16G).	0x0
5	R	Link Training Direction [LTD]	The state of this bit indicates whether the Controller completed link training as an upstream port(Endpoint)(=0) or a downstream port(Root Port)(=1). Default value depends on CORE_TYPE strap pin.	0x1
6	R/W	Phy Error Reporting [APER]	This bit controls the reporting of Errors Detected by the PHY. The Errors Detected by the PHY include: • Received errors indicated on PIPE RxStatus interface • 8.0 GT/s Invalid Sync Header received error • 16.0 GT/s Invalid Sync Header received error If PHY Error Reporting bit is set to 0, the Controller will only report those errors that caused a TLP or DLLP to be dropped because of a Detected PHY Error. If PHY Error Reporting bit is set to 1, the Controller will report all Detected PHY Errors regardless of whether a TLP or DLLP was dropped. The following registers report PHY error in conjunction with this bit: • Correctable Error Status Register, i_corr_err_status, bit-0, Receiver Error Status • Local Error and StatusRegister, i_local_error_status_register, bit-7, Phy Error In addition to the Errors Detected by the PHY(PCS), the Controller detects the following Physical Layer Protocol Framing Errors: • Framing Errors in the received DLLP and TLP • Ordered Set Block Received Without EDS • Data Block Received After EDS • Illegal Ordered Set Block Received After EDS • Ordered Set Block Received After Skip OS *Note:* These Errors are always reported independent of the setting of this bit.	0x0
7	R/W	Tx Swing Setting [TSS]	This bit drives the PIPE_TX_SWING output of the Controller.	0x0
15:8	R	Received FTS Count for 2.5 GT/s speed [RFC]	FTS count received from the other side during link training for use at the 2.5 GT/s link speed. The Controller transmits this many FTS sequences while exiting the L0S state when operating at the 2.5 GT/s speed.	0x0
23:16	R	Received Link ID [RLID]	Link ID received from other side during link training.	0x0
29:24	R	LTSSM State [LTSSM]	Current state of the LTSSM. The encoding of the states is given in Appendix C.	0x0

Bits	SW	Name	Description	Reset
30	R	Remote Linkwidth Upconfigure Capability Status [R0]	A 1 in this field indicates that the remote node advertised Linkwidth Upconfigure Capability in the training sequences in the Configuration.Complete state when the link came up. A 0 indicates that the remote node did not set the Link Upconfigure bit.	0x0
31	R/W	Master Loopback Enable [MLE]	When the Controller is operating as a Root Port, setting this to 1 causes the LTSSM to initiate a loopback and become the loopback master. This bit is not used in the Endpoint Mode.	0x0

Physical Layer Configuration Register 1 @0x4

This register contains additional configured parameters at the Physical Layer of the link, and command bits for various Physical Layer functions.

Table 294: i_pl_config_1_reg

Bits	SW	Name	Description	Reset
7:0	R/W	Transmitted Link ID [TLI]	Link ID transmitted by the device in training sequences in the Root Port mode.	0x0
15:8	R/W	Transmitted FTS Count at 2.5 GT/s Speed[TFC1]	FTS count transmitted by the Controller in TS1/TS2 sequences during link training. This value must be set based on the time needed by thereceiver to acquire sync while exiting from L0S state.	0x80
23:16	R/W	Transmitted FTS Count at 5 GT/s Speed [TFC2]	FTS count transmitted by the Controller in TS1/TS2 sequences during link training. This value must be set based on the time needed by the receiver to acquire sync while exiting from L0S state.	0x80
31:24	R/W	Transmitted FTS Count at 8 GT/s Speed [TFC3]	FTS count transmitted by the Controller in TS1/TS2 sequences during link training. This value must be set based on the time needed by the receiver to acquire sync while exiting from L0S state.	0x80

Data Link Layer Timer Configuration Register @0x8

This register defines the replay timeout values used by the DL receive and transmit sides of the link. It can be read or written via the local management APB bus.

Table 295: i_dll_tmr_config_reg

Bits	SW	Name	Description	Reset
8:0	R/W	Transmit-Side Replay Timeout Adjustment [TSRT]	Additional transmit-side replay timer timeout interval. This 9-bit value is added as a signed 2's complement number to the internal replay timer timeout value computed by the Controller based on the PCI Express Specifications. This enables the user to make minor adjustments to the spec-defined replay timer settings. Its value is in multiples of (2 Symbol Times). At Gen1 adjustment range = (+2040 ns to -2048 ns). At Gen2 adjustment range = (+1020 ns to -1024 ns). At Gen3 adjustment range = (+510 ns to -512 ns).	0x0
15:9	R	Reserved [R9]	Reserved	0x0
24:16	R/W	Receive-Side ACK-NAK Replay Timeout Adjustment [RSART]	Additional receive side ACK-NAK timer timeout interval. This 9-bit value is added as a signed 2's complement number to the internal ACK-NAK timer timeout value computed by the Controller based on the PCI Express Specifications. This enables the user to make minor adjustments to the spec-defined replay timer settings.Its value is in multiples of (2 Symbol Times). At Gen1 adjustment range = (+2040 ns to -2048 ns). At Gen2 adjustment range = (+1020 ns to -1024 ns). At Gen3 adjustment range = (+510 ns to -512 ns).	0x0
31:25	R	Reserved [R25]	Reserved	0x0

Receive Credit Limit Register 0 VC0 @0xc

This register contains the initial credit limits advertised by the Controller during th DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize the DL for the modified settings to take effect. The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values. The default values are set to advertise the full size of the receive buffers. If a value of 0x00 is programmed, it implies infinite credit. *Note:* This may result in receiver overflow if received data is back pressured on the Client interface.

Table 296: i_rcv_cred_lim_0_reg

Bits	SW	Name	Description	Reset
11:0	R/W	Posted Payload Credit VC0 [PPC]	Posted payload credit limit advertised by the Controller for VC 0. This field is in units of four DWords, 16 DWords, or 64 DWords based on the Local Posted Payload Credit Scale for VC 0. • 00b => (units of four DWords), • 01b => (units of four DWords), • 10b => (units of 16 DWords), • 11b => (units of 64 DWords). *Note:*When Scaled FLow Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of four DW and then advertised in the InitFC DLLPs. **Caution:** The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.	0x0f8
19:12	R/W	Posted Header Credit VC0 [PHC]	Posted header credit limit advertised by the Controller for VC 0. This field is in units of one, four, or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 0. • 00b => (units of one Packet Header), • 01b => (units of one Packet Header), • 10b => (units of four Packet Headers), • 11b => (units of 16 Packet Headers). *Note:*When Scaled Flow Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of (one Packet Header) and then advertised in the InitFC DLLPs. *Note:* Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of End-End TLP Prefixes permitted in a TLP. **Caution:** The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.	0x20
31:20	R/W	Non-Posted Payload Credit VC0 [NPPC]	Non-Posted payload credit limit advertised by the Controller for VC 0. This field is in units of four DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 0. • 00b => (units of four DWords), • 01b => (units of four DWords), • 10b => (units of 16 DWords), • 11b => (units of 64 DWords). *Note:*When Scaled FLow Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of four DW and then advertised in the InitFC DLLPs. **Caution:** The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.	0x20

Receive Credit Limit Register 1 VC0 @0x10

This register contains the initial credit limits advertised by the Controller during the DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize

the DL for the modified settings to take effect. The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values. The default values are set to advertise the full size of the receive buffers. If a value of 0x00 is programmed, it implies infinite credit.

Note: This may result in receiver overflow if received data is back pressured on the Client interface.

Table 297: i_rcv_cred_lim_1_reg

Bits	SW	Name	Description	Reset
7:0	R/W	Non-Posted Header Credit Limit VC0 [NPHCL]	Non-Posted header credit limit advertised by the Controller for VC 0 (in number of packets). This field is in units of one, four, or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 0. • 00b => (units of one Packet Header) • 01b => (units of one Packet Header) • 10b => (units of four Packet Headers) • 11b => (units of 16 Packet Headers) *Note:* When Scaled FLow Control is Activated, the programmed credit value is advertised inthe InitFC DLLPs. Else, the programmed credit value is internally normalized to units of (one Packet Header) and then advertised in the InitFC DLLPs. *Note:* Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of End-End TLP Prefixes permitted in a TLP. **Caution:** The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.	0x20
19:8	R/W	Completion Payload Credit VC0 [CPC]	Completion payload credit limit advertised by the Controller for VC 0. This field is in units of four DWords, 16 DWords, or 64 DWords based on the Local Posted Payload Credit Scale for VC 0. • 00b => (units of four DWords) • 01b => (units of four DWords) • 10b => (units of 16 DWords) • 11b => (units of 64 DWords) *Note:*When Scaled FLow Control is Activated, the programmed creditvalue is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of four DW and then advertised in the InitFC DLLPs. **Caution:**The programmed Header andPayload credit values must not exceed the actual size of the Receive Buffer.	0x0
23:20	R	Reserved [R2]	Reserved	0x0
31:24	R/W	Completion Header Credit VC0 [CHC]	Completion header credit limit advertised by the Controller for VC 0 (in number of packets). This field is in units of one, four, or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 0. • 00b => (units of one Packet Header) • 01b => (units of one Packet Header) • 10b => (units of four Packet Headers) • 11b => (units of 16 Packet Headers) *Note:* When Scaled FLow Control is Activated, the programmed credit value is advertised inthe InitFC DLLPs. Else, the programmed credit value is internally normalized to units of (one Packet Header) and then advertised in the InitFC DLLPs. *Note:* Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of End-End TLP Prefixes permitted in a TLP. **Caution:** The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.	0x0

Transmit Credit Limit Register 0 VC0 @0x14

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

Table 298: i_transm_cred_lim_0_reg

Bits	SW	Name	Description	Reset
11:0	R	Posted Payload Credit VC0 [PPC]	Posted payload credit limit received by the Controller for this link. This field is in units of four DWords, 16 DWords, or 64 DWords based on the Remote Posted Payload Credit Scale for VC0. • 00b => (units of four DWords) • 01b => (units of four DWords) • 10b => (units of 16 DWords) • 11b => (units of 64 DWords)	0x0
19:12	R	Posted Header Credit VC0 [PHC]	Posted header credit limit received by the Controller for this link. This field is in units of one, four, or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 0. • 00b => (units of one Packet Header) • 01b => (units of one Packet Header) • 10b => (units of four Packet Headers) • 11b => (units of 16 Packet Headers) *Note:* Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of End-End TLP Prefixes permitted in a TLP.	0x0
31:20	R	Non-Posted Payload Credit VC0 [NPPC]	Non-Posted payload credit limit received by the Controller for Link 0. This field is in units of four DWords, 16 DWords, or 64 DWords based on the Remote Posted Payload Credit Scale for VC 0 • 00b => (units of four DWords) • 01b => (units of four DWords) • 10b => (units of 16 DWords) • 11b => (units of 64 DWords)	0x0

Transmit Credit Limit Register 1 VC0 @0x18

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

Table 299: i_transm_cred_lim_1_reg

Bits	SW	Name	Description	Reset
7:0	R	Non-Posted Header Credit VC0 [NPHC]	Non-Posted header credit limit received by the Controller for VC 0. This field is in units of one, four, or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 0. • 00b => (units of one Packet Header) • 01b => (units of one Packet Header) • 10b => (units of four Packet Headers) • 11b=> (units of 16 Packet Headers) *Note:* Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of End-End TLP Prefixes permitted in a TLP.	0x0
19:8	R	Completion Payload Credit VC0 [CPC]	Completion payload credit limit received by the Controller for VC 0. This field is in units of four DWords, 16 DWords, or 64 DWords based on the Remote Posted Payload Credit Scale for VC 0. • 00b => (units of four DWords) • 01b => (units of four DWords) • 10b => (units of 16 DWords) • 11b => (units of 64 DWords)	0x0
23:20	R	Reserved [R3]	Reserved	0x0

Bits	SW	Name	Description	Reset
31:24	R	Completion Header Credit VC0 [CHC]	Completion header credit limit received by the Controller for VC 0. This field is in units of one, four, or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 0. • 00b => (units of one Packet Header) • 01b => (units of one Packet Header) • 10b => (units of four Packet Headers) • 11b=> (units of 16 Packet Headers) *Note:* Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of End-End TLP Prefixes permitted in a TLP.	0x0

Transmit Credit Update Interval Configuration Register 0 @0x1c

This register contains parameters that control how frequently the Controller sends a credit update to the opposite node.

Table 300: i_transm_cred_update_int_config_0_reg

Bits	SW	Name	Description	Reset
15:0	R/W	Minimum Posted Update Interval [MPUI]	Minimum credit update interval for posted transactions. The Controller follows this minimum interval between issuing posted credit updates on the link to limit the bandwidth use of credit updates. If new credit becomes available in the receive FIFO since the last update was sent, the Controller will issue a new update only after this interval has elapsed since the last update. The value is in units of 16 ns. This field is re-written by the internal logic when the negotiated link width or link speed changes. The user may override this default value by writing into this register field. The value written will be lost on a change in the negotiated link width/speed.	16'd4
31:16	R/W	Minimum Non-PostedUpdate Interval [MNUI]	Minimum credit update interval for non-posted transactions. The Controller follows this minimum interval between issuing posted credit updates on the link. This is to limit the bandwidth use of credit updates. If new credit becomes available in the receive FIFO since the last update was sent, the Controller will issue a new update only after this interval has elapsed since the last update. The value is in units of 16 ns. This field is re-written by the internal logic when the negotiated link width or link speed changes. The user may override this default value by writing into this register field. The value written will be lost on a change in the negotiated link width/speed.	16'd4

Transmit Credit Update Interval Configuration Register 1 @0x20

This register contains parameters that control how frequently the Controller sends a credit update to the opposite node.

Table 301: i_transm_cred_update_int_config_1_reg

Bits	SW	Name	Description	Reset
15:0	R/W	Minimum Completion Update Interval [CUI]	Minimum credit update interval for Completion packets. The Controller follows this minimum interval between issuing completion credit updates on the link. This is to limit the bandwidth use of credit updates. If new credit becomes available in the receive FIFO since the last update was sent, the Controller will issue a new update only after this interval has elapsed since the last update. The value is in units of 16 ns. This parameter is not used when the Completion credit is infinity.	16'd4

Bits	SW	Name	Description	Reset
31:16	R/W	Maximum Update Interval [MUI]	Maximum credit update interval for all transactions. If no new credit has become available since the last update, the Controller will repeat the last update after this interval. This is to recover from any losses of credit update packets. The value is in units of 16 ns. This field could be re-written by the internal logic when the negotiated link width or link speed changes. The user may override this default value by writing into this register field. The value written will be lost on a change in the negotiated link width/speed.	16'd938

L0S Timeout Limit Register @0x24

This register defines the timeout value for transitioning to the L0S power state. If the transmit side has been idle for this interval, the Controller will transmit the idle sequence on the link and transition the state of the link to L0S .

Table 302: i_L0S_timeout_limit_reg

Bits	SW	Name	Description	Reset
15:0	R/W	L0S Timeout [LT]	Contains the timeout value (in units of 16 ns) for transitioning to the L0S power state. Setting this parameter to 0 permanently disables the transition to the L0S power state.	0x0177
31:16	R	Reserved [R4]	Reserved	0x0

Transmit TLP Count Register @0x28

This register contains the number of Transaction-Layer packets transmitted by the Controller on the link since the register was last reset. This counter saturates on reaching a count of all 1's. Writing all 1's to this register causes it to be reset to 0.

Table 303: i_transmit_tlp_count_reg

Bits	SW	Name	Description	Reset
31:0	R/WOCLR	Transmit TLP Count [TTC]	Count of TLPs transmitted.	0x0

Transmit TLP Payload Dword Count Register @0x2c

This register contains the aggregate number of payload double-words transmitted in Transaction-Layer Packets by the Controller on the link since the register was last reset. This counter saturates on reaching a count of all 1's. Writing all 1's to this register causes it to be reset to 0.

Table 304: i_transmit_tlp_payload_dword_count_reg

Bits	SW	Name	Description	Reset
31:0	R/WOCLR	Transmit TLP Payload Byte Count [TTPBC]	Count of TLPs payload Dwords transmitted.	0x0

Receive TLP Count Register @0x30

This register contains the number of Transaction-Layer packets received by the Controller from the link since the register was last reset. This counter saturates on reaching a count of all 1's. Writing all 1's to this register causes it to be reset to 0.

Table 305: i_receive_tlp_count_reg

Bits	SW	Name	Description	Reset
31:0	R/WOCLR	Receive TLP Count [RTC]	Count of TLPs received.	0x0

Receive TLP Payload Dword Count Register @0x34

This register contains the aggregate number of payload double-words received in Transaction-Layer packets by the Controller from the link since the register was last reset. This counter saturates on reaching a count of all 1's.

Writing all 1's to this register causes it to be reset to 0.

Table 306: i_receive_tlp_payload_dword_count_reg

Bits	SW	Name	Description	Reset
31:0	R/WOCLR	Receive TLP Payload Byte Count [RTPDC]	Count of TLP payload Dwords received.	0x0

Completion Timeout Limit Register 0 @0x38

This register contains the timeout value used to detect a completion timeout event for a request originated by the Controller from it master interface, when sub-range 1 is programmed in the Device Control 2 Register.

Table 307: i_compln_tmout_lim_0_reg

Bits	SW	Name	Description	Reset
15:0	R/W	Completion Timeout Limit [CTL]	Timeout limit for completion timers. This value is in multiples of 4096 ns. Default value is 50ms. Please note that there could be a variation of 0 to+8us on the programmed Completion Timeout.	16'd12207
23:16	R	RSVD	RSVD	8'h00
31:24	R	Reserved [R5]	Reserved	0x0

Completion Timeout Limit Register 1 @0x3c

This register contains the timeout value used to detect a completion timeout event for a request originated by the Controller from its master interface, when sub-range 2 is programmed in the Device Control 2 Register.

Table 308: i_compln_tmout_lim_1_reg

Bits	SW	Name	Description	Reset
15:0	R/W	Completion Timeout Limit [CTL]	Timeout limit for completion timers. This value is in multiples of 4096 ns. Default value is 200ms. Please note that there could be a variation of 0 to+8us on the programmed Completion Timeout.	16'd48_828
27:16	R	RSVD	RSVD	12'h000
31:28	R	Reserved [R6]	Reserved	0x0

L1 State Re-Entry Delay Register @0x40

This register specifies the time the Controller will wait before it re-enters the L1 state if its link partner transitions the link to L0 while all the Functions of the Controller are in D3 power state. The Controller will change the power state of the link from L0 to L1 if no activity is detected both

on the transmit and receive sides before this interval, while all Functions are in D3 state and the link is in L0. Setting this register to 0 disables re-entry to L1 state if the link partner returns the link to L0 from L1 when all the Functions of the Controller are in D3 state. This register controls only the re-entry to L1. The initial transition to L1 always occurs when all of the Functions of the Controller are set to the D3 state.

Table 309: i_L1_st_reentry_delay_reg

Bits	SW	Name	Description	Reset
31:0	R/W	L1 Re-Entry Delay [L1RD]	Delay to re-enter L1 after no activity (in units of 16 ns).	0x0

Vendor ID Register @0x44

This register contains the Vendor ID and Subsystem Vendor ID that the device advertises during its enumeration of the PCI configuration space.

Table 310: i_vendor_id_reg

Bits	SW	Name	Description	Reset
15:0	R/W	Vendor ID [VID]	Vendor ID	16'h17cd
31:16	R/W	Subsystem Vendor ID [SVID]	Subsystem Vendor ID	16'h17cd

ASPM L1 Entry Timeout Delay Register @0x48

This register defines the timeout value for transitioning to the L1 power state under Active State Power management. If the transmit side has been idle for this interval, the Controller will initiate a transition of its link to the L1 power state.

Table 311: i_aspm_L1_entry_tmout_delay_reg

Bits	SW	Name	Description	Reset
19:0	R/W	L1 Timeout [L1T]	Contains the timeout value(in units of 16 ns) for transitioning to the L1 power state. Setting it to 0 permanently disables the transition to the L1 power state.	20'd750
30:20	R	Reserved [R7]	Reserved	0x0
31	R/W	Disable Check for LinkRX IDLE [DISLNRXCHK]	This bit is used to configure the ASPM L1 Entry mechanism: • 1: Link is checked for IDLE only on the TX to determine ASPM L1 Entry. ASPM L1 entry is initiated if no TLP is transmitted for the L1 timeout period. • 0: Link is checked for IDLE both on the TX and RX to determine ASPM L1 Entry. ASPM L1 entry is initiated if no TLP is transmitted/received for the L1 timeout period.	0x0

PME TurnOff Ack Delay Register @0x4c

Defines the time interval between the Controller receiving a PME_Turn_Off message from the link and generating an ack for it.

Table 312: i_pme_turnoff_ack_delay_reg

Bits	SW	Name	Description	Reset
15:0	R/W	PME Turnoff Ack Delay [PTOAD]	Time in microseconds between the Controller receiving a PME_TurnOff message TLP and the Controller sending a PME_TO_Ack response to it. This field must be set to a non-zero value in order for the Controller to send a response. Setting this field to 0 suppresses the Controller's response to PME_TurnOff message, so that the client may transmit the PME_TO_Ack message through the master interface.	0x64
31:16	R	Reserved [R7]	Reserved	0x0

Linkwidth Control Register @0x50

This register can be used to re-train the link to a different width without bringing the link down. This register can also be used to re-train the link to a different speed without bringing the link down.

Table 313: i_linkwidth_control_reg

Bits	SW	Name	Description	Reset
3:0	R/W	Target Lane Map [TLM]	This field contains the bitmap of the lanes to be included in forming the link during the re-training. • 0001 - Retrain to a x1 link • 0011 - Retrain to ax2 link • 1111 - Retrain to a x4 link If the target lane map includes lanes that were inactive when re-training is initiated, then both the Controller and its link partner must support the LinkWidth Upconfigure Capability to be able to activate those lanes. In RC Mode, the user can check if the remote node has this capability by reading the Remote Link Upconfigure Capability Status bit in Physical Layer Configuration Register 0 after the link first came up.	4'b1111
15:4	R	Reserved [R0]	Reserved	0x0
16	R/W	Link Upconfigure Retrain Link [RL]	Writing a 1 into this field results in the Controller re-training the link to change its width. When setting this bit to 1, the software must also set the target lane-map field to indicate the lanes it desires to be part of the link. The Controller will attempt to form a link with this set of lanes. The link formed at the end of the retraining may include all of these lanes (if both nodes agree on them during re-training), or the largest subset that both sides were able to activate. This bit is cleared by the internal logic of the Controller after the re-training has been completed and link has reached the L0 state. Software must wait for the bit to be clear before setting it again to change the link width. *NOTE:* LINK WIDTH CHANGE FEATURE IS BEING DEPRECATED. FOR POWER SAVING, IT IS RECOMMENDED TO USE L1.	0x0
17	R/W	Disable Auto Gen2 Speed Change [DSAG2SC]	This bit is used Only in RP mode. This bit is not used in EP mode of the Controller. During initial link training, if both components advertise Gen2 capability and if Gen2 is the highest common supported speed the Controller (RP) autonomously initiates Gen1 to Gen2 speed change. If Gen2 autonomous speed change was unsuccessful, then the Link transitions back to Gen1 L0. Software can re-initiate Gen2 speed change. Autonomous Speed Change to Gen2 can be disabled by programming this bit to 1.	0x0
18	R/W	Disable Auto Gen3 Speed Change [DSAG3SC]	This bit is used Only in RP mode. This bit is not used in EP mode of the Controller. During initial link training, if both components advertise Gen3 capability, the Controller (RP) autonomously initiates Gen1 to Gen3 speed change, equalization. If Gen3 autonomous speed change/equalization was unsuccessful, then the Link transitions back to Gen1 L0. Software can re-initiate Gen3 speed change. Autonomous Speed Change to Gen3 can be disabled by programming this bit to 1.	0x0

Bits	SW	Name	Description	Reset
19	R/W	Disable Auto Gen4 Speed Change [DSAG4SC]	This bit is used Only in RP mode. This bit is not used in EP mode of the Controller. During initial link training, if both components advertise Gen4 capability and if Gen3 speed change, equalization was successful, the Controller (RP) autonomously initiates Gen3 to Gen4 speed change, equalization. If Gen4 autonomous speed change/equalization was unsuccessful, then the Link transitions back to Gen3 L0. Software can re-initiate Gen4 speed change. Autonomous Speed Change to Gen4 can be disabled by programming this bit to 1. *Note:* IfDisable Auto Gen3 Speed Change is disabled, then Auto Gen4 Speed Change must also be disabled by setting this bit to 1.	0x0
20	R/W	Disable Auto Gen5 Speed Change [DSAG5SC]	This bit is used Only in RP mode. This bit is not used in EP mode of the Controller. During initial link training, if both components advertise Gen5 capability and if Gen4 speed change, equalization was successful, the Controller (RP) autonomously initiates Gen4 to Gen5 speed change, equalization. If Gen5 autonomous speed change/equalization was unsuccessful, then the Link transitionsback to Gen4 L0. Software can re-initiate Gen5 speed change. Autonomous Speed Change to Gen5 can be disabled by programming this bit to 1. *Programming Note1:* When either (No Eq Capable) Or (Equalization Bypass to Highest Rate)Support is advertised in pl_32gts_capabilities_reg, then the i_linkwidth_control_reg[20:17] must be (4'b0000) or (4'b1110) or (4'b1111). *Programming Note2:* When both (No Eq Capable) and (Equalization Bypass to Highest Rate) Supportare Not advertised in pl_32gts_capabilities_reg, then the i_linkwidth_control_reg[20:17] must be (4'b0000) or (4'b1000) or (4'b1100) or (4'b1110) or (4'b1111).	0x0
23:21	R	Reserved [R21]	Reserved	0x0
26:24	R/W	EP Target Link Speed [EPTLS]	This field contains the Link Speed that the EP intends to change to during the re-training. Client needs to ensure that this field is programmedto a speed which is lesser than or equal to the Target Link Speed field of PF0 Configuration Link Control 2 Register. Client also needs to ensure that this does not exceed PCIE_GENERATION_SEL strap input. Defined encodings of this field are: • 000 - GEN1 • 001 - GEN2 • 010 - GEN3 • 011 - GEN4 • 100 - Reserved	0x0
30:27	R	Reserved [R2]	Reserved	0x0
31	R/W	EP Link Speed Change Retrain Link [EPLSCRL]	Writing a 1 into this field results in the Controller re-training the link to change its speed. When setting this bit to 1, the software must also setthe EP Target Link Speed field to indicate the speed that the EP desires to change on the link. The EP Controller will attempt to change the link to this speed. This bit is cleared by the internal logic of the Controller after the re-training has been completed and link has reached the L0 state. Software must wait for the bit to be clear before setting it again to change the link speed.	0x0

Physical Layer Configuration Register 2 @0x54

This register controls various LTSSM related capabilities.

Table 314: i_pl_config_2_reg

Bits	SW	Name	Description	Reset
0	R/W	Link Training Enable Software Control [LK_TRN]	This bit is AND'ed with the input LINK_TRAINING_ENABLE strap to enable Link Training.	1'b1
2:1	R/W	Detect Quiet Minimum Delay Control [DQMDC]	As per PCIe specification, All Receivers must meet the the Z-RX-DC specification for 2.5 GT/s within 1ms of entering Detect.Quiet LTSSM substate. The LTSSM must stay in this substate until the ZRX- DC specification for 2.5 GT/s is met. This register field can be used to program the minimum time that LTSSM waits on entering Detect.Quiet state. • 00 : 0us minimum wait time in Detect.Quiet state. • 01 : 100us minimum wait time in Detect.Quiet state. • 10 : 1ms minimum wait time in Detect.Quiet state. • 11 : 2ms minimum wait time in Detect.Quiet state.	2'b01
3	R	Reserved [R3]	Reserved	0x0
7:4	R/W	RX Electrical Idle Min Delay [RXEIMD]	Minimum time that the Receive logic will stay in Idle after receiving EIOS, before checking for RX electrical idle exit sequences such as EIEOS/TS1/FTS. This is used to prevent spurious receive data from causing an exit after EIOS is received. Register value indicates the minimum delay in units of 16 ns. All received data will be ignored for the programmed Min Delay. Default value is 3.	4'b0011
8	R/W	Disable Extended Speed Change Delay [DESCD]	After changing the speed, the LTSSM waits for phy_status response from PHY. This field is used to control the maximum time the LTSSM waits for the response. • 0 : 4 ms maximum time LTSSM waits in Recovery.Speed for PHY STATUS response • 1 : 1 ms maximum time LTSSM waits in Recovery.Speed for PHY STATUS response	1'b0

14:9	R/W	Disable Enhanced TS Symbol Consecutive Check [DTSSCC]	The Controller LTSSM checks symbols of the received TS OS to match to determine if the TS are consecutive. This field can be used to turn off this check.
			• Bit-0:
			  — 0 : Enable symbol 1 consecutive check in TS OS
			  — 1 : Disable symbol 1 consecutive check
			• Bit-1:
			  — 0 : Enable symbol 2 consecutive check in TS OS
			  — 1 : Disable symbol 2 consecutive check
			• Bit-2:
			  — 0 : Enable symbol 3 consecutive check in TS OS
			  — 1 : Disable symbol 3 consecutive check
			• Bit-3:
			  — 0 : Enable symbol 4 consecutive check in TS OS
			  — 1 : Disable symbol 4 consecutive check
			• Bit-4:
			  — 0 : Enable symbol 5 consecutive check in TS OS
			  — 1 : Disable symbol 5 consecutive check
			• Bit-5:
			  — 0 : Enable symbol 6,7,8,9 consecutive checks in TS in all states at Gen3 and higher and Symbol 6 consecutive checks in all states at Gen1,2
			  — 1 : Enable symbol 6,7,8,9 consecutive checks in TS only in Equalization states at Gen3 and higher
				0x0

15	R	Reserved [R15]	Reserved	0x0

Bits	SW	Name	Description	Reset
16	R/W	Disable Rate Identifier ConsecutiveCheck [DRICC]	The Data Rate supported by remote end is advertised in the received TS1/TS2. The advertised data rates are captured by the Controller in eight consecutive TS1s/TS2s in various LTSSM states. This field can be used to disable waiting for eight consecutive TS1/TS2 and capture based on every TS1/TS2 in Recovery and Configuration. • 0 : Wait for eight consecutive TS1/TS2 and capture advertised data rates • 1 : Capture advertised data rates from every TS1/TS2 in Recovery and Configuration States	1'b0
17	R/W	Disable Electrical Idle Data Blank [DEIDB]	During entry into RX Electrical Idle, an EIOS is received. Controller is required to ignore any receive data after EIOS. The receive data after EIOS is blanked by the Controller by default. Setting this bit to 1 disables data blanking and allows spurious receive data after EIOS. This bit must be 0 for functional modes. • 0 : Blank RX Data after EIOS, till a valid electrical idle exit • 1 : Do not blank RX Data after EIOS	1'b0
31:18	R	Reserved [R18]	Reserved	0x0

SRIS Control Register @0x74

This register contains control bits to enable the SRIS operation in the PHY Layer

Table 315: i_sris_control_reg

Bits	SW	Name	Description	Reset
0	R/W	SRIS Enable [SRISE]	Setting this bit enables SRIS mode in the PHY layer. This bit should be changed before link training begins by holding theLINK_TRAINING_ENABLE input to 1'b0. When SRIS is disabled using this bit the Lower SKP OS Generation Supported Speeds Vector and Lower SKP OS Reception Supported Speeds Vector in the Link Capabilities Register 2 will be forced to ZERO. The default value of this register can be controlled using the SRIS_ENABLE strap input.	0x0
31:1	R	Reserved [R31]	Reserved	0x0

Shadow Register Header Log 0 @0x100

Table 316: i_shdw_hdr_log_0_reg

Bits	SW	Name	Description	Reset
31:0	R/W	Shadow header log 0[SHDW_HDR_LOG_0]	The value here will be reflected in the target function's header log register when f/w sets any bit in the shadow error register. If the header log is already set in the function's AER space, the value here may not get written and a header log overflow bit would get set. This register holds [31:0] value of the TLP header.	0x0

Shadow Register Header Log 1 @0x104

(no description)

Table 317: i_shdw_hdr_log_1_reg

Bits	SW	Name	Description	Reset
31:0	R/W	Shadow header log 1[SHDW_HDR_LOG_1]	The value here will be reflected in the target function's header log register when f/w sets any bit in the shadow error register. If the header log is already set in the function's AER space, the value here may not get written and a header log overflow bit would get set. This register holds [63:32] value of the TLP header.	0x0

Shadow Register Header Log 2 @0x108

(no description)

Table 318: i_shdw_hdr_log_2_reg

Bits	SW	Name	Description	Reset
31:0	R/W	Shadow header log 2[SHDW_HDR_LOG_2]	The value here will be reflected in the target function's header log register when f/w sets any bit in the shadow error register. If the header log is already set in the function's AER space, the value here may not get written and a header log overflow bit would get set. This register holds [95:64] value of the TLP header.	0x0

Shadow Register Header Log 3 @0x10c

Table 319: i_shdw_hdr_log_3_reg

Bits	SW	Name	Description	Reset
31:0	R/W	Shadow header log 3 [SHDW_HDR_LOG_3]	The value here will be reflected in the target function's header log register when f/w sets any bit in the shadow error register. If the header log is already set in the function's AER space, the value here may not get written and a header log overflow bit would get set. This register holds [127:96] value of the TLP header.	0x0

Shadow Register Function Number @0x110

Table 320: i_shdw_func_num_reg

Bits	SW	Name	Description	Reset
7:0	R/W	Shadow register target function number [SHDW_FUNC_NUM]	The value here will be the target function number when f/w sets any bit in the shadow error register.	0x0
31:8	R	Reserved [R0]	Reserved	0x0

Shadow Register UR Error @0x114

Shadow register to create UR error via local f/w. Please make sure this register is written to last, after writing to all the header log and function number registers. A write to this register with any bits set, will internally create a single cycle pulse with the corresponding error type and the header log will reflect the value written in the shadow header log registers.

Table 321: i_shdw_ur_err_reg

Bits	SW	Name	Description	Reset
0	W	Posted UR Error[P_UR_ERR]	If this bit is set, the corresponding posted UR error bits will be set in the AER and device status registers of the target function.	0x0

Bits	SW	Name	Description	Reset
1	W	Non Posted Error [NP_UR_ERR]	If this bit is set, the corresponding non-posted UR error bits will be set in the AER and device status registers of the target function.	0x0
31:2	R	Reserved [R0]	Reserved	0x0

PM_CLK Frequency Register @0x140

This register should be programmed with the frequency of the PM_CLK input to the Controller. The Controller supports the frequency range of 2 MHz to 60 MHz for PM_CLK. The reset value reflects the PM_CLK frequency chosen during Controller configuration.

NOTE: PM_CLK will be timed at 60 Mhz and the Controller SDC file will be generated accordingly. If timing is to be closed at a different frequency, then the user needs to update the SDC accordingly.

Table 322: i_pm_clk_frequency_reg

Bits	SW	Name	Description	Reset
7:0	R/W	PM_CLKFrequency Select [PMCLKFRQ]	This field specifies the PM_CLK Frequency selected. The encoding is described below: • 000000: Reserved • 000001: Reserved • 000010: PM_CLK is 2 MHz • 000011: PM_CLK is 3 MHz • 000100: PM_CLK is 4 MHz • 000101: PM_CLK is 5 MHz • 111010: PM_CLK is 58 MHz • 111011: PM_CLK is 59 MHz • 111100: PM_CLK is 60 MHz • 111101: Reserved • 111110: Reserved • 111111: Reserved	8'd25
31:8	R	Reserved [R0]	Reserved	0x0

DL GEN1 Receive DLLP Count Debug Register @0x144

This register indicates the total number of DLLPs received by the Controller in GEN1. This counter rolls over back to 0 after 4G DLLPs are received. This register can be used for Debug purposes.

Table 323: i_debug_dllp_count_gen1_reg

Bits	SW	Name	Description	Reset
31:0	R	GEN1DLLP Count [DLLPCNT1]	Reflects the total number of DLLPs received by the Controller at GEN1 speed.	0x0

DL GEN2 Receive DLLP Count Debug Register @0x148

This register indicates the total number of DLLPs received by the Controller in GEN2. This counter rolls over back to 0 after 4G DLLPs are received. This register can be used for Debug purposes.

Table 324: i_debug_dllp_count_gen2_reg

Bits	SW	Name	Description	Reset
31:0	R	GEN2DLLP Count [DLLPCNT2]	Reflects the total number of DLLPs received by the Controller at GEN2 speed.	0x0

DL GEN3 Receive DLLP Count Debug @0x14c

This register indicates the total number of DLLPs received by the Controller in GEN3. This counter rolls over back to 0 after 4G DLLPs are received. This register can be used for Debug purposes.

Table 325: i_debug_dllp_count_gen3_reg

Bits	SW	Name	Description	Reset
31:0	R	GEN3DLLP Count [DLLPCNT3]	Reflects the total number of DLLPs received by the Controller at GEN3 speed.	0x0

DL GEN4 Receive DLLP Count Debug Register @0x150

This register indicates the total number of DLLPs received by the Controller in GEN4. This counter rolls over back to 0 after 4G DLLPs are received. This register can be used for Debug purposes.

Table 326: i_debug_dllp_count_gen4_reg

Bits	SW	Name	Description	Reset
31:0	R	GEN4DLLP Count [DLLPCNT4]	Reflects the total number of DLLPs received by the Controller at GEN4 speed.	0x0

Vendor Defined Message Tag Register @0x158

The 8-bit Tag field of the Outbound Vendor Defined Messages, transmitted by the Controller, can be programmed in this register.

Table 327: i_vendor_defined_message_tag_reg

Bits	SW	Name	Description	Reset
7:0	R/W	Vendor Defined Message Tag [VDMTAG]	The Controller will use the tag programed in this register for all Outbound Vendor Defined Messages.	0x0
31:8	R	RSVD	RSVD	24'h000000

Negotiated Lane Map Register @0x200

This register contains a map of the active lanes used by the Controller to form the link during link training. It also contains a bit to indicate whether the Controller reversed the lane number on its lanes during link training.

Table 328: i_negotiated_lane_map_reg

Bits	SW	Name	Description	Reset
3:0	R	Negotiated Lane Map [NLM]	Bit i of this field is set to 1 at the end of link training if Lane i is part of the PCIe link. The value of this field is valid only when the link is in L0 or L0s states.	0x0
15:4	R	Reserved [R70]	Reserved	0x0
16	R	Lane Reversal Status [LRS]	This bit set by the Controller at the end of link training if the LTSSM had to reverse the lane numbers to form the link.	0x0
31:17	R	Reserved [R71]	Reserved	0x0

Receive FTS Count Register @0x204

This register contains the FTS count values received from the link partner during link training for use at the 5 GT/s, 8 GT/s, and 16 GT/s speeds. These values determine the number of Fast Training Sequences transmitted by the Controller when it exits the L0s link power state.

Table 329: i_receive_fts_count_reg

Bits	SW	Name	Description	Reset
7:0	R	Received FTS Count for 5GT/s Speed [RFC5S]	FTS count received from the other side during link training for use at the 5 GT/s link speed. The Controller transmits this many FTS sequenceswhile exiting the L0S state, when operating at the 5 GT/s speed.	0x0
15:8	R	Received FTS Count for 8GT/s Speed [RFC8S]	FTS count received from the other side during link training for use at the 8 GT/s link speed. The Controller transmits this many FTS sequenceswhile exiting the L0S state, when operating at the 8 GT/s speed.	0x0
23:16	R	Received FTS Count for 16GT/s Speed [RFC16S]	FTS count received from the other side during link training for use at the 16 GT/s link speed. The Controller transmits this many FTS sequences while exiting the L0S state, when operating at the 16 GT/s speed.	0x0
31:24	R	Reserved [R24]	Reserved	0x0

Debug Mux Control Register @0x208

Table 330: i_debug_mux_control_reg

Bits	SW	Name	Description	Reset
4:0	R/W	Reserved	Reserved	0x0
6:5	R	Reserved [R6]	Reserved	0x0
7	R/W	Reserved [R77]	This bit should be set to 0 for backward compatibility.	0x0
8	R	Reserved [R88]	Reserved	0x0
9	R/W	MSI Vector Count Mode Select [MSIVCMS]	Sets the mode of generating MSI_VECTOR_COUNT output for all functions. 0 - MSI_VECTOR_COUNT always outputs the configured value of MSI Multiple Message Enable[2:0] register. 1 - MSI_VECTOR_COUNT outputs the lesser of the MSI Multiple Message Enable[2:0] and MSI Multiple Message Capable[2:0] This mode can be used to handle any programming error form the Host software.	0x0

Bits	SW	Name	Description	Reset
10	R/W	Disable RX NP Starvation Prevention [DRXNPSP]	As per PCIe specification, Non-Posted packets should not pass ahead of a Posted packet. Posted and Non-Posted packets are stored in a common Receive PNP FIFO. Controller ensures that the P and NP are delivered to the HAL/AXI target interface without violating the Ordering rules. When a mix of P and NP requests are received over the link, the NP packets can be starved if multiple Posted packets are stored in the PNP RX FIFO. Controller implements a mechanism to prevent NP Starvation Prevention which can be programmed through this bit: • 0: Send P and NP in the received order, instead of giving priority only for P and starve NP when continous P, NP packets are received. • 1: Priority only for P. Starve NP when continous P, NP packets are received. NP packets sent to HAL/AXI target interface only when all P packets in the PNP FIFO are delivered.	0x0
11	R/W	Disable Client TX MUXarbitartion [R1111]	When this bit is 1, Disable Client TX MUX Completion and PNP request arbitartion,roundrobin priority logic addedto prevent PNP requests from starving when completions are present.	0x0
12	R	Reserved [R1212]	Reserved	0x0
13	R	Reserved [R1313]	Reserved	0x0
14	R/W	Disable Set Slot Power Limit Message [DSSPLM]	Disable sending Set Slot Power Limit Message if the Slot Capabilitied register is configured.	0x0
15	R/W	Force Disable Scrambling [FDS]	Disable Scrambling/Descrambling in Gen1/Gen2.	0x0
16	R/W	Enable AXI Bridge Write Priority [AWRPRI]	When this bit is 1, the AXI bridge places a write request on the HAL Master interface in preference over a read request if both AXI write and AXI read requests are available to be asserted on the same clock cycle.	0x0
17	R/W	Disable Parity Check [HPRSUPP]	When this bit is 1, data path parity check is disabled on the TX side of the Controller.	0x0
18	R/W	Disable OS After Skip Framing Check [DOASFC]	When this bit is 1, the Controller will not check for OS after SKIP OS as part of Gen3 Framing Error Checks. This bit should normally set to 0, as thisis a mandatory Gen3 Framing Error check in the PCIe 3.0 specifications.	0x0
19	R/W	Disable Illegal OS After EDS Framing Check [DIOAEFC]	When this bit is 1, the Controller will not check for illegal OS after EDS as part of Gen3 Framing Error Checks. This bit should normally set to 0, as thisis a mandatory Gen3 Framing Error check in the PCIe 3.0 specifications.	0x0
20	R/W	Disable checking of invalidmessage codes [DCIVMC]	When this bit is 1, the Controller will not check for invalid message codes. This bit should normally set to 0, as the invalid message code checking is mandatory in the PCIe 3.0 specifications.	0x0
21	R/W	Disable Sync Header Error Check [DSHEC]	When this bit is 0, the Controller will signal a framing error if it detects a sync header error in the received blocks at 8 GT/s or 16 GT/s speed (A 00 or 11 binary setting of the sync header on the received blocks in any lane constitutes a framing error). Setting this bit to 1 suppresses this error check. This bit should normally be set to 0, as the sync header check is mandatory in the PCIe 3.0 Specifications.	0x0
22	R/W	Disable Link Re-Training on Framing Error [DLRFE]	When this bit is 1, the Controller will not transition its LTSSM into the Recovery state when it detects a Framing Error at 8 GT/s or 16 GT/s speed (as defined in Section 4.2.2.3.3 of the PCIe Base Specification 3.0. This bit must normally be set to 0 so that a Framing Error will cause the LTSSM to enter Recovery. The setting of this bit has no effect on the operation of the Controller at 2.5 and 5 GT/s speeds.	0x0

Bits	SW	Name	Description	Reset
23	R/W	Disable Link Upconfigure Capability [DLUC]	The user may set this bit to turn off the link upconfigure capability of the Controller. Setting this bit prevents the Controller from advertising the link upconfigure capability in training sequences transmitted in the Configuration.Complete state. In addition, setting this bit causes the Controller to put the unused lanes into Turn Off mode. When disable_link_upconfigure_capability==1: Controller drives PIPE_TX_ELEC_IDLE==1 AND PIPE_TX_COMPLIANCE==1 for the Unused upper lanes. The Unused upper lanes are put into Turn Off mode by the PHY as per PIPE specification. When disable_link_upconfigure_capability==0:Controller drives PIPE_TX_ELEC_IDLE==1 AND PIPE_TX_COMPLIANCE==0 for the Unused upper lanes. The Unused upper lanes are put into Electrical Idle by the PHY.	0x0
24	R/W	Enable Fast Link Training [EFLT]	This bit is provided to shorten the link training time to facilitate fast simulation of the design, especially at the gate level. Enabling this bit has the following effects: • The 1 ms, 2 ms, 12 ms, 24 ms, 32 ms, and 48 ms timeout intervals in the LTSSM are shortened by a factor of 500. • In the Polling.Active state of the LTSSM, only 16 training sequences are required to be transmitted (Instead of 1024) to make the transition to the Configuration state. This bit should not be set during normal operation of the Controller.	0x0
25	R/W	Enable Slot Power Capture [ESPC]	When this bit is set to 1, the Controller will capture the Slot Power Limit Value and Slot Power Limit Scale parameters from a Set_Slot_Power_Limit message received in the Device Capabilities Register. When this bit is 0, the capture is disabled. This bit is valid only when the Controller is configured as an Endpoint. It has no effect when the Controller is a Root Complex.	0x0
26	R/W	Inject End-to-End Data Protection Parity Error [IEDPPE]	When set to 1, this bit inverts the parity bits generated by the Controller for end-to-end data protection. This will result in the inversion of parity bits for data payloads delivered through the HAL Target Interface request descriptor. This bit is to be used for diagnostics only, and should not be set during normal operation.	0x0
27	R/W	Disable Gen3 LFSR Update from SKP [DGLUS]	Setting this bit to 1 disables the update of the LFSRs in the Gen3 descramblers of the Controller, from the values received in SKP sequences. This bit should not be set during normal operation, but is useful for testing.	0x0
28	R/W	Disable Electrical Idle Infer in L0 State [DEI]	Setting this bit to 1 disables the inferring of electrical idle in the L0 state. Electrical idle is inferred when no flow control updates and no SKP sequences are received within an interval of 128 µs. This bit should not be set during normal operation, but is useful for testing.	0x0
29	R/W	Disable Flow Control Update Timeout [DFCUT]	When this bit is 0, the Controller will time out and re-train the link when no Flow Control Update DLLPs are received from the link within an interval of 128 µs. Setting this bit to 1 disables this timeout. When the advertised receive credit of the link partner is infinity for the header and payload of all credit types, this timeout is always suppressed. The setting of this bit has no effect in this case. This bit should not be set during normal operation, but is useful for testing.	0x0
30	R/W	Disable Ordering Checks [DOC]	Setting this bit to 1 disables the ordering check in the Controller between Completions and Posted requests received from the link.	1'b0
31	R/W	Enable Function- Specific Reporting of Type-1 Configuration Accesses [EFSRTCA]	Setting this bit to 0 causes all the enabled Functions to report an error when a Type-1 configuration access is received by the Controller, targeted at any Function. Setting it to 1 limits the error reporting to the type-0 Function whose number matches with the Function number specified in the request. If the Function number in the request refers to an unimplemented or disabled Function, all enabled Functions report the error regardless of the setting of this bit.	0x01

Local Error and Status Register @0x20c

This register contains the status of the various events, errors, and abnormal conditions in the Controller. Any of the status bits can be reset by writing a 1 into the bit position. This register does not capture any errors signaled by remote devices using PCIe error messages when the

Controller is operating in the RC mode. Unless masked by the setting of the Local Interrupt Mask Register, the occurrence of any of these conditions causes the Controller to activate the LOCAL_INTERRUPT output.

Table 331: i_local_error_status_register

Bits	SW	Name	Description	Reset
0	R/WOCLR	PNP RX FIFOParity Error [PRFPE]	Parity error detected while reading from the PNP Receive FIFO RAM.	0x0
1	R/WOCLR	Completion RX FIFO Parity Error [CRFPE]	Parity error detected while reading from the Completion Receive FIFO RAM.	0x0
2	R/WOCLR	Replay RAM Parity Error [RRPE]	Parity error detected while reading from Replay Buffer RAM.	0x0
3	R/WOCLR	PNP RX FIFOOverflow [PRFO]	Overflow occurred in the PNP Receive FIFO.	0x0
4	R/WOCLR	Completion RX FIFO Overflow [CRFO]	Overflow occurred in the Completion Receive FIFO.	0x0
5	R/WOCLR	Replay Timeout [RT]	Replay timer timed out.	0x0
6	R/WOCLR	Replay Timer Rollover [RTR]	Replay timer rolled over after four transmissions of the same TLP.	0x0
7	R/WOCLR	Phy Error [PE]	Phy error detected on receive side. This bit is set when an error is detected in the receive side of the Physical Layer of the Controller (e.g., a bit error or coding violation). This bit is set upon any of the following errors: • PHY reported 8B10B error, Disparity Error, Elastic Buffer Overflow Error, Underflow Error • GEN3 TLP, DLLP Framing Errors • OS Block Received Without EDS • Data Block Received After EDS • Illegal OS Block After EDS • OS Block Received After SKIP OS • OS Block Received After SDS • Sync Header Error • Loss of Gen3 Block Alignment. This error is not Function-specific.	0x0
8	R/WOCLR	Malformed TLP Received [MTR]	Malformed TLP received from the link.	0x0
9	R/WOCLR	Unexpected Completion Received [UCR]	Unexpected Completion received from the link.	0x0
10	R/WOCLR	Flow Control Error [FCE]	An error was observed in the flow control advertisements from the other side.	0x0
11	R/WOCLR	Completion Timeout [CT]	A request timed out waiting for completion.	0x0
12	R	Reserved [R12]	Reserved	0x0
16:13	R	Reserved [R13]	Reserved	0x0
17	R/WOCLR	End to End Parity Error [EEPE]	The Controller detected an End-to-End Parity Error.	0x0
18	R/WOCLR	Unmapped TC [UTC]	Unmapped TC error. This bit is tied to 0 since this configuration of the Controller does not implement the Virtual Channel Capability Registers.	0x0
19	R/WOCLR	MSI Mask Value Change [MMVC]	This status bit is set whenever the MSI mask register value in the MSI capability register changes value in ANY of the functions in the controller.	0x0
20	R	Reserved [R22]	Reserved	0x0

Bits	SW	Name	Description	Reset
21	R/WOCLR	Hardware Autonomous Width Change Disable Toggle [HAWCD]	This interrupt status bit indicates that the Host toggled the Hardware Autonomous Width Change bit in the Link Control Register through a Config Write. Upon this interrupt, the Client firmware must read the Link Control Register to check the value set by Host in the Hardware Autonomous Width Change bit. The Host Software may disable autonomous width change by setting Hardware Autonomous Width Disable bit in the Link Control register. If disabled by the Host and if the Endpoint firmware had initiated an autonomous width downsizing prior to this interrupt, then the local Client firmware is responsible to upconfigure the Link to go to its full functional width by initiating the link_upconfigure_retrain_link within 1 ms of this interrupt.	0x0
22	R	Reserved [R23_1]	Reserved	0x0
24:23	R	Reserved [R24]	Reserved	0x0
25	R/WOCLR	MSIX Function Mask Change [MSIXMSKST]	This interrupt status bit is used when MSIX Function Mask Enhanced Interrupt Enable bit is set to 0 by the User. This status bit indicates that the MSIX Function Mask bit of any function, PF or VF, was programmed or configured by Local Firmware Or Host SW.	0x0
27:26	R	Reserved [R27]	Reserved	0x0
28	R	Reserved [R28]	Reserved	0x0
29	R/WOCLR	axi master read FIFO ram ecc uncorrectable error [AXIMASTER_RFIFO_ER_UN]	This indicates an uncorrectable axi master write FIFO ram parity/ ecc error.	0x0
30	R/WOCLR	axi slave write FIFO ram ecc uncorrectable error [AXISLAVE_WFIFO_ER_UN]	This indicates an uncorrectable axi slave write FIFO ram parity/ecc error.	0x0
31	R/WOCLR	AXI slave reorder RAM ECC uncorrectable error [REORDER_ER_UN]	This indicates an uncorrectable axi slave reorder ram parity/ecc error.	0x0

Local Interrupt Mask Register @0x210

This register contains a mask bit for each interrupting condition. Setting the bit to 1 prevents the corresponding condition in the Local Error Status Register from activating the LOCAL_INTERRUPT output.

Table 332: i_local_intrpt_mask_reg

Bits	SW	Name	Description	Reset
0	R/W	PNP RX FIFOParity Error [PRFPE]	Parity error detected while reading from the PNP Receive FIFO RAM.	1'b1
1	R/W	Completion RX FIFO Parity Error [CRFPE]	Parity error detected while reading from the Completion Receive FIFO RAM.	1'b1
2	R/W	Replay RAM Parity Error [RRPE]	Parity error detected while reading from Replay Buffer RAM.	1'b1
3	R/W	PNP RX FIFOOverflow [PRFO]	Overflow occurred in the PNP Receive FIFO.	1'b1
4	R/W	Completion RX FIFO Overflow [CRFO]	Overflow occurred in the Completion Receive FIFO.	1'b1
5	R/W	Replay Timeout [RT]	Replay timer timed out.	1'b1
6	R/W	Replay Timer Rollover [RTR]	Replay timer rolled over after four transmissions of the same TLP.	1'b1
7	R/W	Phy Error [PE]	Phy error detected on receive side.	1'b1
8	R/W	Malformed TLP Received [MTR]	Malformed TLP received from the link.	1'b1
9	R/W	Unexpected Completion Received [UCR]	Unexpected Completion received from the link.	1'b1
10	R/W	Flow Control Error [FCE]	An error was observed in the flow control advertisements from the other side.	1'b1

Bits	SW	Name	Description	Reset
11	R/W	Completion Timeout [CT]	A request timed out waiting for completion.	1'b1
12	R	Reserved [R12]	Reserved	1'b0
16:13	R	Reserved [R13]	Reserved	0x0
17	R/W	End to End Parity Error [EEPE]	The Controller detected an End-to-End Parity Error.	1'b1
18	R/W	Unmapped TC [UTC]	Unmapped TC error.	0x1
19	R/W	MSI Mask Value Change [MMVC]	MSI mask register value in the MSI capability register changes value in ANY of the functions in the controller.	0x1
20	R	Reserved [R45]	Reserved	1'b0
21	R/W	Hardware Autonomous Width Change Disable Toggle [HAWCD]	This bit is used to mask interrupt that indicates that the Host toggled the Hardware Autonomous Width Change in the Endpoint Link Control Register through a Config Write.	1'b1
22	R	Reserved [R23_1]	Reserved	0x0
24:23	R	Reserved [R24]	Reserved	0x0
25	R/W	MSIX Function Mask Change [MSIXMSK]	This bit is used to mask interrupt that indicates that the MSIX Function Mask bit of any function, PF or VF, was programmed or configured by Local Firmware Or Host SW.	1'b1
27:26	R	Reserved [R27]	Reserved	0x0
28	R	Reserved [R28]	Reserved	0x0
29	R/W	AXI master read FIFO RAM ECC uncorrectable error mask [AXIMASTER_RFIFO_ER_UN]	Mask for uncorrectbale axi master write FIFI RAM parity/ECC error.	0x0
30	R/W	AXI slave write FIFO RAM ECC uncorrectable error mask [AXISLAVE_WFIFO_ER_UN]	Mask for uncorrectbale AXI slave write FIFO RAM parity/ECC error.	0x0
31	R/W	AXI slave reorder RAM ECC uncorrectable error mask [REORDER_ER_UN]	Mask for uncorrectbale AXI slave reorder RAM parity/ECC error.	0x0

LCRC Error Count Register @0x214

This register contains the count of the number of TLPs received by the Controller with LCRC errors in them. This is a 16-bit saturating counter that can be reset to 0 by writing all 1's into it.

Table 333: i_lcrc_err_count_reg

Bits	SW	Name	Description	Reset
15:0	R/WOCLR	LCRC Eror Count [LEC]	Number of TLPs received with LCRC errors.	0x0
31:16	R	Reserved [R11]	Reserved	0x0

ECC Correctable Error Count Register @0x218

This register contains the count of the number of ECC errors detected and corrected during reads from the PCIe core external RAMs.

Table 334: i_ecc_corr_err_count_reg

Bits	SW	Name	Description	Reset
7:0	R/WOCLR	PNP FIFO RAMCorrectable Error Count [PFRCER]	Number of correctable errors detected while reading from the PNP FIFO RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.	0x0
15:8	R/WOCLR	SC FIFO RAMCorrectable Error Count [SFRCER]	Number of correctable errors detected while reading from the SC FIFO RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.	0x0

Bits	SW	Name	Description	Reset
23:16	R/WOCLR	Replay RAM Correctable Error Count [RRCER]	Number of correctable errors detected while reading from the Replay Buffer RAM. This is an 8- bit saturating counter that can be cleared by writing all 1's into it.	0x0
31:24	R	Reserved [R31_2]	Reserved	0x0

LTR Snoop/No-Snoop Latency Register @0x21c

This register contains the Snoop and No-Snoop Latency parameters used by the Controller when sending Latency Tolerance Reporting (LTR) Message. When the Controller is configured in the Endpoint mode, client software can program these fields to the desired latency settings and then set the Send LTR Message bit in the LTR Message Generation Control Register to send an LTR message to the Root Complex. The fields in this register should not be changed when the Send LTR Message bit in the LTR Message Generation Control Register is 1, which indicates that an LTR message is pending to be transmitted.

Table 335: i_ltr_snoop_lat_reg

Bits	SW	Name	Description	Reset
9:0	R/W	No-Snoop Latency Value [NSLV]	The client software must program this field with the value to be sent in the No-Snoop Latency Value field of the LTR message.	0x0
12:10	R/W	No-Snoop Latency Scale [NSLS]	The client software must program this field with the value to be sent in the No-Snoop Latency Scale field of the LTR message.	0x0
14:13	R	Reserved [R12]	Reserved	0x0
15	R/W	No-Snoop Latency Requirement [NSLR]	The client software must set this bit to 1 to set the No-Snoop Latency Requirement bit in the LTR message to be sent.	0x0
25:16	R/W	Snoop Latency Value [SLV]	The client software must program this field with the value to be sent in the Snoop Latency Value field of the LTR message.	0x0
28:26	R/W	Snoop Latency Scale [SLS]	The client software must program this field with the value to be sent in the Snoop Latency Scale field of the LTR message.	0x0
30:29	R	Reserved [R13]	Reserved	0x0
31	R/W	Snoop Latency [SL]	The client software must set this bit to 1 to set the Snoop Latency Requirement bit in the LTR message to be sent.	0x0

LTR Message Generation Control Register @0x220

This register contains fields for the generation of Latency Tolerance Reporting (LTR) Messages. This register is to be used only when the Controller is configured in the Endpoint mode.

Table 336: i_ltr_msg_gen_ctl_reg

Bits	SW	Name	Description	Reset
9:0	R/W	Minimum LTR Interval [MLI]	This field specifies the minimum spacing between LTR messages transmitted by the Controllerin units of microseconds. The PCI Express Specifications recommend sending no more than two LTR messages within a 500 microsecond interval. The Controller will wait for the minimum delay specified by this field after sending an LTR message, before transmitting a new LTR message. *NOTE:* The LINK can be in low power states (L0s and L1) when send LTR Message is trigered. So, the user has to consider the exit latencies while programming this field. It is recommended to program this field with about 2 µs higher than the required interval to account for the L0s/L1 exit latencies.	0xFA

Bits	SW	Name	Description	Reset
10	R	Send LTR Message [SLM]	Setting this bit causes the Controller to transmit an LTR message with the parameters specified in the LTR Snoop/No-Snoop Latency Register (Section 8.4.2.9). This bit is cleared by the Controller on transmitting the LTR message, and stays set until then. Client software must read this register and verify that this bit is 0 before setting it again to send a new message. This field becomes writable when LTR mechanism is enabled in device control-2 register.	0x0
11	R/W	Transmit Message on LTR Mechanism Enable Transition [TMLMET]	When this bit is set to 1, the Controller will automatically transmit an LTR message whenever the LTR Mechanism Enable bit in the Device Control 2 Register changes from 0 to 1, with the parameters specified in the LTR Snoop/No-Snoop Latency Register. When this bit is 1, the Controller will also transmit an LTR message wheneverthe LTR Mechanism Enable bit is cleared, if the following conditions are both true: **1.** The Controller sent at least one LTR message since the LTR Mechanism Enable bit was last set. **2.** The most recent LTR message transmitted by the Controller had as least one of the Requirement bits set. The Controller will set the Requirement bits in this LTR message to 0. When this bit 11 is 0, the Controller will not, by itself, send any LTR messages in response to state changes of the LTR Mechanism Enable bit. Client logic may monitor the state of the LTR_MECHANISM_ ENABLE output of the Controller and transmit LTR messages through the master interface, in response to its state changes.	0x1
12	R/W	Transmit Message on Function Power State Change [TMFPSC]	When this bit is set to 1, the Controller will automatically transmit an LTR message when all the Functions in the Controller have transitioned to a non-D0 power state, provided that the following conditions are both true: **1.** The Controller sentat least one LTR message since the Data Link layer last transitioned from down to up state. **2.** The most recent LTR message transmitted by the Controller had as least one of the Requirement bits set. The Controller will set the Requirement bits in this LTR message to 0. When this bit 12 is 0, the Controller will not, by itself, send any LTR messages in response to Function Power State changes. Client logic may monitor the FUNCTION_POWER_STATE outputs of the Controller and transmit LTR messages through the master interface, in response to changes in their states.	0x1
31:13	R	RSVD	RSVD	19'h00000

PME Service Timeout Delay Register @0x224

This register stores the timeout delay parameter for the service timeout mechanism associated with the generation of PM_PME messages. In the Endpoint mode, the Controller will re-transmit a PM_PME message after the expiration of this delay if the Root Complex did not clear the PME Status bit in the Power Management Control and Status Register. This register is not used when the Controller is configured as Root Complex.

Table 337: i_pme_service_timeout_delay_reg

Bits	SW	Name	Description	Reset
19:0	R/W	PME Service Timeout Delay [PSTD]	Specifies the timeout delay for retransmission of PM_PME messages. The value is in units of microseconds. The actual time elapsed has a +1 microseconds tolerance from the value programmed.	0x186A0
20	R/W	Disable PME message on PM Status [DPMOPS]	When this bit is set, Controller will not automatically send a PME message when the PM Status bit in PMCSR register is set.	0x0
31:21	R	Reserved [R21]	Reserved	0x0

Root Port Requestor ID Register @0x228

When the Controller is configured as Root Complex, this ID will be used for all internally generated messages.

Table 338: i_root_port_requestor_id_reg

Bits	SW	Name	Description	Reset
15:0	R/W	Root Port Requestor ID [RPRI]	RID (bus, device and function numbers) for all TLPs internally generated by Root Port.	0x0
31:16	R	Reserved [R0]	Reserved	0x0

Endpoint Bus and Device Number Register @0x22c

When the Controller is configured as Endpoint, this register holds the Bus and Device number captured for Function 0

Table 339: i_ep_bus_device_number_reg

Bits	SW	Name	Description	Reset
4:0	R	Device Number [EPDN]	Device Number captured by Function 0 in Endpoint mode	0x0
7:5	R	Reserved [R5]	Reserved	0x0
15:8	R	Bus Number [EPBN]	Bus Number captured by Function 0 in Endpoint mode	0x0
31:16	R	Reserved [R16]	Reserved	0x0

Debug Mux Control 2 Register @0x234

Table 340: i_debug_mux_control_2_reg

Bits	SW	Name	Description	Reset
0	R/W	Disable LOCALLF, LOCALFSsampling after speed change [DLFFS]	As per PIPE 4.2 specification, the LOCALLF, LOCALFS outputs from PHY can be sampled uponf PHYSTATUS pulse after Reset# OR upon the first PHYSTATUS pulse after speed change to GEN3. This bit can be set to 1 to disable sampling after speed change to GEN3 or higher	0x0
1	R/W	Enable Extended Config Snoop Read [EXTSNP]	This bit can be set if extra clock cycles (up to 16) are required by the Client Application logic to respond with the Read Data on Configuration Snoop Interface. Please refer to the user guide section on Configuration Snoop Interface for timing diagrams.	0x0
2	R/W	Disable SDS OS Check [DISSDSCHK]	As per PCIe specification, When using 128b/130b encoding, next state is L0 if eight consecutive Symbol Times of Idle data are received on all configured Lanes. The Controller checks to ensure that the Idle symbols of data are received in Data Blocks after SDS OS. This check is enabled by default. Setting this bit to 1 turns off this check.This bit is recommended to be kept at the default value of 0.	0x0
3	R/W	Enable Link Lane Number Check for Loopback and Link Disable [ENLNCHK]	As per PCIe specification, LTSSM should transition to Disabled after any Lanes that are transmitting TS1 Ordered Sets receive two consecutive TS1 Ordered Sets with the Disable Link bit asserted. Similarly, LTSSM should transition to Loopback after all Lanes that are transmitting TS1 Ordered Sets, that are also receiving TS1 Ordered Sets, receive the Loopback bit asserted in two consecutive TS1 Ordered Sets. Controller ignores the Link and Lane Number in the Received TS1s with Loopback/Disable bit set. Setting this bit to 1 turns on the check for link number (assigned by RC in Recovery.Idle) and lane number (PAD in Config.LW.Start or as assigned by RC in Recovery.Idle). This bit is recommended to be kept at the default value of 0.	0x0

Bits	SW	Name	Description	Reset
4	R/W	ARI Capable Hierarchy Mode [ARICAPMOD]	As per SR IOC specification, ARI Capable Hierarchy bit is only present in the lowest numbered PF of a Device. The Controller has two modes to determine the lowest numbered PF. • 0: The first PF which is enabled (PF0) is taken as the lowest numbered PF. • 1: The first PF which has a non-zero TOTAL_VF_COUNT field is taken as the lowest numbered PF(Default Mode).	0x1
5	R/W	Gen3 Block Alignment Check Disable [BLKALNCHK]	When in the data stream at Gen3 or higher speeds, the pipe_rx_valid is asserted by the PHY. If the block alignment is lost, then the PHY may deassert pipe_rx_valid. Block Alignment may be lost if the received sync header is invalid. Controller supports detecting loss of block alignment while in a data stream in Gen3. • 0: Enable check for loss of Gen3 Block Alignment during data stream. • 1: Disable check for loss of Gen3 Block Alignment.	0x0
7:6	R/W	Gen3 Block Alignment Check Window [BLKALNWIN]	When in the data stream at Gen3 or higher speeds, the pipe_rx_valid is asserted by the PHY. If the block alignment is lost, then the PHY may deassert pipe_rx_valid. Controller reports loss of block alignment if pipe_rx_valid or pipe_rx_data_valid=0 for a period consecutive clock cycles as programmed in this field. • 00: 8CORE_CLK cycles • 01: 16 CORE_CLK cycles • 10: 64 CORE_CLK cycles • 11: 256 CORE_CLK cycles	0x1
8	R/W	Gen4 Enable Spec Rev0.5 Features [ENG4REV05]	When operating in Gen4 16GT/s, this Enables Gen4 Spec Revision 0.5 EIEOS and SKP features. When disabled, the Gen4 1.0 features are enabled, by default this bit is ZERO. • 1: Enable Gen4 0.5 Features • 0: Disable Gen4 0.5 Features (This enabled the Gen4 1.0 Features).	0x0
9	R/W	MSI Pending Status In Mode Select [MSIPIMS]	If the Client wishes to use the MSI_PENDING_STATUS_IN Signal to Update the MSI pending Bits register, this bit needs to be set to 1. Otherwise the Pending Bits register is updated via the APB Interface	0x0
10	R/W	Poisoned TLP Received Advisory Non-Fatal [PSNADV]	As per PCIe specification 2.7.2.2, the following Poisoned TLP requests must be handled as Uncorrectable and not as Advisory: I/O Write Request, Memory Write Request, or non-vendor-defined Message with data that target a Control structure. Since it is not possible for the Controller to determine if the target is a Control or a non-Control strusture, the Controller implements this bit for the user to determine the required handling. • 1: Poisoned TLP of type IOWr, MemWr, MsgD will be handled as Advisory Non-Fatal Error. • 0: Poisoned TLP of type IOWr, MemWr, MsgD will be handled as Uncorrectable Error. *Note:* Poisoned CpID will always be reported as Advisory Non-Fatal and is not controlled by this register setting.	0x0
11	R/W	Completion Timeout Advisory Non-Fatal [CMPTOADV]	As per PCIe specification on Error Signaling, the Requester detecting a Completion Timeout is allowed to handle this as an Advisory Non-Fatal Error. • 1: Completion Timeout is handled as Advisory Non-Fatal Error. • 0: Completion Timeout is handled as normally as a Non-Fatal Error.	0x1
12	R/W	Enable Gen12 Enhanced Deskew With Skip [ENG12SK]	• 0: In Gen1/2, Deskew based on TS1/TS2 COM method. Deskew limit up to seven symbols. • 1: In Gen1/2, Deskew based on SKIP OS method. Deskew limit up to 20 symbols.	0x0

Bits	SW	Name	Description	Reset
22:13	R/W	Maximum NP Outstanding Request Limit [MAXNPREQ]	The Controller supports 256 outstanding NP requests that can be initiated by the User. However, the number of split completion TLPs that can be stored in the Controller is limited to 128. The Completion FIFO will overflow if more than 128 split completion packets are pending. If the User interface can accept inbound Posted and Completion packets at the samerate as received from PCIe link, then the split completion FIFO will never reach the FULL condition. However, if the User cannot guarantee this, then this register needs to be programmed as described in the Programming Guide section of the Controller User guide. The Controller will limit the maximum number of outstanding NP requests to the value programmed in this register. Example: • 8: Controller will limit maximum number of outstanding NP requests to 8. • 0–7: Reserved Default Value is 256.	10'd128
23	R/W	Enable Variable Core Clock [VARCCLKEN]	If this bit is set the CORE_CLK input can be driven with Variable Clock depending on the Link Speed, similar to the PIPE_PCLK.	0x0
24	R/W	MSI Mask Change Enhanced Interrupt Enable [MSIMSKEN]	By default, the Controller provides a single status bit when any function's MSI Mask is programmed or configured by Local firmware or Host SW. Controller also implements an enhanced MSI Mask Interrupt mechanism, which provides per-function set/clear status when a function's MSI Mask is updated by SW. This Local Management programmable bit allows user to choose between the Default and Enhanced MSI Mask Change Interrupt mechanisms.	0x0
25	R/W	MSIX Function Mask Change Enhanced Interrupt Enable [MSIXMSKEN]	By default, the Controller provides a single status bit when any function's MSIX Function Mask is programmed or configured by Local firmware or Host SW. Controller also implements an enhanced MSIX Function Mask Interrupt mechanism, which provides per-function set/clear status when a function's MSIX Function Mask is updated by SW. This Local Management programmable bit allows user to choose between the Default and Enhanced MSIX Function Mask Change Interrupt mechanisms.	0x0
26	R	Reserved [R26]	Reserved	0x0
27	R/W	Disable Tx Nullify on E2E Parity Error [DTAE2EP]	By default, when End-to-End Parity error is detected on inbound/outbound data streams, then all the transmitted outbound packets will be Nullified by the Controller. This bit can be used to turn off nullifying Tx packets on End-to-End Parity Error.	0x0
28	R/W	Disable FLR Termination Resp Block [DFLRTRB]	• 1 : NP Termination due to FLR/Completion Timeout is delayed till the RX Completion FIFO is Empty. • 0 : NP Termination due to FLR is done immediately on receiving FLR/Completion Timeout.	1'b1
29	R/W	Disable Rx RAM freeze Uncorrectable Error [DRXRMFR]	By default, when an Uncorrectable error is detected on a receive FIFO RAM, then no packets are read out of the RAM subsequent to the error and the RAMs are frozen. • 0: Receive FIFO RAMs are frozen after an uncorrectable error. • 1: Receive FIFO RAMs continue to read subsequent packets after an uncorrectable error.	0x0
30	R	Reserved [R30]	Reserved	0x0
31	R/W	HOT Reset Level Trigger [HRLT]	If set this bit makes the HOT_RESET_OUT signal behave as a level signal rather than a pulse. When set, the HOT_RESET_OUT will be asserted as long as the controller is in the HOT Reset state.	0x0

PHY STATUS 1 Register @0x238

This status register provides additional debug information about the PHY. Bits 8:0 provide information to debug Receiver Errors.

Table 341: i_phy_status_1_reg

Bits	SW	Name	Description	Reset
0	R/WOCLR	TLP PHYError Status [TLPPHYER]	This bit indicates that a PHY Error was detected on the PIPE_RX_STATUS within a TLP. Write a 1 to clear this field.	0x0
1	R/WOCLR	OS Block After Skip OS [OSASKP]	This bit indicates that an Ordered Set BLock was received immediately after a SKIP OS. This is a framing error. Write a 1 to clear this field.	0x0
2	R/WOCLR	Illegal OS BlockAfter EDS [ILOSEDS]	The Valid OS blocks after an EDS are EIOS, EIEOS and SKP. If any other OS blocks are received after EDS, then it is a framing error and this bit is asserted.	0x0
3	R/WOCLR	Data Block After EDS [DATEDS]	This bit is set if a Data Block is received after an EDS. Write a 1 to clear this error.	0x0
4	R/WOCLR	OS Block Received without EDS [OSWOEDS]	This bit is set if an Ordered Set Block is received without an EDS. This is a framing error. Write a 1 to clear this error.	0x0
5	R/WOCLR	Gen3 Framing Error Detected [G3FRERR]	This bit is set if a framing error is detected while receiving a TLP in Gen3. Example, if an invalid token is received in a data stream, this error is flagged. Write a 1 to clear this error.	0x0
6	R/WOCLR	OS Block Received After SDS [OSAFSDS]	This bit is set if an SDS is received after an SDS. This is a framing error. Write a 1 to clear this error.	0x0
7	R/WOCLR	Invalid Sync Header Error [INVSYNHR]	This bit is set if an invalid Sync Header is detected. 00 and 11 are Invalid Sync Headers. Write a 1 to clear this error.	0x0
8	R/WOCLR	Loss of Block Alignment Error [LOSBLKALN]	This bit is set if the PHY Loses Block Alignment during data stream. This is detected based upon an unexpected PIPE_RX_VALID input deassertion during data stream. Write a 1 to clear this error.	0x0
31:9	R	Reserved [R31]	Reserved	0x0

Debug Mux Control 3 Register @0x23c

Table 342: i_debug_mux_control_3_reg

Bits	SW	Name	Description	Reset
0	R	Reserved [R0]	Reserved	0x0
1	R/W	Disable GEN4 data parity check [DGDPC]	To disable GEN4 data parity check from LM register.	0x0
2	R/W	Disable link training error [DLTE]	Used to disable and enable link training error logging and by default it is enabled.	0x0
3	R/W	Disable surprise down error status [DSDES]	Used to disable and enable Surprise Down Error status logging and by default it is enabled.	0x0
4	R/W	Disable Rcb check [DRC]	USed to disable and enable the RCB checker and by default it is disable (wrire 0 to enable and write 1 to disable).	1'b1
7:5	R	Reserved [R5]	Reserved	0x0
9:8	R/W	Config LW Eval Window [CLWEW]	This field can be used to control the window in which the Controller waits during Configuration states to determine link width. After two consecutive TS1s are received on any lane, the Controller waits for the time defined in this window for other lanes to receive TS1s before determining link width. • 00: Wait for 4 TS1 window • 01: Wait for 8 TS1 window • 10: Wait for 16 TS1 window • 11: Wait for 24 TS1 window	2'b00

Bits	SW	Name	Description	Reset
10	R/W	Disable LTSSM Freeze 1US Recovery Equalization Phase0 [DLF1USEQ]	As per PCIe specification, the EP is permitted to wait for up to 500 ns after entering Phase 0 before evaluating received information for TS1 Ordered Sets if it needs the time to stabilize its Receiver logic. Similarly, the RP is permitted to wait for up to 500 ns after entering Phase 1 before evaluating received information for TS1 Ordered Sets if it needs the time to stabilize its Receiver logic. Controller implements a 1 µs time on entering Recovery Equalization Phase0/Phase1 during which the received TS1 is ignored. Writing a 1 disables the 1 µs wait.	1'b1
11	R/W	Disable Support for all Ranges (A,B,C,D in Completion Timeout) [DSRCT]	As per PCIe specification, the completion timeout values for the outbound request must be in) Ranges (A,B,C,D) as per the given timeout values. Within these ranges there are Subrange (0 or 1) given which will determine the actual completion timeout values to be used. Disable this bit to support only 1 range (Range B).	1'b1
12	R/W	Error Emulation feature enable for AER registers. [EEFER]	When this bit is set, the AER Uncorrectable/Correctable Error Status registers can be written through LM registers.	1'b0
13	R/W	Error Emulation feature enable for Fatal ErrorInterrupt. [EEFEFE]	This bit is pulse signal which triggers Fatal error Interrupt.	1'b0
14	R/W	Error Emulation feature enable for Non-Fatal Error Interrupt. [EEFENFE]	This bit is pulse signal which triggers Non-Fatal error Interrupt.	1'b0
15	R/W	Error Emulation feature enable for Correctable Error Interrupt. [EEFECE]	This bit is pulse signal which triggers Correctable error Interrupt.	1'b0
17:16	R	Reserved [R16]	Reserved	0x0
18	R/W	Disable Config.Idle to Recovery after Timeout [DCIRTO]	This bit controls the LTSSM transition from Config.Idle to Recovery transition if 2 ms timeout occured in Config.Complete state. • 0: Transition from Config.Idle to Recovery if 2 ms timeout occured in Config.Complete state. • 1: Transition from Config.Idle to L0 transition if IDLE symbols received regardless of 2 ms timeout occuredin Config.Complete state. This bit must be at default value of 0 to be compliant to PCIe spec for Config.Idle state.	1'b0
19	R/W	Disable Link Number Transmit on Discontinuous Lanes [DLNTDL]	This bit controls the Link Number Transmit in Configuration.LinkWidth.Start state in EP Mode when one or more lane is disconnected. • 0: Transmit the received non-PAD LinkNum on all lanes that receive non-PAD LinkNum in Config.LW.Start state. • 1: Transmit the received non-PAD LinkNum on a contiguous set of lanes that receive non-PAD LinkNum in Config.LW.Start state. This bit must be atdefault value of 0 to be compliant to PCIe spec for Config.LW.Start state.	1'b0
20	R/W	Disable Loopback Entry TS1 Loopback bit check [DLETS1LC]	This bit controls the TS1 check during Loopback.Entry to Loopback.Active transition in Loopback Slave mode. In Loopback.Entry state, Next state is Loopback.Active if the data rate is 8.0 GT/s or higher and two consecutive TS1 Ordered Sets are received on all active Lanes. • 0: Transition if two consecutive TS1 receieved on all active lanes with Loopback bit set. • 1: Transition if two consecutive TS1 receieved on all active lanes without checking Loopback bit. This bit must be at default value of 1 to be compliant to PCIe spec for Loopback.Entry state.	1'b1
21	R/W	Disable to clear nak_schedule before TLP end [DCNSBTE]	When set NAK_SCHEDULE flag can be cleared before the TLP end else NAK_SCHEDULE flag will be clear at end of TLP PKT.	1'b0
22	R/W	Disable EIOS Consecutive Counter Reset Unexpected Data [DECCRUD]	This bit controls the EIOS Consecutive Counter. • 0: Reset EIOS consecutive counter if unexpected data received in between EIOS. • 1: Hold EIOS consecutive counter if unexpected data received after receiving 1 EIOS OS.	1'b0

Bits	SW	Name	Description	Reset
23	R/W	Disable rx elec idle exit in any check polling complaince [DREIECPC]	• 0: Check for electrical idle exit in ANY active lane for exit from Polling.Complaince at Gen1. • 1: Check for electrical idle exit in ALL active lanes for exit from Polling.Complaince at Gen1. *Note:* This register must be 0 to be compliant with the PCIe Spec. *Note:* This register is used only when PCIE_GENERATION_SEL==0. When PCIE_GENERATION_SEL> 0, Controller exits Polling.Complaince state based on ANY active lane as per PCIe specification.	1'b0
24	R/W	Disable Link Number check in configuration lanenumwait ltssm state [DLNCCL]	As per PCIe specification, in Configuration.Lanenum.Wait state, a device must check if any of the Lanes receive two consecutive TS1 Ordered Sets that have a Lane number different from when the Lane first entered Configuration.Lanenum.Wait, and not all the Lanes Link numbers are set to PAD Controller implements this check in Controller.Lanenum.Wait state. The received Link Number can be either PAD or non-PAD. • 0: Check for PAD/non-PAD Linknum in received TS1sin Configuration.Lanenum.Wait state. • 1: Check for only non-PAD Linknum in received TS1s in Configuration.Lanenum.Wait state. *Note:* This register must be 0 to be compliant with the PCIe Spec.	1'b0
25	R/W	Disable EIOS detection in gen2 polling complaince [DEIOSGPC]	When Polling.Compliance is entered due to Enter Compliance bit set, the exit is based on received EIOS or Enter Compliance bit programmed back to 0. This bit is used to control EIOS check in Polling.Compliance state. • 0: Enable EIOS-idle sequence detect logic in gen2 Polling.Compliance. • 1: Disable EIOS-idle sequence detect logic in gen2 Polling.Complaince. *Note:* This register must be 0 to be compliant with the PCIe Spec.	1'b0
26	R/W	Disable TS1 Coefficient Mismatch Check Hold [DTSCMCH]	• 0: Register and Hold the coefficient mismatch and use during Recovery.Rcvr.Lock -> Recovery.Rcvr.Cfg transition. • 1: Do not register. Check coefficient mimatch only during Recovery.Rcvr.Lock -> Recovery.Rcvr.Cfg transition. *Note:* This register must be 0 to be compliant with the PCIe Spec.	1'b0
27	R/W	Disable lane equalization control register reset after hot reset [DLERHR]	• 0: Reset Lane Equalization Control Register, PL_16GTS Lane Equalization Control Register during Link Down/Hot Reset. • 1: Do not reset Lane Equalization Control Register, PL_16GTS Lane Equalization Control Register during Link Down/ Hot Reset. *Note:* This register must be 0 to be compliant with the PCIe Spec.	1'b0
28	R/W	Disable to send a NAK due to phy error [DSNPE]	When set Data Link Layer will not send a NAK when PL indicated Phy Error for a received TLP else Nak will be schedule for phy error.	1'b0
29	R/W	Disable zero bus dev num for UR config compl [DZBDFURC]	When set Controller will copy the Bus and Device numbers from the Config Read into the completion for Config Reads done prior to any Config Write (Bus Device Number Capture not done).	1'b0
30	R/W	Disable Receive SKP ENDError Check [DRSEC]	As per PCIe specification, when using 128b/130b encoding, a received SKP Ordered set can be eight, 12, 16, 20, or 24 Symbols. The Elastic Buffer in the PHY can also add four symbols to the received SKP OS. The SKP OS bypasses Scrambling and Descrambling. While processing the received SKP OS, the Descrambler has two modes selected by this bit: • 0: stop SKP OS processing after SKP_ENDis received. • 1: stop SKP OS processing after SKP_END or 28 symbols received.	1'b0

Bits	SW	Name	Description	Reset
31	R/W	Disable Current Link Speed Update in Recovery.Speed State [DCLSRSS]	As per PCIe specification, during speed change in Recovery.Speed state, the new data rate must be reflected in the Current Link Speed field of the Link Status Register. This bit can be used to control the update of Current Link Speed status register: • 0: Update Current Link Speed status register in Recovery.Speed LTSSM state. • 1: Update Current Link Speed status register in L0 LTSSM state.	1'b0

Physical Function BAR Configuration Register 0 @0x240

This register specifies the configuration of the BARs associated with the Physical Function 0.

Table 343: i_pf_0_BAR_config_0_reg

Bits	SW	Name	Description	Reset
4:0	R/W	BAR 0 Aperture [BAR0A]	Specifies the aperture of the 32-bit BAR 0 or 64-bit BAR 0-1. For 32-bit BAR 0, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB (continued on next page)	5'h5

Bits	SW	Name	Description	Reset
		BAR 0 Aperture [BAR0A] (continued)	For 64-bit BAR 0-1, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001= 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	
7:5	R/W	BAR 0 Control [BAR0C]	Specifies the configuration of BAR 0. The various encodings are: • 000: Disabled • 001: 32bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h4

Bits	SW	Name	Description	Reset
12:8	R/W	BAR 1 Aperture [BAR1A]	Specifies the aperture of the BAR 1 when it is configured as a 32-bit BAR. For 32-bit BAR 1, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 01111 = 1 GB • 11000 = 2 GB	5'h5
15:13	R/W	BAR 1 Control [BAR1C]	Specifies the configuration of BAR 1. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0

Bits	SW	Name	Description	Reset
20:16	R/W	BAR 2 Aperture [BAR2A]	Specifies the aperture of the 32-bit BAR 2 or 64-bit BAR 2-3. For 32-bit BAR 2, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB (continued on next page)	5'h5

Bits	SW	Name	Description	Reset
		BAR 2 Aperture [BAR2A] (continued)	For 64-bit BAR 2-3, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	
23:21	R/W	BAR 2 Control [BAR2C]	Specifies the configuration of BAR 2. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h0

Bits	SW	Name	Description	Reset
28:24	R/W	BAR 3 Aperture [BAR3A]	Specifies the aperture of the BAR 3 when it is configured as a 32-bit BAR. For 32-bit BAR 3, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'h5
31:29	R/W	BAR 3 Control [BAR3C]	Specifies the configuration of BAR 3. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0

Physical Function BAR Configuration Register 1 @0x244

This register specifies the configuration of the BARs associated with the Physical Function.

Table 344: i_pf_0_BAR_config_1_reg

Bits	SW	Name	Description	Reset
4:0	R/W	BAR 4 Aperture [BAR4A]	Specifies the aperture of the 32-bit BAR 4 or 64-bit BAR 4-5. For 32-bit BAR 4, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB (continued on next page)	5'h5

Bits	SW	Name	Description	Reset
		BAR 4 Aperture [BAR4A] (continued)	For 64-bit BAR 4-5, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 2 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	
7:5	R/W	BAR 4 Control [BAR4C]	Specifies the configuration of BAR 4. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h0

Bits	SW	Name	Description	Reset
12:8	R/W	BAR 5 Aperture [BAR5A]	Specifies the aperture of the BAR 5 when it is configured as a 32-bit BAR. For 32-bit BAR 5, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'h5
15:13	R/W	BAR 5 Control [BAR5C]	Specifies the configuration of BAR 5. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0
20:16	R/W	EXP-ROM BAR Aperture [ERBA]	Specifies the aperture of the Expansion ROM BAR. The encodings are: • 00000–00011 = undefined • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 00110 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010–11111 = undefined	5'h5
21	R/W	EXP-ROM BAR Enable [ERBE]	This bit must be set to enable the Expansion ROM BAR associated with the Function.	0x01
23:22	R	Reserved [R22]	Reserved	0x0
30:24	R	Reserved [R24]	Reserved	0x0

Bits	SW	Name	Description	Reset
31	R/W	Enable Resizable BAR Capability [ERBC]	Setting this bit to 1 enables the Resizable BAR Capability in the PCI Express Configuration Space of the associated Function. When the Resizable BAR Capability is enabled, the apertures of the memory BARs of the corresponding Function are no longer selected by the fields in this register, but by the setting of the registers in the Resizable BAR Capability Structure.	0x0

Physical Function BAR Configuration Register 0 @0x248

This register specifies the configuration of the BARs associated with the Physical Function 1.

Table 345: i_pf_1_BAR_config_0_reg

Bits	SW	Name	Description	Reset
4:0	R/W	BAR 0 Aperture [BAR0A]	Specifies the aperture of the 32-bit BAR 0 or 64-bit BAR 0-1. For 32-bit BAR 0, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 00111 = 16 KB • 01000 = 32 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 =2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB (continued on next page)	5'h5

Bits	SW	Name	Description	Reset
		BAR 0 Aperture [BAR0A] (continued)	For 64-bit BAR0-1, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	
7:5	R/W	BAR 0 Control [BAR0C]	Specifies the configuration of BAR 0. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64bit memory BAR, prefetchable	3'h4

Bits	SW	Name	Description	Reset
12:8	R/W	BAR 1Aperture [BAR1A]	Specifies the aperture of the BAR 1 when it is configured as a 32-bit BAR. For 32-bit BAR 1, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'h5
15:13	R/W	BAR 1 Control [BAR1C]	Specifies the configuration of BAR 1. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0

Bits	SW	Name	Description	Reset
20:16	R/W	BAR 2 Aperture [BAR2A]	Specifies the aperture of the 32-bit BAR 2 or 64-bit BAR 2-3. For 32-bit BAR 2, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB (continued on next page)	5'h5

Bits	SW	Name	Description	Reset
		BAR 2 Aperture [BAR2A] (continued)	For 64-bit BAR 2-3, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	
23:21	R/W	BAR 2 Control [BAR2C]	Specifies the configuration of BAR 2. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010-011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h0

Bits	SW	Name	Description	Reset
28:24	R/W	BAR 3 Aperture [BAR3A]	Specifies the aperture of the BAR 3 when it is configured as a 32-bit BAR. For 32-bit BAR 3, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'h5
31:29	R/W	BAR 3 Control [BAR3C]	Specifies the configuration of BAR 3. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0

Physical Function BAR Configuration Register 1 @0x24c

This register specifies the configuration of the BARs associated with the Physical Function.

Table 346: i_pf_1_BAR_config_1_reg

Bits	SW	Name	Description	Reset
4:0	R/W	BAR 4 Aperture [BAR4A]	Specifies the aperture of the 32-bit BAR 4 or 64-bit BAR 4-5. For 32-bit BAR 4, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB (continued on next page)	5'h5

Bits	SW	Name	Description	Reset
		BAR 4 Aperture [BAR4A] (continued)	For 64-bit BAR 4-5,the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	
7:5	R/W	BAR 4 Control [BAR4C]	Specifies the configuration of BAR 4. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h0

Bits	SW	Name	Description	Reset
12:8	R/W	BAR 5 Aperture [BAR5A]	Specifies the aperture of the BAR 5 when it is configured as a 32-bit BAR. For 32-bit BAR 5, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'h5
15:13	R/W	BAR 5 Control [BAR5C]	Specifies the configuration of BAR 5. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0
20:16	R/W	EXP-ROM BAR Aperture [ERBA]	Specifies the aperture of the Expansion ROM BAR. The encodings are: • 00000–00011 = undefined • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 00110 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010–11111 = undefined	5'h5
21	R/W	EXP-ROM BAR Enable [ERBE]	This bit must be set to enable the Expansion ROM BAR associated with the Function.	0x01
23:22	R	Reserved [R22]	Reserved	0x0
30:24	R	Reserved [R24]	Reserved	0x0

Bits	SW	Name	Description	Reset
31	R/W	Enable Resizable BAR Capability [ERBC]	Setting this bit to 1 enables the Resizable BAR Capability in the PCI Express Configuration Space of the associated Function. When the Resizable BAR Capability is enabled, the apertures of the memory BARs of the corresponding Function are no longer selected by the fields in this register, but by the setting of the registers in the Resizable BAR Capability Structure.	0x0

Physical Function BAR Configuration Register 0 @0x250

This register specifies the configuration of the BARs associated with the Physical Function 2.

Table 347: i_pf_2_BAR_config_0_reg

Bits	SW	Name	Description	Reset
4:0	R/W	BAR 0 Aperture [BAR0A]	Specifies the aperture of the 32-bit BAR 0 or 64-bit BAR 0-1. For 32-bit BAR 0, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 =16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB (continued on next page))	5'h5

Bits	SW	Name	Description	Reset
		BAR 0 Aperture [BAR0A] (continued)	For 64-bit BAR 0-1, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	
7:5	R/W	BAR 0 Control [BAR0C]	Specifies the configuration of BAR 0. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h4

Bits	SW	Name	Description	Reset
12:8	R/W	BAR 1 Aperture [BAR1A]	Specifies the aperture of the BAR 1 when it is configured as a 32-bit BAR. For 32-bit BAR 1, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'h5
15:13	R/W	BAR 1 Control [BAR1C]	Specifies the configuration of BAR 1. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0

Bits	SW	Name	Description	Reset
20:16	R/W	BAR 2 Aperture [BAR2A]	Specifies the aperture of the 32-bit BAR 2 or 64-bit BAR 2-3. For 32-bit BAR 2, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB (continued on next page)	5'h5

Bits	SW	Name	Description	Reset
		BAR 2 Aperture [BAR2A] (continued)	For 64-bit BAR 2-3, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	
23:21	R/W	BAR 2 Control [BAR2C]	Specifies the configuration of BAR 2. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h0

Bits	SW	Name	Description	Reset
28:24	R/W	BAR 3 Aperture [BAR3A]	Specifies the aperture of the BAR 3 when it is configured as a 32-bit BAR. For 32-bit BAR 3, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'h5
31:29	R/W	BAR 3 Control [BAR3C]	Specifies the configuration of BAR 3. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0

Physical Function BAR Configuration Register 1 @0x254

This register specifies the configuration of the BARs associated with the Physical Function.

Table 348: i_pf_2_BAR_config_1_reg

Bits	SW	Name	Description	Reset
4:0	R/W	BAR 4 Aperture [BAR4A]	Specifies the aperture of the 32-bit BAR 4 or 64-bit BAR 4-5. For 32-bit BAR 4, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100= 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB (continued on next page)	5'h5

Bits	SW	Name	Description	Reset
		BAR 4 Aperture [BAR4A] (continued)	For 64-bit BAR 4-5, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	
7:5	R/W	BAR 4 Control [BAR4C]	Specifies the configuration of BAR 4. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h0

Bits	SW	Name	Description	Reset
12:8	R/W	BAR 5 Aperture [BAR5A]	Specifies the aperture of the BAR 5 when it is configured as a 32-bit BAR. For 32-bit BAR 5, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'h5
15:13	R/W	BAR 5 Control [BAR5C]	Specifies the configuration of BAR 5. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0
20:16	R/W	EXP-ROM BAR Aperture [ERBA]	Specifies the aperture of the Expansion ROM BAR. The encodings are: • 00000–00011 = undefined • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 00110 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010–11111 = undefined	5'h5
21	R/W	EXP-ROM BAR Enable [ERBE]	This bit must be set to enable the Expansion ROM BAR associated with the Function.	0x01
23:22	R	Reserved [R22]	Reserved	0x0
30:24	R	Reserved [R24]	Reserved	0x0

Bits	SW	Name	Description	Reset
31	R/W	Enable Resizable BAR Capability [ERBC]	Setting this bit to 1 enables the Resizable BAR Capability in the PCI Express Configuration Space of the associated Function. When the Resizable BAR Capability is enabled, the apertures of the memory BARs of the corresponding Function are no longer selected by the fields in this register, but by the setting of the registers in the Resizable BAR Capability Structure.	0x0

Physical Function BAR Configuration Register 0 @0x258

This register specifies the configuration of the BARs associated with the Physical Function 3.

Table 349: i_pf_3_BAR_config_0_reg

Bits	SW	Name	Description	Reset
4:0	R/W	BAR 0 Aperture [BAR0A]	Specifies the aperture of the 32-bit BAR 0 or 64-bit BAR 0-1. For 32-bit BAR 0, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB (continued on next page)	5'h5

Bits	SW	Name	Description	Reset
		BAR 0 Aperture [BAR0A] (continued)	For 64-bit BAR 0-1, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	
7:5	R/W	BAR 0 Control [BAR0C]	Specifies the configuration of BAR 0. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h4

Bits	SW	Name	Description	Reset
12:8	R/W	BAR 1 Aperture [BAR1A]	Specifies the aperture of the BAR 1 when it is configured as a 32-bit BAR. For 32-bit BAR 1, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'h5
15:13	R/W	BAR 1 Control [BAR1C]	Specifies the configuration of BAR 1. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0

Bits	SW	Name	Description	Reset
20:16	R/W	BAR 2 Aperture [BAR2A]	Specifies the aperture of the 32-bit BAR 2 or 64-bit BAR 2-3. For 32-bit BAR 2, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB (continued on next page)	5'h5

Bits	SW	Name	Description	Reset
		BAR 2 Aperture [BAR2A] (continued)	For 64-bit BAR2-3, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	
23:21	R/W	BAR 2 Control [BAR2C]	Specifies the configuration of BAR 2. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h0

Bits	SW	Name	Description	Reset
28:24	R/W	BAR 3 Aperture [BAR3A]	Specifies the aperture of the BAR 3 when it is configured as a 32-bit BAR. For 32-bit BAR 3, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'h5
31:29	R/W	BAR 3 Control [BAR3C]	Specifies the configuration of BAR 3. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0

Physical Function BAR Configuration Register 1 @0x25c

This register specifies the configuration of the BARs associated with the Physical Function.

Table 350: i_pf_3_BAR_config_1_reg

Bits	SW	Name	Description	Reset
4:0	R/W	BAR 4 Aperture [BAR4A]	Specifies the aperture of the 32-bit BAR 4 or 64-bit BAR 4-5. For 32-bit BAR 4, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB (continued on next page)	5'h5

Bits	SW	Name	Description	Reset
		BAR 4 Aperture [BAR4A] (continued)	For 64-bit BAR 4-5, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	
7:5	R/W	BAR 4 Control [BAR4C]	Specifies the configuration of BAR 4. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h0

Bits	SW	Name	Description	Reset
12:8	R/W	BAR 5 Aperture [BAR5A]	Specifies the aperture of the BAR 5 when it is configured as a 32-bit BAR. For 32-bit BAR 5, the valid encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'h5
15:13	R/W	BAR 5 Control [BAR5C]	Specifies the configuration of BAR 5. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0
20:16	R/W	EXP-ROM BAR Aperture [ERBA]	Specifies the aperture of the Expansion ROM BAR. The encodings are: • 00000–00011 = undefined • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 00110 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010–11111 = undefined	5'h5
21	R/W	EXP-ROM BAR Enable [ERBE]	This bit must be set to enable the Expansion ROM BAR associated with the Function.	0x01
23:22	R	Reserved [R22]	Reserved	0x0
30:24	R	Reserved [R24]	Reserved	0x0

Bits	SW	Name	Description	Reset
31	R/W	Enable Resizable BAR Capability [ERBC]	Setting this bit to 1 enables the Resizable BAR Capability in the PCI Express Configuration Space of the associated Function. When the Resizable BAR Capability is enabled, the apertures of the memory BARs of the corresponding Function are no longer selected by the fields in this register, but by the setting of the registers in the Resizable BAR Capability Structure.	0x0

Virtual Function BAR Configuration Register 0 @0x280

This register specifies the configuration of the VF BARs associated with the Physical Function 0

Table 351: i_pf_0_vf_BAR_config_0_reg

Bits	SW	Name	Description	Reset
4:0	R/W	VF BAR 0 Aperture [VFBAR0A]	Specifies the aperture of the 32-bit VF BAR 0 or 64-bit VF BAR 0-1. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	5'hf
7:5	R/W	VF BAR 0 Control [VFBAR0C]	Specifies the configuration of VF BAR 0. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h6

Bits	SW	Name	Description	Reset
12:8	R/W	VF BAR 1 Aperture [VFBAR1A]	Specifies the aperture of the VF BAR 1 when it is configured as a 32-bit BAR. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'hf
15:13	R/W	VF BAR 1 Control [VFBAR1C]	Specifies the configuration of VF BAR 1. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h4

Bits	SW	Name	Description	Reset
20:16	R/W	VF BAR 2 Aperture [VFBAR2A]	Specifies the aperture of the 32-bit VF BAR 2 or 64-bit VF BAR 2-3. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	5'hf
23:21	R/W	VF BAR 2 Control [VFBAR2C]	Specifies the configuration of VF BAR 2. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h0

Bits	SW	Name	Description	Reset
28:24	R/W	VF BAR 3 Aperture [VFBAR3A]	Specifies the aperture of the VF BAR 3 when it is configured as a 32-bit BAR. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'hf
31:29	R/W	VF BAR 3 Control [VFBAR3C]	Specifies the configuration of VF BAR 3. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0

Virtual Function BAR Configuration Register 1 @0x284

This register specifies the configuration of the VF BARs associated with the Physical Function.

Table 352: i_pf_0_vf_BAR_config_1_reg

Bits	SW	Name	Description	Reset
4:0	R/W	VF BAR 4 Aperture [VFBAR4A]	Specifies the aperture of the 32-bit VF BAR 4 or 64-bit VF BAR 4-5. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	5'hf
7:5	R/W	VF BAR 4 Control [VFBAR4C]	Specifies the configuration of VF BAR 4. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h0

Bits	SW	Name	Description	Reset
12:8	R/W	VF BAR 5 Aperture [VFBAR5A]	Specifies the aperture of the VF BAR 5 when it is configured as a 32-bit BAR. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'hf
15:13	R/W	VF BAR 5 Control [VFBAR5C]	Specifies the configuration of VF BAR 5. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0
31:16	R	Reserved [R16]	Reserved	0x0

Virtual Function BAR Configuration Register 0 @0x288

This register specifies the configuration of the VF BARs associated with the Physical Function 1.

Table 353: i_pf_1_vf_BAR_config_0_reg

Bits	SW	Name	Description	Reset
4:0	R/W	VF BAR 0 Aperture [VFBAR0A]	Specifies the aperture of the 32-bit VF BAR 0 or 64-bit VF BAR 0-1. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	5'hf
7:5	R/W	VF BAR 0 Control [VFBAR0C]	Specifies the configuration of VF BAR 0. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h6

Bits	SW	Name	Description	Reset
12:8	R/W	VF BAR 1 Aperture [VFBAR1A]	Specifies the aperture of the VF BAR 1 when it is configured as a 32-bit BAR. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'hf
15:13	R/W	VF BAR 1 Control [VFBAR1C]	Specifies the configuration of VF BAR 1. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h4

Bits	SW	Name	Description	Reset
20:16	R/W	VF BAR 2 Aperture [VFBAR2A]	Specifies the aperture of the 32-bit VF BAR 2 or 64-bit VF BAR 2-3. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	5'hf
23:21	R/W	VF BAR 2 Control [VFBAR2C]	Specifies the configuration of VF BAR 2. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h0

Bits	SW	Name	Description	Reset
28:24	R/W	VF BAR 3 Aperture [VFBAR3A]	Specifies the aperture of the VF BAR 3 when it is configured as a 32-bit BAR. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'hf
31:29	R/W	VF BAR 3 Control [VFBAR3C]	Specifies the configuration of VF BAR 3. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0

Virtual Function BAR Configuration Register 1 @0x28c

This register specifies the configuration of the VF BARs associated with the Physical Function.

Table 354: i_pf_1_vf_BAR_config_1_reg

Bits	SW	Name	Description	Reset
4:0	R/W	VF BAR 4 Aperture [VFBAR4A]	Specifies the aperture of the 32-bit VF BAR 4 or 64-bit VF BAR 4-5. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB.	5'hf
7:5	R/W	VF BAR 4 Control [VFBAR4C]	Specifies the configuration of VF BAR 4. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h0

Bits	SW	Name	Description	Reset
12:8	R/W	VF BAR 5 Aperture [VFBAR5A]	Specifies the aperture of the VF BAR 5 when it is configured as a 32-bit BAR. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'hf
15:13	R/W	VF BAR 5 Control [VFBAR5C]	Specifies the configuration of VF BAR 5. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0
31:16	R	Reserved [R16]	Reserved	0x0

Virtual Function BAR Configuration Register 0 @0x290

This register specifies the configuration of the VF BARs associated with the Physical Function 2.

Table 355: i_pf_2_vf_BAR_config_0_reg

Bits	SW	Name	Description	Reset
4:0	R/W	VF BAR 0 Aperture [VFBAR0A]	Specifies the aperture of the 32-bit VF BAR 0 or 64-bit VF BAR 0-1. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	5'hf
7:5	R/W	VF BAR 0 Control [VFBAR0C]	Specifies the configuration of VF BAR 0. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h6

Bits	SW	Name	Description	Reset
12:8	R/W	VF BAR 1 Aperture [VFBAR1A]	Specifies the aperture of the VF BAR 1 when it is configured as a 32-bit BAR. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'hf
15:13	R/W	VF BAR 1 Control [VFBAR1C]	Specifies the configuration of VF BAR 1. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h4

Bits	SW	Name	Description	Reset
20:16	R/W	VF BAR 2 Aperture [VFBAR2A]	Specifies the aperture of the 32-bit VF BAR 2 or 64-bit VF BAR 2-3. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	5'hf
23:21	R/W	VF BAR 2 Control [VFBAR2C]	Specifies the configuration of VF BAR 2. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h0

Bits	SW	Name	Description	Reset
28:24	R/W	VF BAR 3 Aperture [VFBAR3A]	Specifies the aperture of the VF BAR 3 when it is configured as a 32-bit BAR. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'hf
31:29	R/W	VF BAR 3 Control [VFBAR3C]	Specifies the configuration of VF BAR 3. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0

Virtual Function BAR Configuration Register 1 @0x294

This register specifies the configuration of the VF BARs associated with the Physical Function.

Table 356: i_pf_2_vf_BAR_config_1_reg

Bits	SW	Name	Description	Reset
4:0	R/W	VF BAR 4 Aperture [VFBAR4A]	Specifies the aperture of the 32-bit VF BAR 4 or 64-bit VF BAR 4-5. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	5'hf
7:5	R/W	VF BAR 4 Control [VFBAR4C]	Specifies the configuration of VF BAR 4. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h0

Bits	SW	Name	Description	Reset
12:8	R/W	VF BAR 5 Aperture [VFBAR5A]	Specifies the aperture of the VF BAR 5 when it is configured as a 32-bit BAR. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110= 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'hf
15:13	R/W	VF BAR 5 Control [VFBAR5C]	Specifies the configuration of VF BAR 5. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0
31:16	R	Reserved [R16]	Reserved	0x0

Virtual Function BAR Configuration Register 0 @0x298

This register specifies the configuration of the VF BARs associated with the Physical Function 3.

Table 357: i_pf_3_vf_BAR_config_0_reg

Bits	SW	Name	Description	Reset
4:0	R/W	VF BAR 0 Aperture [VFBAR0A]	Specifies the aperture of the 32-bit VF BAR 0 or 64-bit VF BAR 0-1. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	5'hf
7:5	R/W	VF BAR 0 Control [VFBAR0C]	Specifies the configuration of VF BAR 0. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h6

Bits	SW	Name	Description	Reset
12:8	R/W	VF BAR 1 Aperture [VFBAR1A]	Specifies the aperture of the VF BAR 1 when it is configured as a 32-bit BAR. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110= 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'hf
15:13	R/W	VF BAR 1 Control [VFBAR1C]	Specifies the configuration of VF BAR 1. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h4

Bits	SW	Name	Description	Reset
20:16	R/W	VF BAR 2 Aperture [VFBAR2A]	Specifies the aperture of the 32-bit VF BAR 2 or 64-bit VF BAR 2-3. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	5'hf
23:21	R/W	VF BAR 2 Control [VFBAR2C]	Specifies the configuration of VF BAR2. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h0

Bits	SW	Name	Description	Reset
28:24	R/W	VF BAR 3 Aperture [VFBAR3A]	Specifies the aperture of the VF BAR 3 when it is configured as a 32-bit BAR. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'hf
31:29	R/W	VF BAR 3 Control [VFBAR3C]	Specifies the configuration of VF BAR 3. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0

Virtual Function BAR Configuration Register 1 @0x29c

This register specifies the configuration of the VF BARs associated with the Physical Function.

Table 358: i_pf_3_vf_BAR_config_1_reg

Bits	SW	Name	Description	Reset
4:0	R/W	VF BAR 4 Aperture [VFBAR4A]	Specifies the aperture of the 32-bit VF BAR 4 or 64-bit VF BAR 4-5. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB • 11001 = 4 GB • 11010 = 8 GB • 11011 = 16 GB • 11100 = 32 GB • 11101 = 64 GB • 11110 = 128 GB • 11111 = 256 GB	5'hf
7:5	R/W	VF BAR 4 Control [VFBAR4C]	Specifies the configuration of VF BAR 4. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	3'h0

Bits	SW	Name	Description	Reset
12:8	R/W	VF BAR 5 Aperture [VFBAR5A]	Specifies the aperture of the VF BAR 5 when it is configured as a 32-bit BAR. The encodings are: • 00000 = 128 B • 00001 = 256 B • 00010 = 512 B • 00011 = 1 KB • 00100 = 2 KB • 00101 = 4 KB • 00110 = 8 KB • 00111 = 16 KB • 01000 = 32 KB • 01001 = 64 KB • 01010 = 128 KB • 01011 = 256 KB • 01100 = 512 KB • 01101 = 1 MB • 01110 = 2 MB • 01111 = 4 MB • 10000 = 8 MB • 10001 = 16 MB • 10010 = 32 MB • 10011 = 64 MB • 10100 = 128 MB • 10101 = 256 MB • 10110 = 512 MB • 10111 = 1 GB • 11000 = 2 GB	5'hf
15:13	R/W	VF BAR 5 Control [VFBAR5C]	Specifies the configuration of VF BAR 5. The various encodings are: • 000: Disabled • 001–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	3'h0
31:16	R	Reserved [R16]	Reserved	0x0

Physical Function Configuration Register @0x2c0

This register contains the enable bits for all the Functions implemented by the Controller. Resetting the enable bit of a Function disables the Function from responding to configuration requests.

Table 359: i_pf_config_reg

Bits	SW	Name	Description	Reset
0	R	Function 0 Enable [F0E]	Enable for Function 0. This bit is hardwired to 1.	0x01
1	R/W	Function 1 Enable [F1E]	Enable for Function 1. This bit can be modified from the local management bus.	0x01
2	R/W	Function 2 Enable [F2E]	Enable for Function 2. This bit can be modified from the local management bus.	0x01
3	R/W	Function 3 Enable [F3E]	Enable for Function 3. This bit can be modified from the local management bus.	0x01
31:4	R	Reserved [R]	Reserved	0x0

Root Complex BAR Configuration Register @0x300

The root complex side of the Controller contains two memory BARs that can be used for address range checking of incoming requests from devices connected to it. The fields in this register determine the configuration of these BARs.

Table 360: i_rc_BAR_config_reg

Bits	SW	Name	Description	Reset
5:0	R/W	RC BAR 0 Aperture [RCBAR0A]	This field specifies the aperture of the RC BAR 0. The encodings are: • 0000 = 4, • 00001 = 8B, • ..... • 01_1111 = 8G, • 10_0100 = 256G.	0x14
8:6	R/W	RC BAR 0 control [RCBAR0C]	Specifies the configuration of RC BAR 0. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110: 64-bit memory BAR, non-prefetchable • 111: 64-bit memory BAR, prefetchable	0x4
13:9	R/W	RC BAR 1 Aperture [RCBAR1A]	This field specifies the aperture of the RC BAR 1. The encodings are: • 0000 = 4, • 00001 = 8B, • ..... • 1_1101 = 2G	0x14
16:14	R/W	RC BAR 1 control [RCBAR1C]	Specifies the configuration of RC BAR 1. The various encodings are: • 000: Disabled • 001: 32-bit I/O BAR • 010–011: Reserved • 100: 32-bit memory BAR, non-prefetchable • 101: 32-bit memory BAR, prefetchable • 110–111: Reserved	0x0
17	R/W	Type 1 cfg prefetchable mem bar enable [RCBARPME]	Enable for Prefetchable memory base and limit registers in type 1 config space	0x0
18	R/W	Type 1 cfg prefetchable mem bar size [RCBARPMS]	Width of Prefetchable Memory Base and Limit registers in type 1 config space. • 0 = 32 bits • 1 = 64bits	0x0
19	R/W	Type 1 cfg I/O bar enable [RCBARPIE]	Enable for I/O Base and Limit registers in type 1 config space	0x0
20	R/W	Type 1 cfg I/O bar size [RCBARPIS]	Width of I/O Base and Limit registers in type 1 config space. • 0 = 32 bits • 1 = 64bits	0x0
30:21	R	Reserved [R10]	Reserved	0x0
31	R/W	RC BAR Check Enable [RCBCE]	This bit must be set to 1 to enable BAR checking in the RC mode. When this bit is set to 0, the Controller will forward all incoming memory requests to the client logic without checking their address ranges.	0x0

Gen 3 Default TX Preset and Rx Preset Hint Register @0x360

This is register specifies the default transmitter preset and default receiver preset hint used by Controller for lanes that have not received EQ TS2s during Recovery.RcvrConfig LTSSM state.

Table 361: i_gen3_default_preset_reg

Bits	SW	Name	Description	Reset
3:0	R/W	Default Transmitter Preset [GDTXP]	Default transmitter preset value used for a lane that did not receive EQ TS2 in Recovery.RcvrCfg LTSSM state.	0x0
6:4	R/W	Default Receiver Preset Hint [GDRXPH]	Default receiver preset hint value used for a lane that did not receive EQ TS2 in Recovery.RcvrCfg LTSSM state.	0x0
7	R	Reserved [R7]	Reserved	0x0
18:8	R/W	Supported 8G Preset [S8GPR]	This register can be used to program the Presets that are supported by local Transmitter at 8Gbps. Default value of this register is determined by the SUPPORTED_PRESET strap input. *Note:* At 8.0 GT/s and 16.0 GT/s all preset values must be supported for Full swing signaling. Reduced swing signaling must implement presets #4, #1, #9, #5,#6, and #3.	11'h7ff
31:19	R	Reserved [R31]	Reserved	0x0

Gen 3 Gen4 Link Equalization 2ms Timeout Tuning Register @0x364

This register is used to tune the time spent for evaluation per TX Setting in Endpoint Phase 2 (RC Mode Phase 3) of GEN3, GEN4 Link Equalization. The PCIe Spec defines a timeout of 2ms per TX setting and hence the default value for this register is set to 2ms. This can be tweaked based on the total number of iterations done and the time required for the PHY to respond with feedback for RXEQEVAL request. The total time taken in Endpoint Phase 2 (RC Mode Phase 3) must be less than 24 ms as defined by spec. Guideline: (Total Number of iterations)*(link_eq_timeout_2ms_reg + max time required for PHY to respond to RXEQEVAL) less than 24ms

Table 362: i_gen3_gen4_link_eq_timeout_2ms_reg

Bits	SW	Name	Description	Reset
27:0	R/W	Link Equalization Timeout 2ms [LEQT2ms]	Time spent for evaluation per TX Setting in Endpoint Phase 2 (RC Mode Phase 3) of Link Equalization specified in multiples of 16ns. For example: The value 125000 will result in 125000*16ns = 2ms. Simulation with reduced time mode (PCIE_SIM define) will give a smaller value of 300 as power on reset value.	0x1E880
28	R	Reserved [R28]	Reserved	0x0
29	R/W	RXEQINPROGRESS Abort Disable [RXEQABD]	In an unexpected case where the PIPE_PCLK stops due to error in equalization, this bit can be set to de-couple RxEqInProgress from the rest of the equalization state machine. This bit should not be set for normal usage.	0x0

Bits	SW	Name	Description	Reset
31:30	R/W	RXEQINPROGRESS Abort Timer Mode Control [RXEQABM]	When a 24 ms timeout occurs in the LTSSM Equalization Phase 2 (EP Mode) or Phase 3 (RP Mode), the Controller aborts Equalization Phase 2 (EP Mode)/Phase 3 (RP Mode) and transitions to Recovery.Speed. In this case, theRxEqEval output on the PIPE Interface will be de-asserted immediately (if it was asserted). The RxEqInProgress output will stay high and waits for PhyStatus pulse. Controller implements a timer to select an upper limit to wait for this PhyStatus pulse during an abort to de-assert RxEqInProgress. • 00: Wait for a maximum of 4 PIPE_PCLK period. • 01: Wait for a maximum of 8 PIPE_PCLK period. • 10: Wait for a maximum of 16 PIPE_PCLK period. • 11: Disabled. Wait until PhyStatus Pulse is received. *Note:* This register is used only if RxEqEval was asserted when LTSSM 24ms timeout occured in Equalization.	0x3

PIPE FIFO Latency Control Register @0x368

This is register includes bits to control pipe FIFO latency

Table 363: i_pipe_fifo_latency_ctrl_reg

Bits	SW	Name	Description	Reset
0	R/W	Disable PIPE TX FIFOCentering on Empty [DPTFCE]	By default, if FIFO empty is reached, the PIPE TX FIFO accumulates two entries before reading the FIFO again. This is to prevent FIFO from reaching empty again. This bit must remain at 0 to allow the PIPE TX FIFO to recover effectively from a Empty condition.	0x0
1	R/W	Reserved [DPRFLR]	Reserved. Must be 1'b1 for functional mode.	0x1
14:2	R	Reserved [R14]	Reserved	0x0
15	R/W	Disable PIPE TX FIFO Write Idle Filter [DPTFWF]	This bit can be used to prevent PIPE_TX_FIFO from reaching full during TX Electrical Idle. • 0: During TX Electrical Idle, the PIPE_TX_FIFO is kept at half fill level by filtering the writes into the PIPE_TX_FIFO. • 1: The PIPE_TX_FIFO write filtering logic is turned off. Default value of this bit is 1.	0x1
31:16	R	Reserved [R31]	Reserved	0x0

Gen 4 Default TX Preset Register @0x374

This is register specifies the default transmitter preset and default receiver preset hint used by Controller for lanes that have not received 16G EQ TS2s during Recovery.RcvrConfig LTSSM state.

Table 364: i_gen4_default_preset_reg

Bits	SW	Name	Description	Reset
3:0	R/W	Default Gen4 Transmitter Preset [GDTXP]	Default Gen4 transmitter preset value used for a lane that did not receive 16G EQ TS2 in Recovery.RcvrCfg LTSSM state.	0x0
6:4	R	Reserved [R6]	Reserved	0x0
7	R	Reserved [R7]	Reserved	0x0
18:8	R/W	Supported 16G Preset [S16GPR]	This register can be used to program the Presets that are supported by local Transmitter at 16Gbps. Default value of this register is determined by the SUPPORTED_PRESET strap input. *Note:* At 8.0 GT/s and 16.0 GT/s all preset values must be supported for Full swing signaling. Reduced swing signaling must implement presets #4, #1, #9, #5,#6, and #3.	11'h7ff

Bits	SW	Name	Description	Reset
31:19	R	Reserved [R31]	Reserved	0x0

PHY register 3, used in GEN4 @0x378

This is register specifies the PHY Specific registers for used in Gen4.

Table 365: i_phy_config_reg3

Bits	SW	Name	Description	Reset
7:0	R/W	Transmitted FTS Count at 16 GT/s Speed [TFC4]	FTS count transmitted by the Controller in TS1/TS2 sequences during link training. This value must be set based on the time needed by the receiver to acquire sync while exiting from L0S state at 16 GT/s speed.	0x80
31:8	R	Reserved [R24]	Reserved	0x0

Gen 3 Gen 4 Link Equalization Control Register @0x37c

This register is used to Control GEN3, GEN4 Link Equalization Procedure.

Table 366: i_gen3_gen4_link_eq_ctrl_reg

Bits	SW	Name	Description	Reset
2:0	R/W	Max Eval Convergence Count [MXECC]	Controls the number of consecutive RxEqEval iterations with direction change feedback of 00s before Equalization Convergence is inferred. • 0 : Infer Convergence after 1 feedback of 000000 • 1 : Infer Convergence after 2 feedback of 000000 • 2 : Infer Convergence after 3 consecutive feedback of 000000. • 7 : Infer Convergence after 8 consecutive feedback of 000000. *Note:* Each lane independently counts consecutive feedback of 000000. *Note:* Count is reset after a non-000000 feedback on each lane.	0x0
3	R/W	Disable Max Eval Iteration [DMEI]	The MAX_EVAL_ITERATION input controls the maximum number of iterations in Equalization Phase2 (EP) or Phase3 (RP). This bit can be used to mask the MAX_EVAL_ITERATION and perform more iterations till Convergence or a 24ms timeout.	0x0
4	R/W	EP 8GTs Request Equalization Retrain Link [EP8GRE]	This bit can be used by Endpoint Device FW to request for 8GT/s Equalization redo. This bit can be set at any time after the Link is Up. Writing a 1 into this field results in the Controller to transition to Recovery. The Request Equalization bit in TS2 Ordered Sets will be set to 1 in Recovery.Rcvr.Cfg to request equalization at 8GTs. This bit is auto-cleared by the internal logic of the Controller after the re-training has been completed and link has reached the L0 state. This bit is also auto-cleared when not in Gen3 or Gen4. Device Firmware must wait for the bit to be clear before any subsequent retrain requests.	0x0
5	R/W	EP 16GTs Request Equalization Retrain Link [EP16GRE]	Writing a 1 into this field results in the Controller to transition to Recovery. The Request Equalization bit and Equalization Request Data Rate bit in TS2 Ordered Sets will be set to 1 in Recovery.Rcvr.Cfg to request equalization at 16GTs. This bit is auto-cleared by the internal logic of the Controller after the re-training has been completed and link has reached the L0 state. This bit is also auto-cleared when not in Gen3 or Gen4. Device Firmware must wait for the bit to be clear before any subsequent requests.	0x0
6	R	Reserved [RES6]	Reserved	0x0
7	R	Reserved [RES7]	Reserved	0x0

Bits	SW	Name	Description	Reset
8	R/W	Quiesce Guarantee 8GTs [QG8GT]	This bit can be used to program the Quiesce Guarantee bit of the TS2 in Recovery.Rcvr.Cfg state during 8GT/s Request Equalization.	0x0
9	R/W	Quiesce Guarantee 16GTs [QG16GT]	This bit can be used to program the Quiesce Guarantee bit of the TS2 in Recovery.Rcvr.Cfg state during 16GT/s Request Equalization.	0x0
10	R	Reserved [RES10]	Reserved	0x0
11	R	Reserved [RES11]	Reserved	0x0
15:12	R/W	Max 8GTs Equalization Request Limit [MX8GERL]	This register is used during error scenario where the coefficients at the end of Equalization mismatch with the coefficients agreed during Equalization. If Recovery.RcvrLock was entered from Recovery.Equalization, the Upstream Port must evaluate the equalization coefficients or preset received by all Lanes that receive eight TS1 Ordered Sets and note whether they are different from the final set of coefficients or preset that was accepted in Phase 2 of the equalization process. *Note:* Mismatches are reported in Recovery.RcvrCfg by setting the Request Equalization bit of TS2 Ordered Sets. The number of 8GT/s Equalization Requests must be finite as per PCIe specification. This register can be used to program the maximum numberof 8GT/s equalization requests automatically initiated by the Endpoint. • 0000: Automatic 8GT/s Equalization Request Disabled. • 0001: Automatic 8GT/s Equalization request limit is 1. • 0010: Automatic 8GT/s Equalization request limit is 2. • 1111: Automatic 8GT/s Equalization requestlimit is 15.	0x0
19:16	R/W	Max 16GTs Equalization Request Limit [MX16GERL]	This register is used during error scenario where the coefficients at the end of Equalization mismatch with the coefficients agreed during Equalization. If Recovery.RcvrLock was entered from Recovery.Equalization, the Upstream Port must evaluate the equalization coefficients or preset received by all Lanes that receive eight TS1 Ordered Sets and note whether they are different from the final set of coefficients or preset that was accepted in Phase 2 of the equalization process. *Note:* Mismatches are reported in Recovery.RcvrCfg by setting theRequest Equalization bit of TS2 Ordered Sets. The number of 16GT/s Equalization Requests must be finite as per PCIe specification. This register can be used to program the maximum number of 16GT/s equalization requests automaticallyinitiated by the Endpoint. • 0000: Automatic 16GT/s Equalization Request Disabled. • 0001: Automatic 16GT/s Equalization request limit is 1. • 0010: Automatic 16GT/s Equalization request limit is 2. • 1111: Automatic 16GT/s Equalization request limit is 15.	0x0
23:20	R	Reserved [RES20]	Reserved	0x0
30:24	R	Reserved [RES24]	Reserved	0x0
31	R/W	Enable Retry RXEQEVAL After Feedback Error [EREVFBER]	When the Controller receives a direction change feedback from the PHY, the feedback is applied to the current coefficients and checked for errors. During Equalization Phase2(EP) or Phase3(RP), 1 iteration is defined as (Number of Preset Feedback) + (Number of pipe_rxeqeval assertions). This bit controls the device feedback in an iteration in case of direction change errors: • 0: If feedback is invalid, then the Controller, discards the feedback and does not assert PIPE_INVALIDREQUEST and does not retry PIPE_RXEQEVAL in same iteration. The coefficient settings is kept unchanged in the iteration. Retry PIPE_RXEQEVAL in next iteration. • 1: If feedback is invalid, then the Controller asserts PIPE_INVALIDREQUEST to PHY, discards the feedback and retries PIPE_RXEQEVAL in same iteration till a valid feedback is received.	0x0

Gen 3 Link Equalization Debug Register @0x380

This register is used to reflect the negotiated TX Preset, Coefficients at the end of GEN3 Link Equalization. When the Controller is an Endpoint, this register reflects the Preset/Coefficients applied to the Endpoint Transmitter at the end of Gen3 Equalization Phase 3. The value in these registers is valid only after link has reached Gen3 L0 state (i.e., only after Gen3 Equalization is completed). The actual value read out will be based on the equalization and can vary based on the equalization process. When the Controller is an RC, this register reflects the Preset/ Coefficients applied to the RC Transmitter at the end of Gen3 Equalization Phase 2.

Table 367: i_gen3_link_eq_debug_status_reg_lane0

Bits	SW	Name	Description	Reset
3:0	R	Link Equalization TX Preset [LEQTXPR]	TX Preset agreed upon for this lane.	0x0
4	R	Link Equalization TX Preset Valid [LEQTXPRV]	TX Preset Valid Indicator. This bit is set when a TX Preset is received in TS1s with the use_preset bit set in Endpoint Mode Phase 3 or RC Mode Phase 2.	0x0
7:5	R	Reserved [RES75]	Reserved	0x0
25:8	R	Link Equalization TX Coefficient [LEQTXCO]	TX Coefficients agreed upon for this lane. • [25:20] : Post Cursor Coefficient • [19:14] : Cursor Coefficient • [13:8] : Pre-Cursor Coefficient	0x00000
31:26	R	Reserved [RES3126]	Reserved	0x0

Gen 3 Link Equalization Debug Register @0x384

This register is used to reflect the negotiated TX Preset, Coefficients at the end of GEN3 Link Equalization. When the Controller is an Endpoint, this register reflects the Preset/Coefficients applied to the Endpoint Transmitter at the end of Gen3 Equalization Phase 3. The value in these registers is valid only after link has reached Gen3 L0 state (i.e., only after Gen3 Equalization is completed). The actual value read out will be based on the equalization and can vary based on the equalization process. When the Controller is an RC, this register reflects the Preset/ Coefficients applied to the RC Transmitter at the end of Gen3 Equalization Phase 2.

Table 368: i_gen3_link_eq_debug_status_reg_lane1

Bits	SW	Name	Description	Reset
3:0	R	Link Equalization TX Preset [LEQTXPR]	TX Preset agreed upon for this lane.	0x0
4	R	Link Equalization TX Preset Valid [LEQTXPRV]	TX Preset Valid Indicator. This bit is set when a TX Preset is received in TS1s with the use_preset bit set in Endpoint Mode Phase 3 or RC Mode Phase 2.	0x0
7:5	R	Reserved [RES75]	Reserved	0x0
25:8	R	Link Equalization TX Coefficient [LEQTXCO]	TX Coefficients agreed upon for this lane. • [25:20] : Post Cursor Coefficient • [19:14] : Cursor Coefficient • [13:8] : Pre-Cursor Coefficient	0x00000
31:26	R	Reserved [RES3126]	Reserved	0x0

Gen 3 Link Equalization Debug Register @0x388

This register is used to reflect the negotiated TX Preset, Coefficients at the end of GEN3 Link Equalization. When the Controller is an Endpoint, this register reflects the Preset/Coefficients

applied to the Endpoint Transmitter at the end of Gen3 Equalization Phase 3. The value in these registers is valid only after link has reached Gen3 L0 state (i.e., only after Gen3 Equalization is completed). The actual value read out will be based on the equalization and can vary based on the equalization process. When the Controller is an RC, this register reflects the Preset/ Coefficients applied to the RC Transmitter at the end of Gen3 Equalization Phase 2.

Table 369: i_gen3_link_eq_debug_status_reg_lane2

Bits	SW	Name	Description	Reset
3:0	R	Link Equalization TX Preset [LEQTXPR]	TX Preset agreed upon for this lane.	0x0
4	R	Link Equalization TX Preset Valid [LEQTXPRV]	TX Preset Valid Indicator. This bit is set when a TX Preset is received in TS1s with the use_preset bit set in Endpoint Mode Phase 3 or RC Mode Phase 2.	0x0
7:5	R	Reserved [RES75]	Reserved	0x0
25:8	R	Link Equalization TX Coefficient [LEQTXCO]	TX Coefficients agreed upon for this lane. • [25:20] : Post Cursor Coefficient • [19:14] : Cursor Coefficient • [13:8] : Pre-Cursor Coefficient	0x00000
31:26	R	Reserved [RES3126]	Reserved	0x0

Gen 3 Link Equalization Debug Register 0x38c

This register is used to reflect the negotiated TX Preset, Coefficients at the end of GEN3 Link Equalization. When the Controller is an Endpoint, this register reflects the Preset/Coefficients applied to the Endpoint Transmitter at the end of Gen3 Equalization Phase 3. The value in these registers is valid only after link has reached Gen3 L0 state (i.e., only after Gen3 Equalization is completed). The actual value read out will be based on the equalization and can vary based on the equalization process. When the Controller is an RC, this register reflects the Preset/ Coefficients applied to the RC Transmitter at the end of Gen3 Equalization Phase 2.

Table 370: i_gen3_link_eq_debug_status_reg_lane3

Bits	SW	Name	Description	Reset
3:0	R	Link Equalization TX Preset [LEQTXPR]	TX Preset agreed upon for this lane.	0x0
4	R	Link Equalization TX Preset Valid [LEQTXPRV]	TX Preset Valid Indicator. This bit is set when a TX Preset is received in TS1s with the use_preset bit set in Endpoint Mode Phase 3 or RC Mode Phase 2.	0x0
7:5	R	Reserved [RES75]	Reserved	0x0
25:8	R	Link Equalization TX Coefficient [LEQTXCO]	TX Coefficients agreed upon for this lane. • [25:20] : Post Cursor Coefficient • [19:14] : Cursor Coefficient • [13:8] : Pre-Cursor Coefficient	0x00000
31:26	R	Reserved [RES3126]	Reserved	0x0

Gen 4 Link Equalization Debug Register @0x3c0

This register is used to reflect the negotiated TX Preset, Coefficients at the end of GEN4 Link Equalization. When the Controller is an Endpoint, this register reflects the Preset/Coefficients applied to the Endpoint Transmitter at the end of Gen4 Equalization Phase 3. When the Controller is an RC, this register reflects the Preset/Coefficients applied to the RC Transmitter at the end of Gen4 Equalization Phase 2.

Table 371: i_gen4_link_eq_debug_status_reg_lane0

Bits	SW	Name	Description	Reset
3:0	R	Link Equalization TX Preset [LEQTXPR]	TX Preset agreed upon for this lane.	0x8
4	R	Link Equalization TX Preset Valid [LEQTXPRV]	TX Preset Valid Indicator. This bit is set when a TX Preset is received in TS1s with the use_preset bit set in Endpoint Mode Phase 3 or RC Mode Phase 2.	0x0
7:5	R	Reserved [RES75]	Reserved	0x0
25:8	R	Link Equalization TX Coefficient [LEQTXCO]	TX Coefficients agreed upon for this lane. • [25:20] : Post Cursor Coefficient • [19:14] : Cursor Coefficient • [13:8] : Pre-Cursor Coefficient	18'b00011010000100011
31:26	R	Reserved [RES3126]	Reserved	0x0

Gen 4 Link Equalization Debug Register @0x3c4

This register is used to reflect the negotiated TX Preset, Coefficients at the end of GEN4 Link Equalization. When the Controller is an Endpoint, this register reflects the Preset/Coefficients applied to the Endpoint Transmitter at the end of Gen4 Equalization Phase 3. When the Controller is an RC, this register reflects the Preset/Coefficients applied to the RC Transmitter at the end of Gen4 Equalization Phase 2.

Table 372: i_gen4_link_eq_debug_status_reg_lane1

Bits	SW	Name	Description	Reset
3:0	R	Link Equalization TX Preset [LEQTXPR]	TX Preset agreed upon for this lane.	0x8

Gen 4 Link Equalization Debug Register @0x3c8

This register is used to reflect the negotiated TX Preset, Coefficients at the end of GEN4 Link Equalization. When the Controller is an Endpoint, this register reflects the Preset/Coefficients applied to the Endpoint Transmitter at the end of Gen4 Equalization Phase 3. When the Controller is an RC, this register reflects the Preset/Coefficients applied to the RC Transmitter at the end of Gen4 Equalization Phase 2.

Table 373: i_gen4_link_eq_debug_status_reg_lane2

Bits	SW	Name	Description	Reset
3:0	R	Link Equalization TX Preset [LEQTXPR]	TX Preset agreed upon for this lane.	0x8
4	R	Link Equalization TX Preset Valid [LEQTXPRV]	TX Preset Valid Indicator. This bit is set when a TX Preset is received in TS1s with the use_preset bit set in Endpoint Mode Phase 3 or RC Mode Phase 2.	0x0
7:5	R	Reserved [RES75]	Reserved	0x0
25:8	R	Link Equalization TX Coefficient [LEQTXCO]	TX Coefficients agreed upon for this lane. • [25:20] : Post Cursor Coefficient • [19:14] : Cursor Coefficient • [13:8] : Pre-Cursor Coefficient	18'b00011010000
31:26	R	Reserved [RES3126]	Reserved	0x0

Gen 4 Link Equalization Debug Register @0x3cc

This register is used to reflect the negotiated TX Preset, Coefficients at the end of GEN4 Link Equalization. When the Controller is an Endpoint, this register reflects the Preset/Coefficients applied to the Endpoint Transmitter at the end of Gen4 Equalization Phase 3. When the Controller is an RC, this register reflects the Preset/Coefficients applied to the RC Transmitter at the end of Gen4 Equalization Phase 2.

Table 374: i_gen4_link_eq_debug_status_reg_lane3

Bits	SW	Name	Description	Reset
3:0	R	Link Equalization TX Preset [LEQTXPR]	TX Preset agreed upon for this lane.	0x8
4	R	Link Equalization TX Preset Valid [LEQTXPRV]	TX Preset Valid Indicator. This bit is set when a TX Preset is received in TS1s with the use_preset bit set in Endpoint Mode Phase 3 or RC Mode Phase 2.	0x0
7:5	R	Reserved [RES75]	Reserved	0x0
25:8	R	Link Equalization TX Coefficient [LEQTXCO]	TX Coefficients agreed upon for this lane. • [25:20] : Post Cursor Coefficient • [19:14] : Cursor Coefficient • [13:8] : Pre-Cursor Coefficient	18'b00011010000100011
31:26	R	Reserved [RES3126]	Reserved	0x0

ECC Correctable Error Count Register for AXI RAMs @0xc80

This register contains the count of the number of ECC errors detected and corrected during reads from PCIe core AXI external RAMs.

Table 375: i_ecc_corr_err_count_reg_axi

Bits	SW	Name	Description	Reset
7:0	R/ WOCLR	AXI slave reorder RAM ECC correctable error count [REORDER_CER]	Number of correctable errors detected while reading from the AXI slave re-order RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.	0x0
15:8	R/ WOCLR	AXI slave write FIFO RAM ECC correctable Error Count [AXI_SLAVE_WFIFO_CER]	Number of correctable errors detected while reading from the AXI slave write FIFO RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.	0x0
23:16	R/ WOCLR	AXI master read FIFO RAM ECC correctable Error Count [AXI_MASTER_RFIFO_CER]	Number of correctable errors detected while reading from the AXI master read FIFO RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.	0x0
31:24	R	Reserved [R31_24]	Reserved	0x0

Low Power Debug and Control Register 0 @0xc88

This register controls internal behavior of controller for low power operations. Adjustment of this register is not required for normal operations.

Table 376: low_power_debug_and_control0

Bits	SW	Name	Description	Reset
23:0	R/W	L1 substate entry delay [L1XDELAY]	Normaly L1 substate entry process is initiated immedaitely after LTSSM enters L1. A delay in micro-seconds can be given in this field todelay L1 substate entry process. This timeout has 0-1 µs margin of error.	0x0

Bits	SW	Name	Description	Reset
24	R/W	Do Not block Request interface [L1DBRI]	Before entering L1, controller internally blocks all TLP and Register Request interface entering controller. interfaces are internally unblocked while exiting L1. This field control this behavior. '1' in this field makes the controler to do not perform any blocking to interfaces. '0' makes the controller behaves normaly. This is required onlyfor debug purpose. Power shutoff feature has to be disabled while using this field.	0x0
26:25	R	L1 entry mode [L1EM]	This field shows the last entered L1 mode. This is useful for debug. • Bit 0 - Entry mode was ASPM. • Bit 1 - Entry mode was PM. This is reset before any new L1 entry.	0x0
27	R/W	Disable L1 exit upon Pending Tlps [L1DLEUP]	Pending Tlps trigger a L1 exit by default. This includes internaly generated messages and internaly blocked TLPs. Setting this bit changes the default behavior. This is required only for debug purpose.	0x0
31:28	R	RSVD	RSVD	4'h0

Low Power Debug and Control Register 1 @0xc8c

This register controls internal behavior of controller for low power operations. Adjustment of this register is not required for normal operations.

Table 377: low_power_debug_and_control1

Bits	SW	Name	Description	Reset
7:0	R	L1 or L1.x Exit Trigger conditions [L1ER]	This field shows the values of possible L1 or L1-substate exit triggers. This is useful for debug. This is captured during L1 or L1-substate exit process. This field is reset during L1 entry. • 0 : CLIENT_REQ_EXIT_L1 asserted; • 1 : Electrical Idle exit detected at link. • 2 : New TLP request detected. • 3 : Internal request to send TLP. This includes CFG completions, internal messages, and INTx messages. • 4 : Pending TX traffic available. This could be traffic from DMA and blocked traffic due to credits at AXI. • 5 : #CLKREQ assert detected. • 6 : CLIENT_REQ_EXIT_L1_SUBSTATE asserted • 7 : Reg Access request detected. Triggers #5,6,7 are valid only with L1-substate supported configs.	0x0
31:8	R	RSVD	RSVD	24'h000000

Low Power Debug and Control Register 2 @0xc90

This register controls internal behavior of controller for low power operations. Adjustment of this register is not required for normal operations.

Table 378: low_power_debug_and_control2

Bits	SW	Name	Description	Reset
23:0	R/W	Timeout while waiting for RX IDLE and OUTSTANDING Idle [L1TWROI]	This field enables a timeout mechanism while waiting for RX buffers and Outstanding Pkts before turning off power. Controller enters L1 substate after timeout. A value of 0x0 disables this timeout mechanism. Controller do not select internal power shutoff if it enters L1.x with this timeout. User can give timeout in micro-seconds using this register. This field is ignored if L1 substate is disabled.	0x0
24	R	RSVD	RSVD	1'h0

Bits	SW	Name	Description	Reset
25	R/W	Enable outstanding CPL check [L1EOC]	Enable waiting for outstanding completions before entering L1.x. Outstanding packets expected from PCIe link as well as from AXI side is checked.FOR HAL configurations client has to assert PREVENT_L1x_ENTRY signal to prevent L1x entry. This only a tuning register. Not setting this register will cause controller to enter L1.x to save power without checking this. Controller exit from L1.x as soon as it receives expected TLps. This field is ignored if Power shutoff mechanism isselected for L1.x and Controller will always wait for outstanding packets before turning off internal power(with cpf flow). If timeout is enabled, controller enters L1.x without internal power shutoff after timeout. This bit is ignored if L1 substate is disabled.	0x0
26	R/W	Enable RX path check [L1ERC]	Enables waiting for RX path IDLE condition before entering L1.x. This checks that all packets from PCIE link has reached client side before entering L1.x. This only a tuning register. Not setting this register will cause controller to enter L1.x to save power without checking this. Controller will resume transferring RX data once it exit from L1.x state if RX buffers were not empty. This field is ignored if Power shutoff mechanism is enabled for L1.x and Controller will always check RX path idle condition before turning off internal power (with cpf flow). If timeout is enabled, controller enters L1.x without internal power shutoff after timeout. This bit is ignored if L1 substate is disabled.	0x0
27	R	RSVD	RSVD	1'h0
28	R	Timeout occured during RX and outstanding wait [L1TROW]	This is a debug status field. '1' in this field indicates that a timeout has occured while waiting for RX path or OUTstanding packet IDLE conditions. This is cleared on new entry to L1.	0x0
29	R/W	Disable Autonomous L1.x exit upon reg access [L1DAET]	L1.x turns off clocks to the controller. Default behavior is made to exit L1.x if Register access request is present at register interface. Setting this bit disables this feature. If this bit is set and CLKREQ_IN_N is 1(de-asserted), Controller responds with ERROR response to APB requests. Client can use CLIENT_EXIT_L1_SUBSTATE pin to trigger L1.x exit if autonomous exit is disabled for register access. This bit is ignored if L1 substate is disabled.	0x1
30	R/W	Client supplies slow clock to core during L1 [L1CSC]	L1-substate removes CORE_CLK. since the registers are implemented in core-clk, register access is not possible during L1-substate. If client can supply a slow clock to core (CORE_CLK) during L1-substates, APB/mgmt access is possiblein L1.x. set this bit if client can supply slow clock to CORE_CLK when CLKREQ_IN_N is 1(de-asserted). If this bit is set, Controller neither wake-up from L1 or generate error response for APB access during L1.x. Controller behavior is undefined if register write is performed whileslow clock is supplied to core_clk. Recommended flow is to first exit from L1-substate and perform register writes.	0x0
31	R	RSVD	RSVD	1'h0

Transaction Layer Internal Control Register @0xc94

This register controls internal behavior of Transaction layer of controller. Adjustment of this register is not required for normal operations.

Table 379: tl_internal_control

Bits	SW	Name	Description	Reset
0	R/W	Enable CRS under FLR [ECFLR]	By default controller ignores config request if a function is under going FLR. Setting this bit makes the controller to respond with CRS response.	0x0
1	R/W	Disable Outbound Ordering Check [DOOC]	Ordering between outbound Completions and posted packets are maintainted in transaction layer. This is achieved by blocking Completions if required. Completions arrived after EOP of a posted packet are blocked till that posted packet is transmitted. This Ordering checkis required to conform to the PCIe ordering rules. This ordering check can be disabled by setting this field.	0x1
31:2	R	RSVD	RSVD	30'h00000000

Scaled Flow Control management Register @0xcc4

Scaled Flow Control management register. For multi-VC configurations, this register accesses the VC selected in Scaled Flow Control VC Select register.

Table 380: i_scaled_flow_control_mgmt_reg

Bits	SW	Name	Description	Reset
1:0	R/W	Local Posted Header Credit Scale [LPHCS]	This register can be used to program the Posted Header Credit Scale that will be advertised by the Controller.	0x1
3:2	R/W	Local Posted Payload Credit Scale [LPPCS]	This register can be used to program the Posted Payload Credit Scale that will be advertised by the Controller.	0x1
5:4	R/W	Local Non-Posted Header Credit Scale [LNPHCS]	This register can be used to program the Non-Posted Header Credit Scale that will be advertised by the Controller.	0x1
7:6	R/W	Local Non-Posted Payload Credit Scale [LNPPCS]	This register can be used to program the Non-Posted Payload Credit Scale that will be advertised by the Controller.	0x1
9:8	R/W	Local Completion Header Credit Scale [LCHCS]	This register can be used to program the Completion Header Credit Scale that will be advertised by the Controller.	0x1
11:10	R/W	Local Completion Payload Credit Scale [LCPCS]	This register can be used to program the Completion Payload Credit Scale that will be advertised by the Controller.	0x1
15:12	R	Reserved [RES1]	Reserved	0x0
17:16	R	Remote Posted Header Credit Scale [RPHCS]	This register reflects the Posted Header Credit Scale that is advertised by the remote end device during DL Feature Exchange.	0x0
19:18	R	Remote Posted Payload Credit Scale [RPPCS]	This register reflects the Posted Payload Credit Scale that is advertised by the remote end device during DL Feature Exchange.	0x0
21:20	R	Remote Non-Posted Header Credit Scale [RNPHCS]	This register reflects the Non-Posted Header Credit Scale that is advertised by the remote end device during DL Feature Exchange.	0x0
23:22	R	Remote Non-Posted Payload Credit Scale [RNPPCS]	This register reflects the Non-Posted Payload Credit Scale that is advertised by the remote end device during DL Feature Exchange.	0x0
25:24	R	Remote Completion Header Credit Scale [RCHCS]	This register reflects the Completion Header Credit Scale that is advertised by the remote end device during DL Feature Exchange.	0x0
27:26	R	Remote Completion Payload Credit Scale [RCPCS]	This register reflects the Completion Payload Credit Scale that is advertised by the remote end device during DL Feature Exchange.	0x0
31:28	R	Reserved [RES2]	Reserved	0x0

Lane Margining at Receiver Parameters 1 Register @0xcd0

The Lane Margining at Receiver Parameters of the PHY are advertised in this Register.

Table 381: i_margining_parameters_1_reg

Bits	SW	Name	Description	Reset
0	R/W	M VoltageSupported [MVS]	• 1b - Voltage Margining is supported • 0b - Voltage Margining is not supported	0x1
1	R/W	M IndUpDownVoltage [MINDUDVS]	• 1b - Independent Up Down Voltage Margining is supported • 0b - Independent Up Down Voltage Margining is not supported	0x1
2	R/W	M IndLeftRightTimings [MINDLRTS]	• 1b - Independent Left/Right Timing Margining is supported • 0b - Independent Left/Right Timing Margining is not supported	0x1

Bits	SW	Name	Description	Reset
3	R/W	M SampleReporting [MSRM]	• 1b - Sampling Rates M SamplingRateVoltage, M SamplingRateTiming are supported • 0b - Sample Count is supported	0x0
4	R/W	M IndErrorSampler [MIES]	• 1b - Margining will not produce errors (change in the error rate) in data stream (error sampler is independent) • 0b - Margining may produce errors in the data stream	0x1
11:5	R/W	M NumVoltageSteps [MNVS]	Number of voltage steps from default (either up or down), minimum range +/-50 mV as measured by 16.0 GT/s reference equalizer Voltage offset must increase monotonically. The number of steps in both positive and negative direction from the default sample location must be identical This value is undefined if M VoltageSupported is 0b.	0x20
17:12	R/W	M NumTimingSteps [MNTS]	Number of time steps from default (to either left or right), range must be at least +/-0.2 UI. Timing offset must increase monotonically. The numberof steps in both positive (toward the end of the unit interval) and negative (toward the beginning of the unit interval) must be identical.	0x6
23:18	R/W	M MaxTimingOffset [MMTO]	Offset from default at maximum step value as percentage of a nominal UI at 16.0 GT/s A 0 value may be reported if the vendor chooses not to report the offset.	0x14
29:24	R/W	M MaxVoltageOffset [MMVO]	Offset from default at maximum step value as percentage of one volt. A 0 value may be reported if the vendor chooses not to report the offset.	0x5
31:30	R	Reserved [RES]	Reserved	0x0

Lane Margining at Receiver Parameters 2 Register @0xcd4

The Lane Margining at Receiver Parameters of the PHY are advertised in this Register.

Table 382: i_margining_parameters_2_reg

Bits	SW	Name	Description	Reset
5:0	R/W	MSamplingRateVoltage [MSRV]	The ratio of bits tested to bits received during voltage margining. A value of 0 is a ratio of 1:64 (1 bit of every 64 bits received), and a value of 63 is a ratio of 64:64 (all bits received).	0x0
11:6	R/W	MSamplingRateTiming [MSRT]	The ratio of bits tested to bits received during timing margining. A value of 0 is a ratio of 1:64 (1 bit of every 64 bits received), and a value of 63 is a ratio of 64:64 (all bits received).	0x0
16:12	R/W	M MaxLanes [MML]	Maximum number of Lanes minus 1 that can be margined at the same time. It is recommended that this value be greater than or equal to the number of Lanes in the Link minus 1. Encoding Behavior is undefined if software attempts to margin more than MMaxLanes+1 at the same time. *Note:*This value is permitted to exceed the number of Lanes in the Link minus 1.	0x0
31:17	R	Reserved [RES1]	Reserved	0x0

Lane Margining at Receiver Local Control Register @0xcd8

The Lane Margining at Receiver local control fields are implemented in this Register.

Table 383: i_margining_local_control_reg

Bits	SW	Name	Description	Reset
0	R/W	Margining Soft Reset [MSR]	This bit can be used to reset the Margining internal registers and Margining state machines in the Controller. When asserted: **1.** The State machines will be reset to their default values. **2.** All internal FIFOs will be cleared. **3.** All the P2M and M2P registers will be reset. **4.** This does not reset the Margining Configuration and Management Registers. Margining Status register will show the last recorded status. This bit will automatically self-clear after 32-CORE_CLK cycles.	0x0
1	R/W	Accept Margining Command Non-Gen4 [AMCNG4]	By default, the Controller will process a Margin Command only if it is received while in 16GT/ s L0 State. If a Margin Command is received when the link is not in Gen4-L0 state, then the command will be ignored. If this bit is set, then the Controller accepts and stores a margin command that is received when not in Gen4 L0 state. This command will be processed when the link reaches Gen4 L0 state.	0x0
2	R/W	Disable Margin Status Update On Sample Count [DMSUSC]	By default, when a Step Margin command is received, the Controller will update Lane Margin status to Margining in Progress when an Error Count update or a Sample Count update is received from PHY. Set this bit to 1 to not update Lane Margin Status on a Sample Count update from PHY.	0x0
3	R/W	Enable Step Margin Status Update During Clear Error Log Command [ESMSUCE]	• 0: (Default Value) When a Clear Error Log Command is received after a Step Margin Command, the Controller will process the Clear Error Log and respond with Clear Error Log Status. The Step Margin command is still active in the PHY. However, the Step Margin status willnot be reflected in the Margin Status Register since the Margin Control Register holds Clear Error Log Command. Host Margining SW needs to configure the Step Margin Command again in order to get the Step Margin Status. • 1: When this bit is set to1, the Controller waits for Host SW to read the Clear Error Log Status through a CfgRd. After the Host read the Clear Error Log status, the Controller updates the latest Step Margin Status on to the Margin Status Register while the Margin Control Register holds Clear Error Log Command.	0x0
28:4	R	Reserved [RES]	Reserved	0x0
31:29	R/W	Write Ack Wait Timer Control [WAWTC]	When a WriteCommitted command is issued by the Controller, the PHY must respond with a Write_Ack response. The time for which the Controller waits before timing out is controlled by this register. • 000: 10 µs • 001: 100 µs • 010: 1 ms • 011: 2 ms • 100: 10 ms (default) • 101: 20 ms • 110: 100 ms • 111: No Timeout	3'd4

Lane Margining at Receiver Error Status 1 Register @0xcdc

The Lane Margining at Receiver SW Error Status fields are implemented in this Register.

Table 384: i_margining_error_status1_reg

Bits	SW	Name	Description	Reset
15:0	R	Invalid SW Margining Command [ISWMC]	When the Controller receives an Invalid Margining Command from SW in its configuration register, the 16-bit command is logged in this registerfor debug. Only the first Error is logged in this register. This register is valid only when Bit-4, Invalid SW Margining Command Received, of the i_local_error_status_2_register is set. Bit-4 of the i_local_error_status_2_register has to be cleared by local firmware before another error can be logged in this field. .	0x0
19:16	R	Invalid SW Margining Command Lane Number [ISWMCLN]	This field reports the Lane Number for which the Invalid command was received. 0000: Lane 0.0001: Lane 1. and so on. This register is valid only when Bit-4, Invalid SW Margining Command Received, of the i_local_error_status_2_registeris set. Bit-4 of the i_local_error_status_2_register has to be cleared by local firmware before another error can be logged in this field.	0x0
31:20	R	Reserved [RES]	Reserved	0x0

Lane Margining at Receiver Error Status 2 Register @0xce0

The Lane Margining at Receiver PHY Error Status fields are implemented in this Register.

Table 385: i_margining_error_status2_reg

Bits	SW	Name	Description	Reset
7:0	R	Invalid PHY Margining Command [IPHYMC]	When the Controller receives an Invalid Margining Command from PHY over PIPE Interface, the 8-bit PIPE command is logged in this register for debug. Only the first Error is logged in thisregister. This field is valid only when Bit-5, Invalid PHY Margining Command Received, of the i_local_error_status_2_register is set. Bit-5 of the i_local_error_status_2_register has to be cleared by local firmware before another error can be logged in this field. .	0x0
11:8	R	Invalid PHY Margining Command Lane Number [IPHYMCLN]	This field reports the Lane Number for which the Invalid command was received. 0000: Lane 0.0001: Lane 1. and so on. This field is valid only when Bit-5, Invalid PHY Margining Command Received, of the i_local_error_status_2_register is set. Bit-5 of the i_local_error_status_2_register has to be cleared by local firmware before another error can be logged in this field. .	0x0
13:12	R	Reserved [RES12]	Reserved	0x0
17:14	R	Write Ack Wait Timeout Lane Number [WAWTLN]	This field reports the Lane Number for which the Controller detected a 10ms timeout. 0000: Lane 0. 0001: Lane 1. and so on. This field is valid only when Bit-6, Write Ack Wait Timeout Error, of the i_local_error_status_2_register is set. Bit-6 of the i_local_error_status_2_register has to be cleared by local firmware before another error can be logged in this field. .	0x0
21:18	R	Unexpected PHY Response Lane Number [UPRLN]	This field reports the Lane Number for which the Controller received an unexpected PHY Response for Lane Margining. Unexpected PHY Response is detected by Controller if PHY writes to the Margin Status or the Margin NAK bits of RX Margin Status 0 Register when no change in Start Margin or Margin Offset issued by Controller or after the Write Ack Wait Timeout. 0000: Lane 0. 0001: Lane 1. and so on. This field is valid only when Bit-7, Unexpected PHY Response Received, of the i_local_error_status_2_register is set. Bit-7 of the i_local_error_status_2_register has to be cleared by local firmware before another error can be logged in this field. .	0x0
31:22	R	Reserved [RES22]	Reserved	0x0

Local Error and Status 2 Register @0xd00

This is an extension of the Local Error and Status Register. This register contains the status of the various events, errors and abnormal conditions in the Controller. Any of the status bits can be reset by writing a 1 into the bit position. Unless masked by the setting of the Local Interrupt Mask 2 Register, the occurrence of any of these conditions causes the Controller to activate the LOCAL_INTERRUPT output.

Table 386: i_local_error_status_2_register

Bits	SW	Name	Description	Reset
0	R/WOCLR	MSI Mask Cleared Status [MSIMSKCLST]	This status bit indicates that one or more bits of MSI Mask of any function, PF or VF, was programmed or configured from 1 to 0 by local firmware or host software. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the user in debug_mux_control_2_reg. When this status bit is set, the PCIe Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Note that this is a Read Only Status bit. The MSI Mask Clear status per-function is captured in the msi_mask_cleared_status_register. Firmware has to clear the per-function bits in msi_mask_cleared_status_register to clear this status bit and to deassert LOCAL_INTERRUPT.	0x0
1	R/WOCLR	MSI Mask Set Status [MSIMSKSETST]	This status bit indicates that one or more bits of MSI Mask of any function, PF or VF, was programmed or configured from 0 to 1 by local firmware or host software. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Note that this is a Read Only Status bit. The MSI Mask Clear status per-function is captured in the msi_mask_set_status_register. Firmware has to clear the per-function bits in msi_mask_set_status_register to clear this status bit and to deassert LOCAL_INTERRUPT.	0x0
2	R/WOCLR	MSIX Function Mask Cleared Status [MSIXMSKCLST]	This status bit indicates that the MSIX Function Mask of any function, PF or VF, was programmed or configured from 1 to 0 by local firmware or host software. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the user in debug_mux_control_2_reg. When this status bit is set, the PCIe Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Note that this is a Read Only Status bit. The MSIX Function Mask Clear status per-function is captured in the msix_function_mask_cleared_status_register. Firmware has to clear the per-function bits in msix_function_mask_cleared_status_register to clear this status bit and to deassert LOCAL_INTERRUPT.	0x0
3	R/WOCLR	MSIX Function Mask Set Status [MSIXMSKSETST]	This status bit indicates that the MSIX Function Mask of any function, PF or VF, was programmed or configured from 0 to 1 by local firmware or host software. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Note that this is a Read Only Status bit. The MSIX Function Mask Clear status per-function is captured in the msix_function_mask_set_status_register. Firmware has to clear the per-function bits in msix_function_mask_set_status_register to clear this status bit and to deassert LOCAL_INTERRUPT.	0x0
4	R/WOCLR	Invalid SW Margining Command Received [ISWMCR]	This bit validates the 16-bit command stored in bits [15:0] and the Lane Number stored in bits [19:16] of the margining_error_status1_reg register. This bit is set upon receiving the first Error. Local firmware must clear this bit by writing a 1 to this bit before another error can be logged in the margining_error_status1_reg register.	0x0

Bits	SW	Name	Description	Reset
5	R/WOCLR	Invalid PHY Margining Command Received [IPHYMCR]	This bit validates the 8-bit command stored in bits [7:0] and the Lane Number stored in bits [11:8] of the margining_error_status1_reg register. This bit is set upon receiving the first Error. Local firmware must clear this bit by writing a 1 to this bit before another error can be logged in the margining_error_status1_reg register.	0x0
6	R/WOCLR	Write Ack Wait Timeout Error [WAWTE]	This bit indicates that the Controller detected a 10 ms timeout while waiting for Write Ack Lane Margining response from a PHY. The lane on which this timeout was detected is captured in bits 17:14 of the margining_error_status2_reg register. This bit is set upon receiving the first Error. Local firmware must clear this bit by writing a 1 to this bit before another error can be logged in the margining_error_status2_reg register.	0x0
7	R/WOCLR	Unexpected PHY Response Received [UPRR]	This bit indicates that the Controller received an unexpected PHY Response for Lane Margining. The lane on which this error was detected is captured in bits 21:18 of the margining_error_status2_reg register. Unexpected PHY Response is detected by Controller if PHY writes to the Margin Status or the Margin NAK bits of the MAC RX Margin Status 0 Register when no change in Start Margin or Margin Offset issued by Controller or after the Write Ack Wait Timeout. This bit is set upon receiving the first Error. Local firmware must clear this bit by writing a 1 to this bit before another error can be logged in the margining_error_status2_reg register.	0x0
8	R/WOCLR	NFTSTimeout Status [NFTSTOS]	This status bit indicates that a NFTS Timeout occured. This could occur if the PHY failed to achieve lock on the receive data before the NFTS Timeout during Rx_L0s.FTS state. Local firmware should consider increasing the advertized NFTS values if this event occurs.	0x0
9	R	Reserved [R9]	Reserved.	0x0
10	R	Reserved [R10]	Reserved.	0x0
11	R/WOCLR	Split Completion Table byte count RAM uncorrectable error [UNCESCBYTE]	This status bit indicates that the Controller detected an uncorrectable error in the Split Completion Table byte count RAM.	0x0
12	R/WOCLR	Split Completion Table Timer RAM uncorrectable error [UNCESCTIMER]	This status bit indicates that the Controller detected an uncorrectable error in the Split Completion Table Timer RAM.	0x0
13	R/WOCLR	Split Completion Table State RAM uncorrectable error [UNCESCSTATE]	This status bit indicates that the Controller detected an uncorrectable error in the Split Completion Table State RAM.	0x0
14	R/WOCLR	Link Equalization Request Interrupt [LEQRQIN]	**EP Mode:** Indicates that the Controller hardware detected a problem with equalization and automatically requested for equalization redo at the end of the equalization. Controller checks for problems in Recovery.Rcvr.Lock stateby comparing the Tx Coefficients agreed at end of Eq Phase2 with the Tx Coefficients received in TS1s in Recovery.Rcvr.Lock state at the end of equalization. Any mismatch is detected and the Request Equalization bit is set in Recovery.Rcvg.Cfg. This bit is set for 8GT/s, 16GT/s equalization requests. **1.** The Link Eq Request 8GT/s bit-5 in Link Status 2 Register will be set for 8GT/s Eq Request. **2.** The Link Eq Request 16.0 GT/s, bit-4 in 16.0 GT/s Status Register will be set for 16GT/s EqRequest. **RC Mode:** Indicates that the Controller received Equalization Request from downstream component. This bit is set for both 8GT/s and 16GT/s equalization requests. **1.** The Link Eq Request 8GT/s bit-5 in Link Status 2 Register will be set for 8GT/s Eq Request. **2.** The Link Eq Request 16.0 GT/s, bit-4 in 16.0 GT/s Status Register will be set for 16GT/s Eq Request.	0x0
15	R	Reserved [R15]	Reserved.	0x0

Bits	SW	Name	Description	Reset
16	R	LTSSM State Transition Interrupt Status [LSTINT]	Indicates that one or more LTSSM Transitions, that were programmed for firmware monitor/ control has occured. This is a Read-Only Status bit. To process the LTSSM State Transition Interrupt, the FW must go through the following steps: **1.** Read LTSSM Transition Debug Status Register (i_ltssm_transition_debug_stat_reg) to determine the LTSSM Transition event that occured. **2.** Process the LTSSM Transition event and clear by writing a 1 to (i_ltssm_transition_debug_stat_reg).	0x0
17	R	FC Timeout Error Status [FTE]	Assered when Flow control timer cross the limit value. FC Timeout Error causes link to retrain.	0x0
31:18	R	Reserved [R17]	Reserved.	0x0

Local Interrupt Mask 2 Register @0xd04

This is an extension of the Local Interrupt Mask Register. This register contains a mask bit for each interrupting condition in local_error_status_2_register. Setting the bit to 1 prevents the corresponding condition in the Local Error Status 2 Register from activating the LOCAL_INTERRUPT output.

Table 387: i_local_intrpt_mask_2_reg

Bits	SW	Name	Description	Reset
0	R/W	MSI Mask Cleared [MSIMSKCL]	Mask for MSI Mask Cleared Status.	0x0
1	R/W	MSI Mask Set [MSIMSKSET]	Mask for MSI Mask Set Status.	0x0
2	R/W	MSIX Function Mask Cleared [MSIXMSKCL]	Mask for MSIX Function Mask Set Status.	0x0
3	R/W	MSIX Function Mask Set [MSIXMSKSET]	Mask for MSIX Function Mask Cleared Status.	0x0
4	R/W	Invalid SW Margining Error Mask [ISWMEM]	When the Controller receives a Margining Command from SW in its configuration register, it checks if the command is valid. The error status is logged in local_error_status_2_register. This bit can be used to Mask asserting the LOCAL_INTERRUPT output when the Invalid SW Margining Error Status is set. • 1: Error is masked. • 0: Error is not masked.	0x0
5	R/W	Invalid PHY Margining Error Mask [IPHYMEM]	When the Controller receives a Margining Command from PHY over the PIPE Interface, it checks if the command is valid. The errorstatus is logged in local_error_status_2_register. This bit can be used to Mask asserting the LOCAL_INTERRUPT output when the Invalid PHY Margining Error Status is set. • 1: Error ismasked. • 0: Error is not masked.	0x0
6	R/W	Write Ack Wait Timeout Error Mask [WAWTEM]	When a WriteCommitted command is issued by the Controller, the PHY must respond with a Write_Ack within 10ms on the PIPE MessageBus Interface. However, if the Write_Ack is not received within 10ms, the Controller reports Timeout and stops waiting for the write_ack. This bit can be used to Mask asserting the LOCAL_INTERRUPT output upon this 10 ms timeout. • 1: Error is masked. • 0: Error is not masked.	0x0
7	R/W	Unexpected PHY Response Error Mask [UPREM]	Unexpected PHY Response is detected by Controller if PHY writes to the Margin Status or the Margin NAK bits of RX Margin Status 0 Register when no change in Start Margin or Margin Offset issued by Controller or after the Write Ack Wait Timeout. This bit can be used to Mask asserting the LOCAL_INTERRUPT output upon this error. • 1: Error is masked. • 0: Error is not masked.	0x0

Bits	SW	Name	Description	Reset
8	R/W	NFTSTimeout Mask [NFTSTOM]	Mask for NFTS Timeout.	0x0
9	R	Reserved [R9]	Reserved	0x0
10	R	Reserved [R10]	Reserved	0x0
11	R/W	Split Completion Table byte count RAM uncorrectable error mask register [UNCESCBYTE]	Split Completion Table byte count RAM uncorrectable error mask register.	0x0
12	R/W	Split Completion Table Timer RAM uncorrectable error mask register [UNCESCTIMER]	Split Completion Table Timer RAM uncorrectable error mask register.	0x0
13	R/W	Split Completion Table State RAM uncorrectable error mask register [UNCESCSTATE]	Split Completion Table State RAM uncorrectable error mask register.	0x0
14	R/W	Link Equalization Request Interrupt Mask [LEQRQINM]	Mask for Link Equalization Request Interrupt.	1'b1
15	R	Reserved [R15]	Reserved	0x0
16	R/W	LTSSM State Transition Interrupt Mask [LSTINTM]	Mask for LTSSM State Transition Interrupt.	1'b1
17	R/W	FC Timeout Error Mask [FCTEM]	Mask for FC Timeout Error.	1'b0
31:18	R	Reserved [R31]	Reserved	0x0

MSI Mask Cleared Status 1 Register @0xd10

This status register has one bit per function. Each function has a 32-bit MSI Mask. If any bit in the function's MSI Mask register is configured from 1 to 0, then the corresponding function's status bit in this register is set. Local Firmware needs to clear this register by writing a 1.

When each status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked inlocal_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 388: msi_mask_cleared_status_1

Bits	SW	Name	Description	Reset
0	R/WOCLR	PF0 MSI Mask Cleared Status [PF0MSIMSKCLST]	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF0 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
1	R/WOCLR	PF1 MSI Mask Cleared Status [PF1MSIMSKCLST]	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF1 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enablebit is set by the User in debug_mux_control_2_reg.	0x0
2	R/WOCLR	PF2 MSI Mask Cleared Status [PF2MSIMSKCLST]	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF2 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
3	R/WOCLR	PF3 MSI Mask Cleared Status [PF3MSIMSKCLST]	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF3 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enablebit is set by the User in debug_mux_control_2_reg.	0x0
4	R/WOCLR	VF0 MSI Mask Cleared Status [VF0MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF0 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0

Bits	SW	Name	Description	Reset
5	R/WOCLR	VF1 MSI Mask Cleared Status [VF1MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF1 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
6	R/WOCLR	VF2 MSI Mask Cleared Status [VF2MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF2 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
7	R/WOCLR	VF3 MSI Mask Cleared Status [VF3MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF3 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only whenthe MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
8	R/WOCLR	VF4 MSI Mask Cleared Status [VF4MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF4 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
9	R/WOCLR	VF5 MSI Mask Cleared Status [VF5MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF5 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
10	R/WOCLR	VF6 MSI Mask Cleared Status [VF6MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF6 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
11	R/WOCLR	VF7 MSI Mask Cleared Status [VF7MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF7 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
12	R/WOCLR	VF8 MSI Mask Cleared Status [VF8MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF8 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only whenthe MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
13	R/WOCLR	VF9 MSI Mask Cleared Status [VF9MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF9 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
14	R/WOCLR	VF10 MSI Mask Cleared Status [VF10MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF10 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
15	R/WOCLR	VF11 MSI Mask Cleared Status [VF11MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF11 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
16	R/WOCLR	VF12 MSI Mask Cleared Status [VF12MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF12 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
17	R/WOCLR	VF13 MSI Mask Cleared Status [VF13MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF13 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0

Bits	SW	Name	Description	Reset
18	R/WOCLR	VF14 MSI Mask Cleared Status [VF14MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF14 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
19	R/WOCLR	VF15 MSI Mask Cleared Status [VF15MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF15 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
20	R/WOCLR	VF16 MSI Mask Cleared Status [VF16MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF16 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
21	R/WOCLR	VF17 MSI Mask Cleared Status [VF17MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF17 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
22	R/WOCLR	VF18 MSI Mask Cleared Status [VF18MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF18 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
23	R/WOCLR	VF19 MSI Mask Cleared Status [VF19MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF19 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
24	R/WOCLR	VF20 MSI Mask Cleared Status [VF20MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF20 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
25	R/WOCLR	VF21 MSI Mask Cleared Status [VF21MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF21 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
26	R/WOCLR	VF22 MSI Mask Cleared Status [VF22MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF22 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
27	R/WOCLR	VF23 MSI Mask Cleared Status [VF23MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF23 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
28	R/WOCLR	VF24 MSI Mask Cleared Status [VF24MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF24 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
29	R/WOCLR	VF25 MSI Mask Cleared Status [VF25MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF25 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
30	R/WOCLR	VF26 MSI Mask Cleared Status [VF26MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF26 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0

Bits	SW	Name	Description	Reset
31	R/WOCLR	VF27 MSI Mask Cleared Status [VF27MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF27 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0

MSI Mask Set Status 1 Register @0xd14

This status register has one bit per function. Each function has a 32-bit MSI Mask. If any bit in the function's MSI Mask register is configured from 0 to 1, then the corresponding function's status bit in this register is set. Local Firmware needs to clear this register by writing a 1.

When each status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 389: msi_mask_set_status_1

Bits	SW	Name	Description	Reset
0	R/WOCLR	PF0 MSI Mask Set Status [PF0MSIMSKCLST]	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF0 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
1	R/WOCLR	PF1 MSI Mask Set Status [PF1MSIMSKCLST]	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF1 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
2	R/WOCLR	PF2 MSI Mask Set Status [PF2MSIMSKCLST]	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF2 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
3	R/WOCLR	PF3 MSI Mask Set Status [PF3MSIMSKCLST]	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF3 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
4	R/WOCLR	VF0 MSI Mask Set Status [VF0MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF0 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
5	R/WOCLR	VF1 MSI Mask Set Status [VF1MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF1 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
6	R/WOCLR	VF2 MSI Mask Set Status [VF2MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF2 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
7	R/WOCLR	VF3 MSI Mask Set Status [VF3MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF3 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0

Bits	SW	Name	Description	Reset
8	R/WOCLR	VF4 MSI Mask Set Status [VF4MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF4 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
9	R/WOCLR	VF5 MSI Mask Set Status [VF5MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF5 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only whenthe MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
10	R/WOCLR	VF6 MSI Mask Set Status [VF6MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF6 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
11	R/WOCLR	VF7 MSI Mask Set Status [VF7MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF7 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
12	R/WOCLR	VF8 MSI Mask Set Status [VF8MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF8 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
13	R/WOCLR	VF9 MSI Mask Set Status [VF9MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF9 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
14	R/WOCLR	VF10 MSI Mask Set Status [VF10MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF10 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only whenthe MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
15	R/WOCLR	VF11 MSI Mask Set Status [VF11MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF11 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enablebit is set by the User in debug_mux_control_2_reg.	0x0
16	R/WOCLR	VF12 MSIMask Set Status [VF12MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF12 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enablebit is set by the User in debug_mux_control_2_reg.	0x0
17	R/WOCLR	VF13 MSI Mask Set Status [VF13MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF13 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enablebit is set by the User in debug_mux_control_2_reg.	0x0
18	R/WOCLR	VF14 MSI Mask Set Status [VF14MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF14 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enablebit is set by the User in debug_mux_control_2_reg.	0x0
19	R/WOCLR	VF15 MSI Mask Set Status [VF15MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF15 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only whenthe MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
20	R/WOCLR	VF16 MSI Mask Set Status [VF16MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF16 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enablebit is set by the User in debug_mux_control_2_reg.	0x0

Bits	SW	Name	Description	Reset
21	R/WOCLR	VF17 MSI Mask Set Status [VF17MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF17 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enablebit is set by the User in debug_mux_control_2_reg.	0x0
22	R/WOCLR	VF18 MSI Mask Set Status [VF18MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF18 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enablebit is set by the User in debug_mux_control_2_reg.	0x0
23	R/WOCLR	VF19 MSI Mask Set Status [VF19MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF19 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enablebit is set by the User in debug_mux_control_2_reg.	0x0
24	R/WOCLR	VF20 MSI Mask Set Status [VF20MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF20 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only whenthe MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
25	R/WOCLR	VF21 MSI Mask Set Status [VF21MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF21 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enablebit is set by the User in debug_mux_control_2_reg.	0x0
26	R/WOCLR	VF22 MSI Mask Set Status [VF22MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF22 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enablebit is set by the User in debug_mux_control_2_reg.	0x0
27	R/WOCLR	VF23 MSI Mask Set Status [VF23MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF23 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enablebit is set by the User in debug_mux_control_2_reg.	0x0
28	R/WOCLR	VF24 MSI Mask Set Status [VF24MSIMSK]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF24 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enablebit is set by the User in debug_mux_control_2_reg.	0x0
29	R/WOCLR	VF25 MSI Mask Set Status [VF25MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF25 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only whenthe MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.	0x0
30	R/WOCLR	VF26 MSI Mask Set Status [VF26MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF26 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enablebit is set by the User in debug_mux_control_2_reg.	0x0
31	R/WOCLR	VF27 MSI Mask Set Status [VF27MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF27 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enablebit is set by the User in debug_mux_control_2_reg.	0x0

MSIX Function Mask Cleared Status 1 Register @0xd18

This status register has one bit per function. Each function has a 1-bit MSIX Function Mask. If the function's MSIX Function Mask register is configured from 1 to 0, then the corresponding

function's status bit in this register is set. Local Firmware needs to clear this register by writing a 1.

Each bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 390: msix_function_mask_cleared_status_1

Bits	SW	Name	Description	Reset
0	R/WOCLR	PF0 MSIX Function Mask Cleared Status [PF0MSIXMSKCLST]	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF0 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
1	R/WOCLR	PF1 MSIX Function Mask Cleared Status [PF1MSIXMSKCLST]	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF1 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
2	R/WOCLR	PF2 MSIX Function Mask Cleared Status [PF2MSIXMSKCLST]	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF2 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
3	R/WOCLR	PF3 MSIX Function Mask Cleared Status [PF3MSIXMSKCLST]	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF3 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
4	R/WOCLR	VF0 MSIX Function Mask Cleared Status [VF0MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF0 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
5	R/WOCLR	VF1 MSIX Function Mask Cleared Status [VF1MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF1 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
6	R/WOCLR	VF2 MSIX Function Mask Cleared Status [VF2MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF2 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
7	R/WOCLR	VF3 MSIX Function Mask Cleared Status [VF3MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF3 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
8	R/WOCLR	VF4 MSIX Function Mask Cleared Status [VF4MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF4 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
9	R/WOCLR	VF5 MSIX Function Mask Cleared Status [VF5MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF5 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
10	R/WOCLR	VF6 MSIX Function Mask Cleared Status [VF6MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF6 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
11	R/WOCLR	VF7 MSIX Function Mask Cleared Status [VF7MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF7 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
12	R/WOCLR	VF8 MSIX Function Mask Cleared Status [VF8MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF8 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
13	R/WOCLR	VF9 MSIX Function Mask Cleared Status [VF9MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF9 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
14	R/WOCLR	VF10 MSIX Function Mask Cleared Status [VF10MSIXMS]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF10 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
15	R/WOCLR	VF11 MSIX Function Mask Cleared Status [VF11MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF11 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
16	R/WOCLR	VF12 MSIX Function Mask Cleared Status [VF12MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF12 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0

Bits	SW	Name	Description	Reset
17	R/WOCLR	VF13 MSIX Function Mask Cleared Status [VF13MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF13 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
18	R/WOCLR	VF14 MSIX Function Mask Cleared Status [VF14MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF14 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
19	R/WOCLR	VF15 MSIX Function Mask Cleared Status [VF15MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF15 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
20	R/WOCLR	VF16 MSIX Function Mask Cleared Status [VF16MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF16 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
21	R/WOCLR	VF17 MSIX Function Mask Cleared Status [VF17MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF17 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
22	R/WOCLR	VF18 MSIX Function Mask Cleared Status [VF18MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF18 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
23	R/WOCLR	VF19 MSIX Function Mask Cleared Status [VF19MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF19 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW. debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.	0x0
24	R/WOCLR	VF20 MSIX Function Mask Cleared Status [VF20MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF20 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
25	R/WOCLR	VF21 MSIX Function Mask Cleared Status [VF21MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF21 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
26	R/WOCLR	VF22 MSIX Function Mask Cleared Status [VF22MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF22 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
27	R/WOCLR	VF23 MSIX Function Mask Cleared Status [VF23MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF23 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
28	R/WOCLR	VF24 MSIX Function Mask Cleared Status [VF24MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF24 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
29	R/WOCLR	VF25 MSIX Function Mask Cleared Status [VF25MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF25 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
30	R/WOCLR	VF26 MSIX Function Mask Cleared Status [VF26MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF26 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0
31	R/WOCLR	VF27 MSIX Function Mask Cleared Status [VF27MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF27 MSIX Function Mask is programmed or configured from 1 to 0 by local Firmware Or Host SW.	0x0

MSIX Function Mask Set Status 1 Register @0xd1c

This status register has one bit per function. Each function has a 1-bit MSIX Function Mask. If the function's MSIX Function Mask register is configured from 0 to 1, then the corresponding function's status bit in this register is set. Local Firmware needs to clear this register by writing a 1.

Each bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When the status bit is set, the Controller asserts

LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 391: msix_function_mask_set_status_1

Bits	SW	Name	Description	Reset
0	R/WOCLR	PF0 MSIX Function Mask Set Status [PF0MSIXMSKCLST]	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF0 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
1	R/WOCLR	PF1 MSIX Function Mask Set Status [PF1MSIXMSKCLST]	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF1 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
2	R/WOCLR	PF2 MSIX Function Mask Set Status [PF2MSIXMSKCLST]	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF2 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
3	R/WOCLR	PF3 MSIX Function Mask Set Status [PF3MSIXMSKCLST]	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF3 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
4	R/WOCLR	VF0 MSIX Function Mask Set Status [VF0MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF0 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
5	R/WOCLR	VF1 MSIX Function Mask Set Status [VF1MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF1 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
6	R/WOCLR	VF2 MSIX Function Mask Set Status [VF2MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF2 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
7	R/WOCLR	VF3 MSIX Function Mask Set Status [VF3MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF3 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
8	R/WOCLR	VF4 MSIX Function Mask Set Status [VF4MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF4 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
9	R/WOCLR	VF5 MSIX Function Mask Set Status [VF5MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF5 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
10	R/WOCLR	VF6 MSIX Function Mask Set Status [VF6MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF6 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
11	R/WOCLR	VF7 MSIX Function Mask Set Status [VF7MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF7 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
12	R/WOCLR	VF8 MSIX Function Mask Set Status [VF8MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF8 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
13	R/WOCLR	VF9 MSIX Function Mask Set Status [VF9MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF9 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
14	R/WOCLR	VF10 MSIX Function Mask Set Status [VF10MSIXMSCLSTKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF10 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
15	R/WOCLR	VF11 MSIX Function Mask Set Status [VF11MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF11 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
16	R/WOCLR	VF12 MSIX Function Mask Set Status [VF12MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF12 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
17	R/WOCLR	VF13 MSIX Function Mask Set Status [VF13MSIXMS]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF13 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0

Bits	SW	Name	Description	Reset
18	R/WOCLR	VF14 MSIX Function Mask Set Status [VF14MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF14 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
19	R/WOCLR	VF15 MSIX Function Mask Set Status [VF15MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF15 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
20	R/WOCLR	VF16 MSIX Function Mask Set Status [VF16MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF16 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
21	R/WOCLR	VF17 MSIX Function Mask Set Status [VF17MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF17 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
22	R/WOCLR	VF18 MSIX Function Mask Set Status [VF18MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF18 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
23	R/WOCLR	VF19 MSIX Function Mask Set Status [VF19MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF19 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
24	R/WOCLR	VF20 MSIX Function Mask Set Status [VF20MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF20 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
25	R/WOCLR	VF21 MSIX Function Mask Set Status [VF21MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF21 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
26	R/WOCLR	VF22 MSIX Function Mask Set Status [VF22MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF22 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
27	R/WOCLR	VF23 MSIX Function Mask Set Status [VF23MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF23 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
28	R/WOCLR	VF24 MSIX Function Mask Set Status [VF24MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF24 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
29	R/WOCLR	VF25 MSIX Function Mask Set Status [VF25MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF25 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
30	R/WOCLR	VF26 MSIX Function Mask Set Status [VF26MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF26 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0
31	R/WOCLR	VF27 MSIX Function Mask Set Status [VF27MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF27 MSIX Function Mask is programmed or configured from 0 to 1 by local Firmware Or Host SW.	0x0

MSI Mask Cleared Status 2 Register @0xd20

This status register has one bit per function. Each function has a 32-bit MSI Mask. If any bit in the function's MSI Mask register is configured from 1 to 0, then the corresponding function's status bit in this register is set. Local Firmware needs to clear this register by writing a 1.

Each VF has a 32-bit MSI Mask. Each bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When the status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked inlocal_intrpt_mask_2_reg. Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 392: msi_mask_cleared_status_2

Bits	SW	Name	Description	Reset
0	R/WOCLR	VF28 MSI Mask Cleared Status [VF28MSIMSKCLST]	This status bit is set when any of the 32-bits in VF28 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
1	R/WOCLR	VF29 MSI Mask Cleared Status [VF29MSIMSKCLST]	This status bit is set when any of the 32-bits in VF29 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
2	R/WOCLR	VF30 MSI Mask Cleared Status [VF30MSIMSKCLST]	This status bit is set when any of the 32-bits in VF30 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
3	R/WOCLR	VF31 MSI Mask Cleared Status [VF31MSIMSKCLST]	This status bit is set when any of the 32-bits in VF31 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
4	R/WOCLR	VF32 MSI Mask Cleared Status [VF32MSIMSKCLST]	This status bit is set when any of the 32-bits in VF32 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
5	R/WOCLR	VF33 MSIMask Cleared Status [VF33MSIMSK]	This status bit is set when any of the 32-bits in VF33 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
6	R/WOCLR	VF34 MSI Mask Cleared Status [VF34MSIMSKCLST]	This status bit is set when any of the 32-bits in VF34 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
7	R/WOCLR	VF35 MSI Mask Cleared Status [VF35MSIMSKCLST]	This status bit is set when any of the 32-bits in VF35 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
8	R/WOCLR	VF36 MSI Mask Cleared Status [VF36MSIMSKCLST]	This status bit is set when any of the 32-bits in VF36 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
9	R/WOCLR	VF37 MSI Mask Cleared Status [VF37MSIMSKCLST]	This status bit is set when any of the 32-bits in VF37 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
10	R/WOCLR	VF38 MSI Mask Cleared Status [VF38MSIMSKCLST]	This status bit is set when any of the 32-bits in VF38 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
11	R/WOCLR	VF39 MSI Mask Cleared Status [VF39MSIMSKCLST]	This status bit is set when any of the 32-bits in VF39 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
12	R/WOCLR	VF40 MSI Mask Cleared Status [VF40MSIMSKCLST]	This status bit is set when any of the 32-bits in VF40 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
13	R/WOCLR	VF41 MSI Mask Cleared Status [VF41MSIMSKCLST]	This status bit is set when any of the 32-bits in VF41 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
14	R/WOCLR	VF42 MSI Mask Cleared Status [VF42MSIMSKCLST]	This status bit is set when any of the 32-bits in VF42 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
15	R/WOCLR	VF43 MSI Mask Cleared Status [VF43MSIMSKCLST]	This status bit is set when any of the 32-bits in VF43 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
16	R/WOCLR	VF44 MSI Mask Cleared Status [VF44MSIMSKCLST]	This status bit is set when any of the 32-bits in VF44 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
17	R/WOCLR	VF45 MSI Mask Cleared Status [VF45MSIMSKCLST]	This status bit is set when any of the 32-bits in VF45 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
18	R/WOCLR	VF46 MSI Mask Cleared Status [VF46MSIMSKCLST]	This status bit is set when any of the 32-bits in VF46 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0

Bits	SW	Name	Description	Reset
19	R/WOCLR	VF47 MSI Mask Cleared Status [VF47MSIMSKCLST]	This status bit is set when any of the 32-bits in VF47 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
20	R/WOCLR	VF48 MSI Mask Cleared Status [VF48MSIMSKCLST]	This status bit is set when any of the 32-bits in VF48 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
21	R/WOCLR	VF49 MSI Mask Cleared Status [VF49MSIMSKCLST]	This status bit is set when any of the 32-bits in VF49 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
22	R/WOCLR	VF50 MSI Mask Cleared Status [VF50MSIMSKCLST]	This status bit is set when any of the 32-bits in VF50 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
23	R/WOCLR	VF51 MSI Mask Cleared Status [VF51MSIMSKCLST]	This status bit is set when any of the 32-bits in VF51 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
24	R/WOCLR	VF52 MSI Mask Cleared Status [VF52MSIMSKCLST]	This status bit is set when any of the 32-bits in VF52 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
25	R/WOCLR	VF53 MSI Mask Cleared Status [VF53MSIMSKCLST]	This status bit is set when any of the 32-bits in VF53 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
26	R/WOCLR	VF54 MSI Mask Cleared Status [VF54MSIMSKCLST]	This status bit is set when any of the 32-bits in VF54 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
27	R/WOCLR	VF55 MSI Mask Cleared Status [VF55MSIMSKCLST]	This status bit is set when any of the 32-bits in VF55 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
28	R/WOCLR	VF56 MSI Mask Cleared Status [VF56MSIMSKCLST]	This status bit is set when any of the 32-bits in VF56 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
29	R/WOCLR	VF57 MSI Mask Cleared Status [VF57MSIMSKCLST]	This status bit is set when any of the 32-bits in VF57 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
30	R/WOCLR	VF58 MSI Mask Cleared Status [VF58MSIMSKCLST]	This status bit is set when any of the 32-bits in VF58 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0
31	R/WOCLR	VF59 MSI Mask Cleared Status [VF59MSIMSKCLST]	This status bit is set when any of the 32-bits in VF59 MSI Mask is programmed or configured from 1 to 0 by Local Firmware or Host SW.	0x0

MSI Mask Set Status 2 Register @0xd24

This status register has one bit per function. Each function has a 32-bit MSI Mask. If any bit in the function's MSI Mask register is configured from 0 to 1, then the corresponding function's status bit in this register is set. Local Firmware needs to clear this register by writing a 1.

Each bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked inlocal_intrpt_mask_2_reg. Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 393: msi_mask_set_status_2

Bits	SW	Name	Description	Reset
0	R/WOCLR	VF28 MSI Mask Set Status [VF28MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF28 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0

Bits	SW	Name	Description	Reset
1	R/WOCLR	VF29 MSI Mask Set Status [VF29MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF29 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
2	R/WOCLR	VF30 MSI Mask Set Status [VF30MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF30 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
3	R/WOCLR	VF31 MSI Mask Set Status [VF31MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF31 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
4	R/WOCLR	VF32 MSI Mask Set Status [VF32MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF32 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
5	R/WOCLR	VF33 MSI Mask Set Status [VF33MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF33 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
6	R/WOCLR	VF34 MSI Mask Set Status [VF34MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF34 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
7	R/WOCLR	VF35 MSI Mask Set Status [VF35MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF35 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
8	R/WOCLR	VF36 MSI Mask Set Status [VF36MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF36 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
9	R/WOCLR	VF37 MSI Mask Set Status [VF37MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF37 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
10	R/WOCLR	VF38 MSI Mask Set Status [VF38MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF38 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
11	R/WOCLR	VF39 MSI Mask Set Status [VF39MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF39 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
12	R/WOCLR	VF40 MSI Mask Set Status [VF40MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF40 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
13	R/WOCLR	VF41 MSI Mask Set Status [VF41MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF41 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
14	R/WOCLR	VF42 MSI Mask Set Status [VF42MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF42 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
15	R/WOCLR	VF43 MSI Mask Set Status [VF43MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF43 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
16	R/WOCLR	VF44 MSI Mask Set Status [VF44MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF44 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
17	R/WOCLR	VF45 MSI Mask Set Status [VF45MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF45 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
18	R/WOCLR	VF46 MSI Mask Set Status [VF46MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF46 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
19	R/WOCLR	VF47 MSI Mask Set Status [VF47MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF47 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
20	R/WOCLR	VF48 MSI Mask Set Status [VF48MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF48 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0

Bits	SW	Name	Description	Reset
21	R/WOCLR	VF49 MSI Mask Set Status [VF49MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF49 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
22	R/WOCLR	VF50 MSI Mask Set Status [VF50MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF50 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
23	R/WOCLR	VF51 MSI Mask Set Status [VF51MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF51 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
24	R/WOCLR	VF52 MSI Mask Set Status [VF52MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF52 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
25	R/WOCLR	VF53 MSI Mask Set Status [VF53MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF53 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
26	R/WOCLR	VF54 MSI Mask Set Status [VF54MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF54 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
27	R/WOCLR	VF55 MSI Mask Set Status [VF55MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF55 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
28	R/WOCLR	VF56 MSI Mask Set Status [VF56MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF56 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
29	R/WOCLR	VF57 MSI Mask Set Status [VF57MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF57 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
30	R/WOCLR	VF58 MSI Mask Set Status [VF58MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF58 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
31	R/WOCLR	VF59 MSI Mask Set Status [VF59MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF59 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0

MSIX Function Mask Cleared Status 2 Register @0xd28

This status register has one bit per function. Each function has a 1-bit MSIX Function Mask. If the function's MSIX Function Mask register is configured from 1 to 0, then the corresponding function's status bit in this register is set. Local Firmware needs to clear this register by writing a 1.

Each VF has a 1-bit MSIX Function Mask. Each bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 394: msix_function_mask_cleared_status_2

Bits	SW	Name	Description	Reset
0	R/WOCLR	VF28 MSIX Function Mask Cleared Status [VF28MSIXMSKCLST]	This status bit is set when the VF28 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
1	R/WOCLR	VF29 MSIX Function Mask Cleared Status[VF29MSIXMSKCLST]	This status bit is set when the VF29 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0

Bits	SW	Name	Description	Reset
2	R/WOCLR	VF30 MSIX Function Mask Cleared Status [VF30MSIXMSKCLST]	This status bit is set when the VF30 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
3	R/WOCLR	VF31 MSIX Function Mask Cleared Status [VF31MSIXMSKCLST]	This status bit is set when the VF31 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
4	R/WOCLR	VF32 MSIX Function Mask Cleared Status [VF32MSIXMSKCLST]	This status bit is set when the VF32 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
5	R/WOCLR	VF33 MSIX Function Mask Cleared Status [VF33MSIXMSKCLST]	This status bit is set when the VF33 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
6	R/WOCLR	VF34 MSIX Function Mask Cleared Status [VF34MSIXMSKCLST]	This status bit is set when the VF34 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
7	R/WOCLR	VF35 MSIX Function Mask Cleared Status [VF35MSIXMSKCLST]	This status bit is set when the VF35 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
8	R/WOCLR	VF36 MSIX Function Mask Cleared Status [VF36MSIXMSKCLST]	This status bit is set when the VF36 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
9	R/WOCLR	VF37 MSIX Function Mask Cleared Status [VF37MSIXMSKCLST]	This status bit is set when the VF37 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
10	R/WOCLR	VF38 MSIX Function Mask Cleared Status [VF38MSIXMSKCLST]	This status bit is set when the VF38 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
11	R/WOCLR	VF39 MSIX Function Mask Cleared Status [VF39MSIXMSKCLST]	This status bit is set when the VF39 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
12	R/WOCLR	VF40 MSIX Function Mask Cleared Status [VF40MSIXMSKCLST]	This status bit is set when the VF40 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
13	R/WOCLR	VF41 MSIXFunction Mask Cleared Status [VF41MSIXMS]	This status bit is set when the VF41 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
14	R/WOCLR	VF42 MSIX Function Mask Cleared Status [VF42MSIXMSKCLST]	This status bit is set when the VF42 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
15	R/WOCLR	VF43 MSIX Function Mask Cleared Status [VF43MSIXMSKCLST]	This status bit is set when the VF43 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
16	R/WOCLR	VF44 MSIX Function Mask Cleared Status [VF44MSIXMSKCLST]	This status bit is set when the VF44 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
17	R/WOCLR	VF45 MSIX Function Mask Cleared Status [VF45MSIXMSKCLST]	This status bit is set when the VF45 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
18	R/WOCLR	VF46 MSIX Function Mask Cleared Status [VF46MSIXMSKCLST]	This status bit is set when the VF46 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
19	R/WOCLR	VF47 MSIX Function Mask Cleared Status [VF47MSIXMSKCLST]	This status bit is set when the VF47 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
20	R/WOCLR	VF48 MSIX Function Mask Cleared Status [VF48MSIXMSKCLST]	This status bit is set when the VF48 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
21	R/WOCLR	VF49 MSIX Function Mask Cleared Status [VF49MSIXMSKCLST]	This status bit is set when the VF49 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0

Bits	SW	Name	Description	Reset
22	R/WOCLR	VF50 MSIX Function Mask Cleared Status [VF50MSIXMSKCLST]	This status bit is set when the VF50 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
23	R/WOCLR	VF51 MSIX Function Mask Cleared Status [VF51MSIXMSKCLST]	This status bit is set when the VF51 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
24	R/WOCLR	VF52 MSIX Function Mask Cleared Status [VF52MSIXMSKCLST]	This status bit is set when the VF52 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
25	R/WOCLR	VF53 MSIX Function Mask Cleared Status [VF53MSIXMSKCLST]	This status bit is set when the VF53 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
26	R/WOCLR	VF54 MSIX Function Mask Cleared Status [VF54MSIXMSKCLST]	This status bit is set when the VF54 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
27	R/WOCLR	VF55 MSIX Function Mask Cleared Status [VF55MSIXMSKCLST]	This status bit is set when the VF55 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
28	R/WOCLR	VF56 MSIX Function Mask Cleared Status [VF56MSIXMSKCLST]	This status bit is set when the VF56 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
29	R/WOCLR	VF57 MSIX Function Mask Cleared Status [VF57MSIXMSKCLST]	This status bit is set when the VF57 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
30	R/WOCLR	VF58 MSIX Function Mask Cleared Status [VF58MSIXMSKCLST]	This status bit is set when the VF58 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
31	R/WOCLR	VF59 MSIX Function Mask Cleared Status [VF59MSIXMSKCLST]	This status bit is set when the VF59 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0

MSIX Function Mask Set Status 2 Register @0xd2c

This status register has one bit per function. Each function has a 1-bit MSIX Function Mask. If the function's MSIX Function Mask register is configured from 0 to 1, then the corresponding function's status bit in this register is set. Local Firmware needs to clear this register by writing a 1.

Each bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 395: msix_function_mask_set_status_2

Bits	SW	Name	Description	Reset
0	R/WOCLR	VF28 MSIX Function Mask Set Status [VF28MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF28 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
1	R/WOCLR	VF29 MSIX Function Mask Set Status [VF29MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF29 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
2	R/WOCLR	VF30 MSIX Function Mask Set Status [VF30MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF30 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
3	R/WOCLR	VF31 MSIX Function Mask Set Status [VF31MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF31 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0

Bits	SW	Name	Description	Reset
4	R/WOCLR	VF32 MSIX Function Mask Set Status [VF32MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF32 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
5	R/WOCLR	VF33 MSIX Function Mask Set Status [VF33MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF33 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
6	R/WOCLR	VF34 MSIX Function Mask Set Status [VF34MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF34 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
7	R/WOCLR	VF35 MSIX Function Mask Set Status [VF35MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF35 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
8	R/WOCLR	VF36 MSIX Function Mask Set Status [VF36MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF36 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
9	R/WOCLR	VF37 MSIX Function Mask Set Status [VF37MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF37 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
10	R/WOCLR	VF38 MSIX Function Mask Set Status [VF38MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF38 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
11	R/WOCLR	VF39 MSIX Function Mask Set Status [VF39MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF39 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
12	R/WOCLR	VF40 MSIX Function Mask Set Status [VF40MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF40 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
13	R/WOCLR	VF41 MSIX Function Mask Set Status [VF41MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF41 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
14	R/WOCLR	VF42 MSIX Function Mask Set Status [VF42MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF42 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
15	R/WOCLR	VF43 MSIX Function Mask Set Status [VF43MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF43 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
16	R/WOCLR	VF44 MSIX Function Mask Set Status [VF44MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF44 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
17	R/WOCLR	VF45 MSIX Function Mask Set Status [VF45MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF45 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
18	R/WOCLR	VF46 MSIX Function Mask Set Status [VF46MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF46 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
19	R/WOCLR	VF47 MSIX Function Mask Set Status [VF47MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF47 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
20	R/WOCLR	VF48 MSIX Function Mask Set Status [VF48MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF48 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
21	R/WOCLR	VF49 MSIX Function Mask Set Status [VF49MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF49 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
22	R/WOCLR	VF50 MSIX Function Mask Set Status [VF50MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF50 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
23	R/WOCLR	VF51 MSIXFunction Mask Set Status [VF51MSIXMS]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF51 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0

Bits	SW	Name	Description	Reset
24	R/WOCLR	VF52 MSIX Function Mask Set Status [VF52MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF52 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
25	R/WOCLR	VF53 MSIX Function Mask Set Status [VF53MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF53 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
26	R/WOCLR	VF54 MSIX Function Mask Set Status [VF54MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF54 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
27	R/WOCLR	VF55 MSIX Function Mask Set Status [VF55MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF55 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
28	R/WOCLR	VF56 MSIX Function Mask Set Status [VF56MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF56 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
29	R/WOCLR	VF57 MSIX Function Mask Set Status [VF57MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF57 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
30	R/WOCLR	VF58 MSIX Function Mask Set Status [VF58MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF58 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
31	R/WOCLR	VF59 MSIX Function Mask Set Status [VF59MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF59 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0

MSI Mask Cleared Status 3 Register @0xd30

This status register has one bit per function. Each function has a 32-bit MSI Mask. If any bit in the function's MSI Mask register is configured from 1 to 0, then the corresponding function's status bit in this register is set. Local Firmware needs to clear this register by writing a 1.

Each bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked inlocal_intrpt_mask_2_reg. Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 396: msi_mask_cleared_status_3

Bits	SW	Name	Description	Reset
0	R/WOCLR	VF60 MSI Mask Cleared Status [VF60MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF60 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
1	R/WOCLR	VF61 MSI Mask Cleared Status [VF61MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF61 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
2	R/WOCLR	VF62 MSI Mask Cleared Status [VF62MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF62 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
3	R/WOCLR	VF63 MSI Mask Cleared Status [VF63MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF63 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
31:4	R	Reserved [R31]	Reserved	0x0

MSI Mask Set Status 3 Register @0xd34

This status register has one bit per function. Each function has a 32-bit MSI Mask. If any bit in the function's MSI Mask register is configured from 0 to 1, then the corresponding function's status bit in this register is set. Local Firmware needs to clear this register by writing a 1.

Each bit is set only when the MSI Mask Change Enhanced Interrupt Enablebit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked inlocal_intrpt_mask_2_reg. Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 397: msi_mask_set_status_3

Bits	SW	Name	Description	Reset
0	R/WOCLR	VF60 MSI Mask Set Status [VF60MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF60 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
1	R/WOCLR	VF61 MSI Mask Set Status [VF61MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF61 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
2	R/WOCLR	VF62 MSI Mask Set Status [VF62MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF62 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
3	R/WOCLR	VF63 MSI Mask Set Status [VF63MSIMSKCLST]	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF63 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
31:4	R	Reserved [R31]	Reserved	0x0

MSIX Function Mask Cleared Status 3 Register @0xd38

This status register has one bit per function. Each function has a 1-bit MSIX Function Mask. If the function's MSIX Function Mask register is configured from 1 to 0, then the corresponding function's status bit in this register is set. Local Firmware needs to clear this register by writing a 1.

Each bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 398: msix_function_mask_cleared_status_3

Bits	SW	Name	Description	Reset
0	R/WOCLR	VF60 MSIX Function Mask Cleared Status [VF60MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF60 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
1	R/WOCLR	VF61 MSIX Function Mask Cleared Status [VF61MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF61 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
2	R/WOCLR	VF62 MSIX Function Mask Cleared Status [VF62MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF62 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
3	R/WOCLR	VF63 MSIX Function Mask Cleared Status [VF63MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF63 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.	0x0
31:4	R	Reserved [R31]	Reserved	0x0

MSIX Function Mask Set Status 3 Register @0xd3c

This status register has one bit per function. Each function has a 1-bit MSIX Function Mask. If the function's MSIX Function Mask register is configured from 0 to 1, then the corresponding function's status bit in this register is set. Local Firmware needs to clear this register by writing a 1.

Each bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 399: msix_function_mask_set_status_3

Bits	SW	Name	Description	Reset
0	R/WOCLR	VF60 MSIX Function Mask Set Status [VF60MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF60 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
1	R/WOCLR	VF61 MSIX Function Mask Set Status [VF61MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF61 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
2	R/WOCLR	VF62 MSIX Function Mask Set Status [VF62MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF62 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
3	R/WOCLR	VF63 MSIX Function Mask Set Status [VF63MSIXMSKCLST]	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF63 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.	0x0
31:4	R	Reserved [R31]	Reserved	0x0

Link Down Indication Control Register @0xda0

This register is for the control of Link Down Indication Auto Reset behavior.

Table 400: i_ld_ctrl

Bits	SW	Name	Description	Reset
23:0	R/W	Link Down Indication Auto Reset Timer Control Value [LDTIMER]	This is a counter timeout value which triggers the internal logic to reset the link down indication bit in the AXI Configuration registers.	0x5F5E10
24	R/W	Link Down indication bit auto reset enable [AUTO_EN]	This bit when set indicates that the link down indication auto reset is enabled.	0x1
31:25	R	Reserved [R7]	Reserved	0x0

PIPE RX Electrical Idle Glitch Control Register @0xda4

This register controls the behavior of glitch filter on the pipe rx Electrical Idle signal from the PHY/PCS. Adjustment of this register is not required for normal operations.

Table 401: rx_elec_idle_filter_control

Bits	SW	Name	Description	Reset
3:0	R/W	RX Electrical Idle Glitch Filter Disable [GFLD]	By default controller enables glitch filter on all lanes. Setting this bit to one makes the controller to disable the glitch filter on that corresponding lanes in which the bit is set. When all bits are set to one the Glitch filter is completely bypassed. When any bit is zero glitch filter is enabled, and de-glitching is done only on the lanes that are set to zero.	0x0
15:4	R	Reserved [RSVGFLD]	Reserved	0x0
23:16	R/W	RX Electrical Idle Glitch Filter Count CORE Clocks [GFLCC]	This controls the glitch filter on CORE Clock domain. This counter indicates the number of CORE Clocks the glitch will be filtered out. The total delay of the glitch filter is calculated as (CORE Clock Period * Number of CORE Clocks) this delay should be same or close enough for both CORE Clock (GFLCC) and PM Clock (GFLCP).	0x20
31:24	R/W	RX Electrical Idle Glitch Filter Count PM Clocks [GFLCP]	This controls the glitch filter on PM Clock domain. This counter indicates the number of PM Clocks the glitch will be filtered out. The total delay of the glitch filter is calculated as (PM Clock Period * Number of PM Clocks) this delay should be same or close enough for both Core Clock (GFLCC) and PM Clock (GFLCP).	0x04

Equalization Debug Monitor Control Register @0xe4c

The register bits to Control EQ debug Monitor operation are implemented in this Register.

Table 402: i_eq_debug_mon_control_reg

Bits	SW	Name	Description	Reset
0	R/W	Clear All capture [CLRCAPT]	Setting this bit clears all captured information in the EQ Debug Status Registers. If it is unset then capture is allowed in status registers.	0x0
4:1	R/W	Capture Lane Select [CAPTLNSEL]	Selects the Lane whose Equalization Debug information is to be captured. Please note, this signifies the physical lane number.	0x0
6:5	R/W	Capture EQ Phase Select [CAPTPHSEL]	Selects the Equalization Phase when capture is to be done. • 01 : Phase 2, • 10 : Phase 3, • 11 : Phase 0, 1, 2, and 3.	0x3
9:7	R/W	Capture EQ Speed Select [CAPTSPDSEL]	Selects the Link Speed at which capture is to be done. • 000 : Any speed, • 001 : Gen 3, • 010 : Gen 4, • 100 : Gen 5.	0x0
10	R	Eq Debug Capture Behavior [CAPTBEH]	If this is set , the first 64 equalization info events are captured else the last 64 events are captured	0x1
31:11	R	Reserved [R1]	Reserved	0x0

Equalization Debug Monitor Status 0 Register @0xe50

Both the Local and Remote EQ FS and LF values are captured in this Register.

Table 403: i_eq_debug_mon_status0_reg

Bits	SW	Name	Description	Reset
5:0	R	Local FS [LCLFS]	Local PHY's FS Value Of the Lane and Speed Selected.	0x0
11:6	R	Local LF [LCLLF]	Local PHY's LF Value Of the Lane and Speed Selected.	0x0
17:12	R	Remote FS [REMFS]	Remote PHY's FS Value Of the Lane and Speed Selected.	0x0
23:18	R	Remote LF [REMLF]	Remote PHY's LF Value Of the Lane and Speed Selected.	0x0
31:24	R	Reserved [R1]	Reserved	0x0

Equalization Debug Monitor Status Register @0xe54

All the Dynamic Equalization information is captured in this Register.This is implemented using a synchronous FIFO, which stores all the captured events as sepereate 32 bit entries. Every read increments the read pointer and the client must store the data read. The FIFO can be cleared using the 'Clear all Capture bit in the EQ Debug Monitor Control Register.

Table 404: i_eq_debug_mon_status_reg

Bits	SW	Name	Description	Reset
17:0	R	Coefficients [EQCOEFF]	• Phase0: Stores Initial Local TX Coefficients mapped from Initial Preset. • Phase1: Stores Initial Remote Coefficients advertised in Phase1. (Cp, LF, FS), EP Ph2/RC. • Phase2: Stores Coefficients Received from Remote Device. • Phase3: Stores CurrentCoefficients of the Remote Device. EP Ph3/RC.	0x0
21:18	R	Preset [EQPRE]	• Phase0: Stores Initial Local TX Preset received in Phase0. • Phase1: Stores Initial Remote Preset advertised in Phase1. EP Ph2/RC. • Phase2: Stores Preset Received from Remote Device. • Phase3: Stores Current Preset of the Remote Device. EP Ph3/RC.	0x0
22	R	Preset Valid [EQPREVD]	1: Preset Valid, Indicates [21:18] is valid. • Phase0: Set to '1' to indicate that the intial Local Preset is Valid. • Phase1: Set to '1' to indicate that the advertised Remote Preset is Valid. EP Ph2/RC. • Phase2: Reflects the use preset bit received from the remote end. • Phase3: Set to 1 if controller provide preset feedback and to 0 for coefficient feedback. EP Ph3/RC.	0x0
23	R	Coefficient Reject [COEFFREJ]	• Phase0: Set to '1' if an unsupported preset is received in Phase0. • Phase1: Set to '0' since no reject in phase1. EP Ph2/RC. • Phase2: Indicates that Controller Rejected the received settings to Remote Device in the TX TS1/TS2. This Reject indicates the current Coefficients or Preset received from Remote Device are rejected. • Phase3: Indicates Reject by the Remote end device. This bit indicates that the current Coefficient or Preset was rejected by the remote end device. EP Ph3/RC.	0x0

Bits	SW	Name	Description	Reset
29:24	R	Direction Feedback [DIRFED]	EP Ph2/RC Ph3: Stores Direction Change Feedback or Preset feedback Transmitted to Remote Device. Bit-22, EQPREVD, indicates if this is a Preset feedback or Direction Change Feedback. EP Ph3/RC Ph2: Reserved	0x0
31:30	R	Equalization Phase [EQPHASE]	Equalization Phase during Capture • 00 : Phase 0, • 01 : Phase 1, • 10 : Phase 2, • 11 : Phase 3.	0x0

AXI Feature Control Register @0xe5c

This register is for the control of AXI Features.

Table 405: i_axi_feature_reg

Bits	SW	Name	Description	Reset
0	R	Reserved [R0]	Reserved	0x0
1	R/W	Block SLVERR Response to AXI forconfiguration requests [SLVERRCTRL]	This bit if set to 1, AXI Slave masks the SLVERR response to be given in case of UR or CRS completion for configuration requests. If this bit is set to 0, UR and CRS completions from the link causes SLVERR at AXI.	0x1
7:2	R	Reserved [R7]	Reserved	0x0
16:8	R	Reserved [R16]	Reserved	0x0
30:17	R	Reserved [R30]	Reserved	0x0
31	R	Reserved [R31]	Reserved	0x0

Link Equalization Control 2 Register @0xe60

This register implements fields to control and override Link Equalization.

Table 406: i_link_eq_control_2_reg

Bits	SW	Name	Description	Reset
0	R/W	Gen3 EQ Phase2 Remote Tx Preset Enable [G3PRRMEN]	Used only in EP Mode. This bit enables the Controller, to feedback a Tx Preset for the Remote end Transmitter in the first iteration of Link Equalization Phase2 at Gen3 speed. The Gen3 Tx Preset that is used for feedback is programmable in bits [4:1] of this register. Reserved for RP Mode.	0x0
4:1	R/W	Gen3 EQ Phase2 Remote Tx Preset [G3RMTXPR]	Used only in EP Mode. When enabled using bit-0, this Tx Preset will be transmitted in TS1s for the Remote end Transmitter in the first iteration of Gen3 Equalization Phase2. Reserved for RP Mode.	0x0
5	R/W	Gen3 Local Override Tx Preset Enable [G3OVRREN]	This is a debug bit. Can be used in both EP and RP Mode. If enabled, the Controller locally applies the Gen3 Local Override Tx Presetto the Local Transmitter throughout Gen3. The Controller performs the Override Preset to Coefficient mapping and then drives on PIPE_TX_DEEMPHASIS signal on the PIPE Interface.	0x0
9:6	R/W	Gen3 Local Override Tx Preset[G3OVRRPR]	This is a debug register field. Can be used in both EP and RP Mode. When enabled using bit-5, this Tx Preset will be applied to the local Transmitter throughout Gen3 regardless of Gen3 Equalization.	0x0
10	R/W	Gen4 EP 8GTEQ TS2 Enable [G4EQTSEN]	Used only in EP Mode. During Gen3 to Gen4 Speed Change negotiation, this bit enables the Controller in EP Mode to transmit 8G EQ TS2 in Recovery.Rcvr.Cfg state instead of standard TS2 as defined in PCIe specification. The Tx Preset that will be used in the 8GT EQ TS2 is programmable in bits [15:12] of this register.	0x0

Bits	SW	Name	Description	Reset
11	R/W	Gen4 EQ Phase2 Remote Tx Preset Enable [G4PRRMEN]	Used only in EP Mode. This bit enables the Controller, to feedback a Tx Preset for the Remote end Transmitter in the first iteration of Link Equalization Phase2 at Gen4 speed. The Gen4 Tx Preset that is used for feedback is programmable in bits [15:12] of this register.	0x0
15:12	R/W	Gen4 EQ Phase2 Remote Tx Preset [G4RMTXPR]	Used only in EP Mode. If enabled, this Tx Preset will be transmitted in 8G EQ TS2s during Gen3 to Gen4 Speed Change negotiation. Also, if enabled, this Tx Preset will be transmitted in TS1s in the first iteration of Gen4 Equalization Phase2. *Note:* If the Remote end device advertised the same preset at start of Equalization Phase2, then this Preset will be skipped.	0x0
16	R/W	Gen4 Local Tx Preset Override Enable [G4OVRREN]	This is a debug bit. Can be used in both EP and RP Mode. If enabled, the Controller locally applies the Gen4 Local Override Tx Presetto the Local Transmitter throughout Gen4. The Controller performs the Override Preset to Coefficient mapping and then drives on PIPE_TX_DEEMPHASIS signal on the PIPE Interface.	0x0
20:17	R/W	Gen4 Local Override Tx Preset [G4OVRRPR]	This is a debug register field. Can be used in both EP and RP Mode. When enabled using bit-16, this Tx Preset will be applied to the local Transmitter throughout Gen4 regardless of Gen4 Equalization.	0x0
31:21	R	Reserved [R21]	Reserved	0x0

Core Feature Control Register @0xe64

This register is for the control of Core Features.

Table 407: i_core_feature_reg

Bits	SW	Name	Description	Reset
0	R	Reserved [R0]	Reserved	0x0
1	R/W	APB Access Clock Shutoff SLVERR select [APBCTRL]	When set the Core will return SLVERR on the APB bus for Read or Writes to Configuration or Local Management registers.	0x0
2	R	Reserved [R2]	Reserved	0x0
31:3	R	Reserved [R30]	Reserved	0x0

Polarity inversion Register @0xe88

This register shows the polarity inversion status of each lane.

Table 408: i_rx_invert_polarity_reg

Bits	SW	Name	Description	Reset
3:0	R	Polarity inversion status [RIPR]	Shows the polarity inversion status of each lane.	0x0
31:4	R	Reserved [R30]	Reserved	0x0

LTSSM Transition Debug Control Register01 @0xf90

This register enables firmware to program two specific LTSSM state transitions to be detected and optionally paused for firmware control.

Table 409: i_ltssm_transition_debug_ctrl_reg01

Bits	SW	Name	Description	Reset
0	R/W	LTSSM State Transition 0 Freeze Enable [LST0FREN]	This bit can be used by firmware to freeze the LTSSM after the programmed LTSSM transition 0 occurs. • 1: LTSSM State will be frozen after the programmed transition 0. LTSSM will stay in current_state, by dropping all OS being received. • 0: LTSSM State will not be frozen after the programmed transition 0. LTSSM will continue to next legal state.	0x0
1	R/W	LTSSM State Transition 0 Check Enable [LST0CHEN]	This bit enables the LTSSM transition 0 check. • 1: LTSSM State transition 0 check is enabled. • 0: LTSSM State transition 0 check is disabled.	0x0
8:2	R/W	Current LTSSM State 0 [CLTST0]	This is the 7-bit Current LTSSM State of LTSSM transition 0 that is required to be checked and optionally paused. Please refer to the 7-bit LTSSM Encoding table for details.	0x0
15:9	R/W	Previous LTSSM State 0 [PLTST0]	This is the 7-bit Previous LTSSM State of LTSSM transition 0 that is required to be checked. Please refer to the 7-bit LTSSM Encoding table for details.	0x0
16	R/W	LTSSM State Transition 1 Freeze Enable [LST1FREN]	This bit can be used by firmware to freeze the LTSSM after the programmed LTSSM transition 1 occurs. • 1: LTSSM State will be frozen after the programmed transition 1. LTSSM will stay in current_state, by dropping all OS being received. • 0: LTSSM State will not be frozen after the programmed transition 1. LTSSM will continue to next legal state.	0x0
17	R/W	LTSSM State Transition 1 Check Enable [LST1CHEN]	This bit enables the LTSSM transition 1 check. • 1: LTSSM State transition 1 check is enabled. • 0: LTSSM State transition 1 check is disabled.	0x0
24:18	R/W	Current LTSSM State 1 [CLTST1]	This is the 7-bit Current LTSSM State of LTSSM transition1 that is required to be checked and optionally paused. Please refer to the 7-bit LTSSM Encoding table for details.	0x0
31:25	R/W	Previous LTSSM State 1 [PLTST1]	This is the 7-bit Previous LTSSM State of LTSSM transition1 that is required to be checked. Please refer to the 7-bit LTSSM Encoding table for details.	0x0

LTSSM Transition Debug Control Register23 @0xf94

This register enables firmware to program two specific LTSSM state transitions to be detected and optionally paused for firmware control.

Table 410: i_ltssm_transition_debug_ctrl_reg23

Bits	SW	Name	Description	Reset
0	R/W	LTSSM State Transition 2 Freeze Enable [LST2FREN]	This bit can be used by firmware to freeze the LTSSM after the programmed LTSSM transition 2 occurs. • 1: LTSSM State will be frozen after the programmed transition 2. LTSSM will stay in current_state, by dropping all OS being received. • 0: LTSSM State will not be frozen after the programmed transition 2. LTSSM will continue to next legal state.	0x0
1	R/W	LTSSM State Transition 2 Check Enable [LST2CHEN]	This bit enables the LTSSM transition 2 check. • 1: LTSSM State transition 2 check is enabled. • 0: LTSSM State transition 2 check is disabled.	0x0
8:2	R/W	Current LTSSM State 2 [CLTST2]	This is the 7-bit Current LTSSM State of LTSSM transition 2 that is required to be checked and optionally paused. Please refer to the 7-bit LTSSM Encoding table for details.	0x0
15:9	R/W	Previous LTSSM State 2 [PLTST2]	This is the 7-bit Previous LTSSM State of LTSSM transition 2 that is required to be checked. Please refer to the 7-bit LTSSM Encoding table for details.	0x0
16	R/W	LTSSM State Transition 3 Freeze Enable [LST3FREN]	This bit can be used by firmware to freeze the LTSSM after the programmed LTSSM transition 3 occurs. • 1: LTSSM State will be frozen after the programmed transition 3. LTSSM will stay in current_state, by dropping all OS being received. • 0: LTSSM State will not be frozen after the programmed transition 3. LTSSM will continue to next legal state.	0x0
17	R/W	LTSSM State Transition 3 Check Enable [LST3CHEN]	This bit enables the LTSSM transition 1 check. • 1: LTSSM State transition 3 check is enabled. • 0: LTSSM State transition 3 check is disabled.	0x0
24:18	R/W	Current LTSSM State 3 [CLTST3]	This is the 7-bit Current LTSSM State of LTSSM transition 3 that is required to be checked and optionally paused. Please refer to the 7-bit LTSSM Encoding table for details.	0x0
31:25	R/W	Previous LTSSM State 3 [PLTST3]	This is the 7-bit Previous LTSSM State of LTSSM transition 3 that is required to be checked. Please refer to the 7-bit LTSSM Encoding table for details.	0x0

LTSSM Transition Debug Control Register45 @0xf98

This register enables firmware to program two specific LTSSM state transitions to be detected and optionally paused for firmware control.

Table 411: i_ltssm_transition_debug_ctrl_reg45

Bits	SW	Name	Description	Reset
0	R/W	LTSSM State Transition 4 Freeze Enable [LST4FREN]	This bit can be used by firmware to freeze the LTSSM after the programmed LTSSM transition 4 occurs. • 1: LTSSM State will be frozen after the programmed transition 4. LTSSM will stay in current_state, by dropping all OS being received. • 0: LTSSM State will not be frozen after the programmed transition 4. LTSSM will continue to next legal state.	0x0

Bits	SW	Name	Description	Reset
1	R/W	LTSSM State Transition 4 Check Enable [LST4CHEN]	This bit enables the LTSSM transition 4 check. • 1: LTSSM State transition 4 check is enabled. • 0: LTSSM State transition 4 check is disabled.	0x0
8:2	R/W	Current LTSSM State 4 [CLTST4]	This is the 7-bit Current LTSSM State of LTSSM transition 4 that is required to be checked and optionally paused. Please refer to the 7-bit LTSSM Encoding table for details.	0x0
15:9	R/W	Previous LTSSM State 4 [PLTST4]	This is the 7-bit Previous LTSSM State of LTSSM transition 4 that is required to be checked. Please refer to the 7-bit LTSSM Encoding table for details.	0x0
16	R/W	LTSSM State Transition 5 Freeze Enable [LST5FREN]	This bit can be used by firmware to freeze the LTSSM after the programmed LTSSM transition 5 occurs. • 1: LTSSM State will be frozen after the programmed transition 5. LTSSM will stay in current_state, by dropping all OS being received. • 0: LTSSM State will not be frozen after the programmed transition 5. LTSSM will continue to next legal state.	0x0
17	R/W	LTSSM State Transition 5 Check Enable [LST5CHEN]	This bit enables the LTSSM transition 1 check. • 1: LTSSM State transition 5 check is enabled. • 0: LTSSM State transition 5 check is disabled.	0x0
24:18	R/W	Current LTSSM State 5 [CLTST5]	This is the 7-bit Current LTSSM State of LTSSM transition 5 that is required to be checked and optionally paused. Please refer to the 7-bit LTSSM Encoding table for details.	0x0
31:25	R/W	Previous LTSSM State 5 [PLTST5]	This is the 7-bit Previous LTSSM State of LTSSM transition 5 that is required to be checked. Please refer to the 7-bit LTSSM Encoding table for details.	0x0

LTSSM Transition Debug Control Register67 @0xf9c

This register enables firmware to program two specific LTSSM state transitions to be detected and optionally paused for firmware control.

Table 412: i_ltssm_transition_debug_ctrl_reg67

Bits	SW	Name	Description	Reset
0	R/W	LTSSM State Transition 6 Freeze Enable [LST6FREN]	This bit can be used by firmware to freeze the LTSSM after the programmed LTSSM transition 6 occurs. • 1: LTSSM State will be frozen after the programmed transition 6. LTSSM will stay in current_state, by dropping all OS being received. • 0: LTSSM State will not be frozen after the programmed transition 6. LTSSM will continue to next legal state.	0x0
1	R/W	LTSSM State Transition 6 Check Enable [LST6CHEN]	This bit enables the LTSSM transition 4 check. • 1: LTSSM State transition 6 check is enabled. • 0: LTSSM State transition 6 check is disabled.	0x0
8:2	R/W	Current LTSSM State 6 [CLTST6]	This is the 7-bit Current LTSSM State of LTSSM transition6 that is required to be checked and optionally paused. Please refer to the 7-bit LTSSM Encoding table for details.	0x0
15:9	R/W	Previous LTSSM State 6 [PLTST6]	This is the 7-bit Previous LTSSM State of LTSSM transition6 that is required to be checked. Please refer to the 7-bit LTSSM Encoding table for details.	0x0
16	R/W	LTSSM State Transition 7 Freeze Enable [LST7FREN]	This bit can be used by firmware to freeze the LTSSM after the programmed LTSSM transition 7 occurs. • 1: LTSSM State will be frozen after the programmed transition 7. LTSSM will stay in current_state, by dropping all OS being received. • 0: LTSSM State will not be frozen after the programmed transition 7. LTSSM will continue to next legal state.	0x0

Bits	SW	Name	Description	Reset
17	R/W	LTSSM State Transition 7 Check Enable [LST7CHEN]	This bit enables the LTSSM transition 1 check. • 1: LTSSM State transition 7 check is enabled. • 0: LTSSM State transition 7 check is disabled.	0x0
24:18	R/W	Current LTSSM State 7 [CLTST7]	This is the 7-bit Current LTSSM State of LTSSM transition7 that is required to be checked and optionally paused. Please refer to the 7-bit LTSSM Encoding table for details.	0x0
31:25	R/W	Previous LTSSM State 7 [PLTST7]	This is the 7-bit Previous LTSSM State of LTSSM transition7 that is required to be checked. Please refer to the 7-bit LTSSM Encoding table for details.	0x0

LTSSM Transition Debug Status Register @0xfa0

This register reflects the Status of the eight LTSSM State Transitions that can be programmed for firmware monitor and control.

Table 413: i_ltssm_transition_debug_stat_reg

Bits	SW	Name	Description	Reset
7:0	R/ WOCLR	LTSSM State Transition Without Freeze Status [LSTWOFR]	This field contains status 1-bit for each of the eight programmable LTSSM State transitions. • 1: Indicates the programmed LTSSM transition occured and was not programmed to freeze on that transition. • 0: Indicates that either the programmed LTSSM transition has not occured or was programmed to freeze. Write 1 to Clear.	0x0
15:8	R/ WOCLR	LTSSM State Transition With Freeze Status [LSTWFR]	This field contains status 1-bit for each of the eight programmable LTSSM State transitions. • 1: Indicates the programmed LTSSM transition occured and was programmed to freeze on that transition. LTSSM is frozen at the Current LTSSM State, waiting for firmware intervention to un-freeze. • 0: Indicates that either the programmed LTSSM transition has not occured or was not programmed to freeze. Write 1 to Clear.	0x0
31:16	R	Reserved [R16]	Reserved	0x0

LTSSM Transition Cause Status Register @0xfa4

This register reflects the most recent LTSSM State Transition and the Cause for the Transition.

Table 414: i_ltssm_transition_cause_stat_reg

Bits	SW	Name	Description	Reset
6:0	R	Previous LTSSM State [PRLTST]	This field contains the 7-bit Previous LTSSM State of the most recent LTSSM Transition.	0x0
13:7	R	Current LTSSM State [CRLTST]	This field contains the 7-bit Current LTSSM State of the most recent LTSSM Transition.	0x0
21:14	R/ WOCLR	LTSSM State Transition Cause [LTSTTRC]	This field contains the 8-bit encoded value of the cause of the most recent LTSSM Transition.	0x0
31:22	R	Reserved [R22]	Reserved	0x0

LTSSM Timer Control Register0 @0xfac

This register enables control of the LTSSM 1 ms and 2 ms timeout limits.

Table 415: i_ltssm_timer_control_reg0

Bits	SW	Name	Description	Reset
11:0	R/W	LTSSM 1ms Time Interval [L1MSTM]	This register holds the LTSSM 1 ms timer interval in units of (1024 ns). This register can be tuned to vary the 1 ms timeout in the LTSSM. Default value is set to 16'd977 to get exact time interval of 1 ms.	12'd977
15:12	R	Reserved [R12]	Reserved	0x0
27:16	R/W	LTSSM 2ms Time Interval [L2MSTM]	This register holds the LTSSM 2 ms timer interval in units of (1024 ns). This register can be tuned to vary the 2 ms timeout in the LTSSM. Default value is set to 16'd1954 to get exact time interval of 2 ms.	12'd1954
31:28	R	Reserved [R28]	Reserved	0x0

LTSSM Timer Control Register1 @0xfb0

This register enables control of the LTSSM 4 ms and 8 ms timeout limits.

Table 416: i_ltssm_timer_control_reg1

Bits	SW	Name	Description	Reset
15:0	R/W	LTSSM 4 ms Time Interval [L4MSTM]	This register holds the LTSSM 4 ms timer interval in units of (1024 ns). This register can be tuned to vary the 4 ms timeout in the LTSSM. Default value is set to 16'd3907 to get exact time interval of 4 ms.	16'd3907
31:16	R/W	LTSSM 8 ms Time Interval [L8MSTM]	This register holds the LTSSM 8 ms timer interval in units of (1024 ns). This register can be tuned to vary the 8 ms timeout in the LTSSM. Default value is set to 16'd7813 to get exact time interval of 8 ms.	16'd7813

LTSSM Timer Control Register2 @0xfb4

This register enables control of the LTSSM 12 ms and 24 ms timeout limits.

Table 417: i_ltssm_timer_control_reg2

Bits	SW	Name	Description	Reset
15:0	R/W	LTSSM 12 msTime Interval [L12MSTM]	This register holds the LTSSM 12 ms timer interval in units of (1024 ns). This register can be tuned to vary the 12 ms timeout in the LTSSM. Default value is set to 16'd11_719 to get exact time interval of 24 ms.	16'd11719
31:16	R/W	LTSSM 24 msTime Interval [L24MSTM]	This register holds the LTSSM 24 ms timer interval in units of (1024 ns). This register can be tuned to vary the 24 ms timeout in the LTSSM. Default value is set to 16'd23_438 to get exact time interval of 24 ms.	16'd23438

LTSSM Timer Control Register3 @0xfb8

This register enables control of the LTSSM 32 ms and 48 ms timeout limits.

Table 418: i_ltssm_timer_control_reg3

Bits	SW	Name	Description	Reset
15:0	R/W	LTSSM 32 ms Time Interval [L32MSTM]	This register holds the LTSSM 32 ms timer interval in units of (1024 ns). This register can be tuned to vary the 32 ms timeout in the LTSSM. Default value is set to 16'd31_250 to get exact time interval of 32 ms.	16'd31250

Bits	SW	Name	Description	Reset
31:16	R/W	LTSSM 48 ms Time Interval [L48MSTM]	This register holds the LTSSM 48 ms timer interval in units of (1024 ns). This register can be tuned to vary the 48 ms timeout in the LTSSM. Default value is set to 16'd46_875 to get exact time interval of 48 ms.	16'd46875

AXI Configuration Registers

The AXI configuration registers with their descriptions are listed in the sections below. For detailed PCIe descriptor fields, please refer to AXI Inbound Access.

Region 0 Outbound AXI to PCIe Address Translation Register 0 @0x0

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 419: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 0 Outbound AXI to PCIe Address Translation Register 1 @0x4

Provides bits 63:32 of the PCIe address.

Table 420: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 0 Outbound PCIe Descriptor Register 0 @0x8

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 421: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 0 Outbound PCIe Descriptor Register 1 @0xc

Provides bits 63:32 of the PCIe Descriptor.

Table 422: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 0 Outbound PCIe Descriptor Register 2 @0x10

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 423: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 0 Outbound PCIe Descriptor Register 3 @0x14

Provides PASID Value and the present bit.

Table 424: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 0 AXI Region Base Address Register 0 @0x18

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 425: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 0 AXI Region Base Address 1 @0x1c

Holds the base address [63:32] of this region.

Table 426: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 1 Outbound AXI to PCIe Address Translation Register 0 @0x20

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 427: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 1 Outbound AXI to PCIe Address Translation Register 1 @0x24

Provides bits 63:32 of the PCIe address.

Table 428: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 1 Outbound PCIe Descriptor Register 0 @0x28

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 429: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 1 Outbound PCIe Descriptor Register 1 @0x2c

Provides bits 63:32 of the PCIe Descriptor.

Table 430: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 1 Outbound PCIe Descriptor Register 2 @0x30

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 431: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 1 Outbound PCIe Descriptor Register 3 @0x34

Provides PASID Value and the present bit.

Table 432: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 1 AXI Region Base Address Register 0 @0x38

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 433: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 1 AXI Region Base Address 1 @0x3c

Holds the base address [63:32] of this region.

Table 434: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 2 Outbound AXI to PCIe Address Translation Register 0 @0x40

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 435: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 2 Outbound AXI to PCIe Address Translation Register 1 @0x44

Provides bits 63:32 of the PCIe address.

Table 436: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 2 Outbound PCIe Descriptor Register 0 @0x48

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 437: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 2 Outbound PCIe Descriptor Register 1 @0x4c

Provides bits 63:32 of the PCIe Descriptor.

Table 438: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 2 Outbound PCIe Descriptor Register 2 @0x50

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 439: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 2 Outbound PCIe Descriptor Register 3 @0x54

Provides PASID Value and the present bit

Table 440: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 2 AXI Region Base Address Register 0 @0x58

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 441: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 2 AXI Region Base Address 1 @0x5c

Holds the base address [63:32] of this region.

Table 442: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region	32'h00000000

Region 3 Outbound AXI to PCIe Address Translation Register 0 @0x60

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 443: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 3 Outbound AXI to PCIe Address Translation Register 1 @0x64

Provides bits 63:32 of the PCIe address.

Table 444: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 3 Outbound PCIe Descriptor Register 0 @0x68

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 445: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 3 Outbound PCIe Descriptor Register 1 @0x6c

Provides bits 63:32 of the PCIe Descriptor.

Table 446: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 3 Outbound PCIe Descriptor Register 2 @0x70

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 447: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 3 Outbound PCIe Descriptor Register 3 @0x74

Provides PASID Value and the present bit.

Table 448: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 3 AXI Region Base Address Register 0 @0x78

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 449: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 3 AXI Region Base Address 1 @0x7c

Holds the base address [63:32] of this region.

Table 450: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 4 Outbound AXI to PCIe Address Translation Register 0 @0x80

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 451: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 4 Outbound AXI to PCIe Address Translation Register 1 @0x84

Provides bits 63:32 of the PCIe address.

Table 452: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 4 Outbound PCIe Descriptor Register 0 @0x88

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 453: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 4 Outbound PCIe Descriptor Register 1 @0x8c

Provides bits 63:32 of the PCIe Descriptor.

Table 454: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 4 Outbound PCIe Descriptor Register 2 @0x90

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 455: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 4 Outbound PCIe Descriptor Register 3 @0x94

Provides PASID Value and the present bit.

Table 456: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 4 AXI Region Base Address Register 0 @0x98

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 457: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 4 AXI Region Base Address 1 @0x9c

Holds the base address [63:32] of this region.

Table 458: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 5 Outbound AXI to PCIe Address Translation Register 0 @0xa0

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 459: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 5 Outbound AXI to PCIe Address Translation Register 1 @0xa4

Provides bits 63:32 of the PCIe address.

Table 460: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 5 Outbound PCIe Descriptor Register 0 @0xa8

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 461: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 5 Outbound PCIe Descriptor Register 1 @0xac

Provides bits 63:32 of the PCIe Descriptor.

Table 462: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 5 Outbound PCIe Descriptor Register 2 @0xb0

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 463: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 5 Outbound PCIe Descriptor Register 3 @0xb4

Provides PASID Value and the present bit.

Table 464: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 5 AXI Region Base Address Register 0 @0xb8

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 465: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 5 AXI Region Base Address 1 @0xbc

Holds the base address [63:32] of this region.

Table 466: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 6 Outbound AXI to PCIe Address Translation Register 0 @0xc0

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 467: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 6 Outbound AXI to PCIe Address Translation Register 1 @0xc4

Provides bits 63:32 of the PCIe address.

Table 468: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 6 Outbound PCIe Descriptor Register 0 @0xc8

Provides bits 31:0 of the Outbound PCIe Descriptor

Table 469: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N	32'h00000000

Region 6 Outbound PCIe Descriptor Register 1 @0xcc

Provides bits 63:32 of the PCIe Descriptor.

Table 470: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 6 Outbound PCIe Descriptor Register 2 @0xd0

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 471: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 6 Outbound PCIe Descriptor Register 3 @0xd4

Provides PASID Value and the present bit.

Table 472: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 6 AXI Region Base Address Register 0 @0xd8

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 473: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 6 AXI Region Base Address 1 @0xdc

Holds the base address [63:32] of this region.

Table 474: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 7 Outbound AXI to PCIe Address Translation Register 0 @0xe0

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 475: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 7 Outbound AXI to PCIe Address Translation Register 1 @0xe4

Provides bits 63:32 of the PCIe address.

Table 476: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 7 Outbound PCIe Descriptor Register 0 @0xe8

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 477: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 7 Outbound PCIe Descriptor Register 1 @0xec

Provides bits 63:32 of the PCIe Descriptor.

Table 478: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 7 Outbound PCIe Descriptor Register 2 @0xf0

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 479: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 7 Outbound PCIe Descriptor Register 3 @0xf4

Provides PASID Value and the present bit.

Table 480: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 7 AXI Region Base Address Register 0 @0xf8

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 481: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 7 AXI Region Base Address 1 @0xfc

Holds the base address [63:32] of this region.

Table 482: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 8 Outbound AXI to PCIe Address Translation Register 0 @0x100

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 483: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 8 Outbound AXI to PCIe Address Translation Register 1 @0x104

Provides bits 63:32 of the PCIe address.

Table 484: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 8 Outbound PCIe Descriptor Register 0 @0x108

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 485: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 8 Outbound PCIe Descriptor Register 1 @0x10c

Provides bits 63:32 of the PCIe Descriptor.

Table 486: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 8 Outbound PCIe Descriptor Register 2 @0x110

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 487: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 8 Outbound PCIe Descriptor Register 3 @0x114

Provides PASID Value and the present bit.

Table 488: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 8 AXI Region Base Address Register 0 Register 0 Address @0x118

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 489: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 8 AXI Region Base Address 1 @0x11c

Holds the base address [63:32] of this region.

Table 490: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 9 Outbound AXI to PCIe Address Translation Register 0 @0x120

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 491: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 9 Outbound AXI to PCIe Address Translation Register 1 @0x124

Provides bits 63:32 of the PCIe address.

Table 492: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 9 Outbound PCIe Descriptor Register 0 @0x128

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 493: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 9 Outbound PCIe Descriptor Register 1 @0x12c

Provides bits 63:32 of the PCIe Descriptor.

Table 494: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 9 Outbound PCIe Descriptor Register 2 @0x130

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 495: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 9 Outbound PCIe Descriptor Register 3 @0x134

Provides PASID Value and the present bit.

Table 496: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 9 AXI Region Base Address Register 0 Register 0 Address @0x138

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 497: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 9 AXI Region Base Address 1 @0x13c

Holds the base address [63:32] of this region.

Table 498: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 10 Outbound AXI to PCIe Address Translation Register 0 @0x140

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 499: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 10 Outbound AXI to PCIe Address Translation Register 1 @0x144

Provides bits 63:32 of the PCIe address.

Table 500: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 10 Outbound PCIe Descriptor Register 0 @0x148

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 501: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 10 Outbound PCIe Descriptor Register 1 @0x14c

Provides bits 63:32 of the PCIe Descriptor.

Table 502: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 10 Outbound PCIe Descriptor Register 2 @0x150

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 503: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 10 Outbound PCIe Descriptor Register 3 @0x154

Provides PASID Value and the present bit.

Table 504: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 10 AXI Region Base Address Register 0 Register 0 Address @0x158

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 505: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 10 AXI Region Base Address 1 @0x15c

Holds the base address [63:32] of this region.

Table 506: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 11 Outbound AXI to PCIe Address Translation Register 0 @0x160

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 507: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 11 Outbound AXI to PCIe Address Translation Register 1 @0x164

Provides bits 63:32 of the PCIe address.

Table 508: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 11 Outbound PCIe Descriptor Register 0 @0x168

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 509: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 11 Outbound PCIe Descriptor Register 1 @0x16c

Provides bits 63:32 of the PCIe Descriptor.

Table 510: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 11 Outbound PCIe Descriptor Register 2 @0x170

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 511: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 11 Outbound PCIe Descriptor Register 3 @0x174

Provides PASID Value and the present bit.

Table 512: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 11 AXI Region Base Address Register 0 @0x178

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 513: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 11 AXI Region Base Address 1 @0x17c

Holds the base address [63:32] of this region.

Table 514: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 12 Outbound AXI to PCIe Address Translation Register 0 @0x180

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 515: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 12 Outbound AXI to PCIe Address Translation Register 1 @0x184

Provides bits 63:32 of the PCIe address.

Table 516: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 12 Outbound PCIe Descriptor Register 0 @0x188

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 517: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 12 Outbound PCIe Descriptor Register 1 @0x18c

Provides bits 63:32 of the PCIe Descriptor.

Table 518: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 12 Outbound PCIe Descriptor Register 2 @0x190

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 519: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 12 Outbound PCIe Descriptor Register 3 @0x194

Provides PASID Value and the present bit.

Table 520: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 12 AXI Region Base Address Register 0 @0x198

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 521: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 12 AXI Region Base Address 1 @0x19c

Holds the base address [63:32] of this region.

Table 522: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 13 Outbound AXI to PCIe Address Translation Register 0 @0x1a0

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 523: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 13 Outbound AXI to PCIe Address Translation Register 1 @0x1a4

Provides bits 63:32 of the PCIe address.

Table 524: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 13 Outbound PCIe Descriptor Register 0 @0x1a8

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 525: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 13 Outbound PCIe Descriptor Register 1 @0x1ac

Provides bits 63:32 of the PCIe Descriptor.

Table 526: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 13 Outbound PCIe Descriptor Register 2 @0x1b0

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 527: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 13 Outbound PCIe Descriptor Register 3 @0x1b4

Provides PASID Value and the present bit.

Table 528: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 13 AXI Region Base Address Register 0 @0x1b8

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 529: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 13 AXI Region Base Address 1 @0x1bc

Holds the base address [63:32] of this region.

Table 530: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 14 Outbound AXI to PCIe Address Translation Register 0 @0x1c0

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 531: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 14 Outbound AXI to PCIe Address Translation Register 1 @0x1c4

Provides bits 63:32 of the PCIe address.

Table 532: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 14 Outbound PCIe Descriptor Register 0 @0x1c8

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 533: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 14 Outbound PCIe Descriptor Register 1 @0x1cc

Provides bits 63:32 of the PCIe Descriptor.

Table 534: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 14 Outbound PCIe Descriptor Register 2 @0x1d0

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 535: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 14 Outbound PCIe Descriptor Register 3 @0x1d4

Provides PASID Value and the present bit.

Table 536: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 14 AXI Region Base Address Register 0 @0x1d8

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 537: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 14 AXI Region Base Address 1 @0x1dc

Holds the base address [63:32] of this region.

Table 538: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 15 Outbound AXI to PCIe Address Translation Register 0 @0x1e0

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 539: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 15 Outbound AXI to PCIe Address Translation Register 1 @0x1e4

Provides bits 63:32 of the PCIe address.

Table 540: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 15 Outbound PCIe Descriptor Register 0 @0x1e8

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 541: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 15 Outbound PCIe Descriptor Register 1 @0x1ec

Provides bits 63:32 of the PCIe Descriptor.

Table 542: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 15 Outbound PCIe Descriptor Register 2 @0x1f0

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 543: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 15 Outbound PCIe Descriptor Register 3 @0x1f4

Provides PASID Value and the present bit.

Table 544: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 15 AXI Region Base Address Register 0 @0x1f8

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 545: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 15 AXI Region Base Address 1 @0x1fc

Holds the base address [63:32] of this region.

Table 546: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 16 Outbound AXI to PCIe Address Translation Register 0 @0x200

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 547: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 16 Outbound AXI to PCIe Address Translation Register 1 @0x204

Provides bits 63:32 of the PCIe address.

Table 548: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 16 Outbound PCIe Descriptor Register 0 @0x208

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 549: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 16 Outbound PCIe Descriptor Register 1 @0x20c

Provides bits 63:32 of the PCIe Descriptor.

Table 550: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 16 Outbound PCIe Descriptor Register 2 @0x210

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 551: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 16 Outbound PCIe Descriptor Register 3 @0x214

Provides PASID Value and the present bit.

Table 552: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 16 AXI Region Base Address Register 0 @0x218

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 553: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 16 AXI Region Base Address 1 @0x21c

Holds the base address [63:32] of this region.

Table 554: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 17 Outbound AXI to PCIe Address Translation Register 0 @0x220

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 555: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 17 Outbound AXI to PCIe Address Translation Register 1 @0x224

Provides bits 63:32 of the PCIe address.

Table 556: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 17 Outbound PCIe Descriptor Register 0 @0x228

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 557: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 17 Outbound PCIe Descriptor Register 1 @0x22c

Provides bits 63:32 of the PCIe Descriptor.

Table 558: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 17 Outbound PCIe Descriptor Register 2 @0x230

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 559: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 17 Outbound PCIe Descriptor Register 3 @0x234

Provides PASID Value and the present bit.

Table 560: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 17 AXI Region Base Address Register 0 @0x238

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 561: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 17 AXI Region Base Address 1 @0x23c

Holds the base address [63:32] of this region.

Table 562: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 18 Outbound AXI to PCIe Address Translation Register 0 @0x240

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 563: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0][num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 18 Outbound AXI to PCIe Address Translation Register 1 @0x244

Provides bits 63:32 of the PCIe address.

Table 564: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 18 Outbound PCIe Descriptor Register 0 @0x248

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 565: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 18 Outbound PCIe Descriptor Register 1 @0x24c

Provides bits 63:32 of the PCIe Descriptor.

Table 566: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 18 Outbound PCIe Descriptor Register 2 @0x250

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 567: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 18 Outbound PCIe Descriptor Register 3 @0x254

Provides PASID Value and the present bit.

Table 568: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 18 AXI Region Base Address Register 0 @0x258

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 569: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 18 AXI Region Base Address 1 @0x25c

Holds the base address [63:32] of this region.

Table 570: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 19 Outbound AXI to PCIe Address Translation Register 0 @0x260

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 571: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 19 Outbound AXI to PCIe Address Translation Register 1 @0x264

Provides bits 63:32 of the PCIe address.

Table 572: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 19 Outbound PCIe Descriptor Register 0 @0x268

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 573: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 19 Outbound PCIe Descriptor Register 1 @0x26c

Provides bits 63:32 of the PCIe Descriptor.

Table 574: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 19 Outbound PCIe Descriptor Register 2 @0x270

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 575: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 19 Outbound PCIe Descriptor Register 3 @0x274

Provides PASID Value and the present bit.

Table 576: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 19 AXI Region Base Address Register 0 @0x278

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 577: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	the value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 19 AXI Region Base Address 1 @0x27c

Holds the base address [63:32] of this region.

Table 578: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 20 Outbound AXI to PCIe Address Translation Register 0 @0x280

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 579: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 20 Outbound AXI to PCIe Address Translation Register 1 @0x284

Provides bits 63:32 of the PCIe address.

Table 580: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 20 Outbound PCIe Descriptor Register 0 @0x288

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 581: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 20 Outbound PCIe Descriptor Register 1 @0x28c

Provides bits 63:32 of the PCIe Descriptor.

Table 582: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 20 Outbound PCIe Descriptor Register 2 @0x290

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 583: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 20 Outbound PCIe Descriptor Register 3 @0x294

Provides PASID Value and the present bit.

Table 584: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 20 AXI Region Base Address Register 0 @0x298

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 585: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 20 AXI Region Base Address 1 @0x29c

Holds the base address [63:32] of this region.

Table 586: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 21 Outbound AXI to PCIe Address Translation Register 0 @0x2a0

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 587: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 21 Outbound AXI to PCIe Address Translation Register 1 @0x2a4

Provides bits 63:32 of the PCIe address.

Table 588: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 21 Outbound PCIe Descriptor Register 0 @0x2a8

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 589: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 21 Outbound PCIe Descriptor Register 1 @0x2ac

Provides bits 63:32 of the PCIe Descriptor.

Table 590: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 21 Outbound PCIe Descriptor Register 2 @0x2b0

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 591: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 21 Outbound PCIe Descriptor Register 3 @0x2b4

Provides PASID Value and the present bit.

Table 592: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 21 AXI Region Base Address Register 0 @0x2b8

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 593: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 21 AXI Region Base Address 1 @0x2bc

Holds the base address [63:32] of this region.

Table 594: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 22 Outbound AXI to PCIe Address Translation Register 0 @0x2c0

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 595: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 22 Outbound AXI to PCIe Address Translation Register 1 @0x2c4

Provides bits 63:32 of the PCIe address.

Table 596: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 22 Outbound PCIe Descriptor Register 0 @0x2c8

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 597: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 22 Outbound PCIe Descriptor Register 1 @0x2cc

Provides bits 63:32 of the PCIe Descriptor.

Table 598: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 22 Outbound PCIe Descriptor Register 2 @0x2d0

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 599: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 22 Outbound PCIe Descriptor Register 3 @0x2d4

Provides PASID Value and the present bit.

Table 600: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 22 AXI Region Base Address Register 0 @0x2d8

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 601: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 22 AXI Region Base Address 1 @0x2dc

Holds the base address [63:32] of this region.

Table 602: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 23 Outbound AXI to PCIe Address Translation Register 0 @0x2e0

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 603: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 23 Outbound AXI to PCIe Address Translation Register 1 @0x2e4

Provides bits 63:32 of the PCIe address.

Table 604: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 23 Outbound PCIe Descriptor Register 0 @0x2e8

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 605: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 23 Outbound PCIe Descriptor Register 1 @0x2ec

Provides bits 63:32 of the PCIe Descriptor.

Table 606: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 23 Outbound PCIe Descriptor Register 2 @0x2f0

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 607: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 23 Outbound PCIe Descriptor Register 3 @0x2f4

Provides PASID Value and the present bit.

Table 608: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 23 AXI Region Base Address Register 0 @0x2f8

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 609: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 23 AXI Region Base Address 1 @0x2fc

Holds the base address [63:32] of this region.

Table 610: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 24 Outbound AXI to PCIe Address Translation Register 0 @0x300

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 611: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 24 Outbound AXI to PCIe Address Translation Register 1 @0x304

Provides bits 63:32 of the PCIe address.

Table 612: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 24 Outbound PCIe Descriptor Register 0 @0x308

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 613: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 24 Outbound PCIe Descriptor Register 1 @0x30c

Provides bits 63:32 of the PCIe Descriptor.

Table 614: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 24 Outbound PCIe Descriptor Register 2 @0x310

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 615: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 24 Outbound PCIe Descriptor Register 3 @0x314

Provides PASID Value and the present bit.

Table 616: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 24 AXI Region Base Address Register 0 @0x318

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 617: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 24 AXI Region Base Address 1 @0x31c

Holds the base address [63:32] of this region.

Table 618: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 25 Outbound AXI to PCIe Address Translation Register 0 @0x320

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 619: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 25 Outbound AXI to PCIe Address Translation Register 1 @0x324

Provides bits 63:32 of the PCIe address.

Table 620: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 25 Outbound PCIe Descriptor Register 0 @0x328

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 621: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 25 Outbound PCIe Descriptor Register 1 @0x32c

Provides bits 63:32 of the PCIe Descriptor.

Table 622: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 25 Outbound PCIe Descriptor Register 2 @0x330

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 623: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 25 Outbound PCIe Descriptor Register 3 @0x334

Provides PASID Value and the present bit.

Table 624: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 25 AXI Region Base Address Register 0 @0x338

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 625: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 25 AXI Region Base Address 1 @0x33c

Holds the base address [63:32] of this region.

Table 626: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 26 Outbound AXI to PCIe Address Translation Register 0 @0x340

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 627: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 26 Outbound AXI to PCIe Address Translation Register 1 @0x344

Provides bits 63:32 of the PCIe address.

Table 628: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 26 Outbound PCIe Descriptor Register 0 @0x348

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 629: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 26 Outbound PCIe Descriptor Register 1 @0x34c

Provides bits 63:32 of the PCIe Descriptor.

Table 630: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 26 Outbound PCIe Descriptor Register 2 @0x350

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 631: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 26 Outbound PCIe Descriptor Register 3 @0x354

Provides PASID Value and the present bit.

Table 632: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 26 AXI Region Base Address Register 0 @0x358

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 633: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 26 AXI Region Base Address 1 @0x35c

Holds the base address [63:32] of this region.

Table 634: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 27 Outbound AXI to PCIe Address Translation Register 0 @0x360

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 635: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 27 Outbound AXI to PCIe Address Translation Register 1 @0x364

Provides bits 63:32 of the PCIe address.

Table 636: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 27 Outbound PCIe Descriptor Register 0 @0x368

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 637: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 27 Outbound PCIe Descriptor Register 1 @0x36c

Provides bits 63:32 of the PCIe Descriptor.

Table 638: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 27 Outbound PCIe Descriptor Register 2 @0x370

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 639: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 27 Outbound PCIe Descriptor Register 3 @0x374

Provides PASID Value and the present bit.

Table 640: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 27 AXI Region Base Address Register 0 @0x378

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 641: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits[31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 27 AXI Region Base Address 1 @0x37c

Holds the base address [63:32] of this region.

Table 642: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 28 Outbound AXI to PCIe Address Translation Register 0 @0x380

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 643: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 28 Outbound AXI to PCIe Address Translation Register 1 @0x384

Provides bits 63:32 of the PCIe address.

Table 644: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 28 Outbound PCIe Descriptor Register 0 @0x388

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 645: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 28 Outbound PCIe Descriptor Register 1 @0x38c

Provides bits 63:32 of the PCIe Descriptor.

Table 646: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 28 Outbound PCIe Descriptor Register 2 @0x390

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 647: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 28 Outbound PCIe Descriptor Register 3 @0x394

Provides PASID Value and the present bit.

Table 648: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 28 AXI Region Base Address Register 0 @0x398

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 649: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 28 AXI Region Base Address 1 @0x39c

Holds the base address [63:32] of this region.

Table 650: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 29 Outbound AXI to PCIe Address Translation Register 0 @0x3a0

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 651: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 29 Outbound AXI to PCIe Address Translation Register 1 @0x3a4

Provides bits 63:32 of the PCIe address.

Table 652: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 29 Outbound PCIe Descriptor Register 0 @0x3a8

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 653: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 29 Outbound PCIe Descriptor Register 1 @0x3ac

Provides bits 63:32 of the PCIe Descriptor.

Table 654: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 29 Outbound PCIe Descriptor Register 2 @0x3b0

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 655: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 29 Outbound PCIe Descriptor Register 3 @0x3b4

Provides PASID Value and the present bit.

Table 656: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 29 AXI Region Base Address Register 0 @0x3b8

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 657: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 29 AXI Region Base Address 1 @0x3bc

Holds the base address [63:32] of this region.

Table 658: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 30 Outbound AXI to PCIe Address Translation Register 0 @0x3c0

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 659: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 30 Outbound AXI to PCIe Address Translation Register 1 @0x3c4

Provides bits 63:32 of the PCIe address.

Table 660: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 30 Outbound PCIe Descriptor Register 0 @0x3c8

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 661: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 30 Outbound PCIe Descriptor Register 1 @0x3cc

Provides bits 63:32 of the PCIe Descriptor.

Table 662: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 30 Outbound PCIe Descriptor Register 2 @0x3d0

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 663: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 30 Outbound PCIe Descriptor Register 3 @0x3d4

Provides PASID Value and the present bit.

Table 664: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 30 AXI Region Base Address Register 0 @0x3d8

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 665: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 30 AXI Region Base Address 1 @0x3dc

Holds the base address [63:32] of this region.

Table 666: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

Region 31 Outbound AXI to PCIe Address Translation Register 0 @0x3e0

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through.

Table 667: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	Number_bits + 1 bits are passed through from AXI address to the PCIe address.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	Address bits [31:8] [data]	Bits [31:8] of PCIe Address Register for region N.	24'h00000000

Region 31 Outbound AXI to PCIe Address Translation Register 1 @0x3e4

Provides bits 63:32 of the PCIe address.

Table 668: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of PCIe Address Register for region N.	32'h00000000

Region 31 Outbound PCIe Descriptor Register 0 @0x3e8

Provides bits 31:0 of the Outbound PCIe Descriptor.

Table 669: desc0

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [31:0] [data]	Lowest 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 31 Outbound PCIe Descriptor Register 1 @0x3ec

Provides bits 63:32 of the PCIe Descriptor.

Table 670: desc1

Bits	SW	Name	Description	Reset
31:0	R/W	Outbound PCIe Descriptor bits [63:32] [data]	Lower middle 32-bits of PCIe Descriptor Register for region N.	32'h00000000

Region 31 Outbound PCIe Descriptor Register 2 @0x3f0

Provides bits 76:64 of the Outbound PCIe Descriptor.

Table 671: desc2

Bits	SW	Name	Description	Reset
12:0	R/W	Outbound PCIe Descriptor bits [76:64] [data]	Upper middle 32-bits of PCIe Descriptor Register for region N.	13'd0
31:13	R	PCIe Descriptor bits [95:77] [rsvd]	Reserved	0x0

Region 31 Outbound PCIe Descriptor Register 3 @0x3f4

Provides PASID Value and the present bit.

Table 672: desc3

Bits	SW	Name	Description	Reset
22:0	R/W	PASID value and the present bit [data]	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}	23'd0
31:23	R	Reserved [rsvd]	Reserved	0x0

Region 31 AXI Region Base Address Register 0 @0x3f8

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability.

Table 673: axi_addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Region size [region_size]	The value programmed in this field + 1 gives the region size.	6'h0
7:6	R/W	Reserved bits [7:6] [rsvd]	These needs to be forced to 0.	2'h0
31:8	R/W	Outbound AXI Region Base Address bits [31:8] [data]	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region.	24'h00000000

Region 31 AXI Region Base Address 1 @0x3fc

Holds the base address [63:32] of this region.

Table 674: axi_addr1

Bits	SW	Name	Description	Reset
31:0	R/W	AXI Outbound Base Address bits [63:32] [data]	Bits [63:32] of AXI outbound Base Address Register used to decode the region.	32'h00000000

BAR 0 Root Port Inbound PCIe to AXI Address Translation Register [31:0] @0x800

Provides bits 31:8 of the AXI Address and the number of PCIE address bits passed through.

Table 675: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	The value programmed in this register +1 bits are passed through from PCIe to AXI.	6'h00
7:6	R	Reserved [rsvd0]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	AXI Address bits [31:8] [data]	Bits [31:8] of AXI Address Register for BAR N.	24'h00000000

BAR 0 Root Port Inbound PCIe to AXI Address Translation Register [63:32] @0x804

Provides bits 63:32 of the AXI Address.

Table 676: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] of the AXI [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

BAR 1 Root Port Inbound PCIe to AXI Address Translation Register [31:0] @0x808

Provides bits 31:8 of the AXI Address and the number of PCIE address bits passed through.

Table 677: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	The value programmed in this register +1 bits are passed through from PCIe to AXI.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	AXI Address bits [31:8] [data]	Bits [31:8] of AXI Address Register for BAR N.	24'h00000000

BAR 1 Root Port Inbound PCIe to AXI Address Translation Register [63:32] @0x80c

Provides bits 63:32 of the AXI Address.

Table 678: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] of the AXI [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

BAR 7 Root Port Inbound PCIe to AXI Address Translation Register [31:0] @0x810

Provides bits 31:8 of the AXI Address and the number of PCIE address bits passed through

Table 679: addr0

Bits	SW	Name	Description	Reset
5:0	R/W	Number_bits [5:0] [num_bits]	The value programmed in this register +1 bits are passed through from PCIe to AXI.	6'h00
7:6	R	Reserved [rsvd]	Bits 7 and 6 are reserved.	2'b00
31:8	R/W	AXI Address bits [31:8] [data]	Bits [31:8] of AXI Address Register for BAR N.	24'h00000000

BAR 7 Root Port Inbound PCIe to AXI Address Translation Register [63:32] @0x814

Provides bits 63:32 of the AXI Address.

Table 680: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] of the AXI [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Link Down Indication Bit @0x824

L0

Bits	SW	Name	Description	Reset
0	R/W	Link down indication bit [clear_link_down_bit_to_proceed]	When this bit is 1, the PCIe link is down, which triggers a hot reset (see **Link Control** > **Reset Types** > **Hot Reset** in the TJ-Series PCIe Controller User Guide). Upon hot reset, to recover and re-train the PCIe link, you must follow the reset handshake shown in **Link Control** > **Reset Handshake** in the user guide.	1'h0
31:1	R	RSVD	RSVD	31'h00000000

Function 0 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x840

Provides bits 31:0 of the AXI address.

Table 681: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 0 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x844

Provides bits 63:32 of the AXI address.

Table 682: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 0 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x848

Provides bits 31:0 of the AXI address.

Table 683: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 0 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x84c

Provides bits 63:32 of the AXI address.

Table 684: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 0 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x850

Provides bits 31:0 of the AXI address.

Table 685: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 0 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x854

Provides bits 63:32 of the AXI address.

Table 686: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 0 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x858

Provides bits 31:0 of the AXI address.

Table 687: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 0 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x85c

Provides bits 63:32 of the AXI address.

Table 688: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 0 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x860

Provides bits 31:0 of the AXI address.

Table 689: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 0 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x864

Provides bits 63:32 of the AXI address.

Table 690: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 0 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x868

Provides bits 31:0 of the AXI address.

Table 691: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 0 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x86c

Provides bits 63:32 of the AXI address.

Table 692: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 0 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x870

Provides bits 31:0 of the AXI address.

Table 693: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 0 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x874

Provides bits 63:32 of the AXI address.

Table 694: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x878

Provides bits 31:0 of the AXI address.

Table 695: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x87c

Provides bits 63:32 of the AXI address.

Table 696: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 1 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x880

Provides bits 31:0 of the AXI address.

Table 697: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 1 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x884

Provides bits 63:32 of the AXI address.

Table 698: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 1 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x888

Provides bits 31:0 of the AXI address.

Table 699: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 1 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x88c

Provides bits 63:32 of the AXI address.

Table 700: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 1 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x890

Provides bits 31:0 of the AXI address.

Table 701: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 1 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x894

Provides bits 63:32 of the AXI address.

Table 702: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 1 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x898

Provides bits 31:0 of the AXI address.

Table 703: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 1 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x89c

Provides bits 63:32 of the AXI address.

Table 704: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 1 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x8a0

Provides bits 31:0 of the AXI address.

Table 705: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 1 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x8a4

Provides bits 63:32 of the AXI address.

Table 706: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 1 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x8a8

Provides bits 31:0 of the AXI address.

Table 707: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 1 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x8ac

Provides bits 63:32 of the AXI address.

Table 708: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 1 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x8b0

Provides bits 31:0 of the AXI address.

Table 709: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 1 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x8b4

Provides bits 63:32 of the AXI address.

Table 710: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x8b8

Provides bits 31:0 of the AXI address.

Table 711: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x8bc

Provides bits 63:32 of the AXI address.

Table 712: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 2 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x8c0

Provides bits 31:0 of the AXI address.

Table 713: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 2 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x8c4

Provides bits 63:32 of the AXI address.

Table 714: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 2 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x8c8

Provides bits 31:0 of the AXI address.

Table 715: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 2 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x8cc

Provides bits 63:32 of the AXI address.

Table 716: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 2 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x8d0

Provides bits 31:0 of the AXI address.

Table 717: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 2 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x8d4

Provides bits 63:32 of the AXI address.

Table 718: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 2 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x8d8

Provides bits 31:0 of the AXI address.

Table 719: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 2 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x8dc

Provides bits 63:32 of the AXI address.

Table 720: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 2 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x8e0

Provides bits 31:0 of the AXI address.

Table 721: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 2 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x8e4

Provides bits 63:32 of the AXI address.

Table 722: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 2 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x8e8

Provides bits 31:0 of the AXI address.

Table 723: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 2 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x8ec

Provides bits 63:32 of the AXI address.

Table 724: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 2 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x8f0

Provides bits 31:0 of the AXI address.

Table 725: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 2 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x8f4

Provides bits 63:32 of the AXI address.

Table 726: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x8f8

Provides bits 31:0 of the AXI address.

Table 727: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x8fc

Provides bits 63:32 of the AXI address.

Table 728: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 3 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x900

Provides bits 31:0 of the AXI address.

Table 729: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 3 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x904

Provides bits 63:32 of the AXI address.

Table 730: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 3 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x908

Provides bits 31:0 of the AXI address.

Table 731: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 3 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x90c

Provides bits 63:32 of the AXI address.

Table 732: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 3 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x910

Provides bits 31:0 of the AXI address.

Table 733: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 3 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x914

Provides bits 63:32 of the AXI address.

Table 734: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 3 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x918

Provides bits 31:0 of the AXI address.

Table 735: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 3 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x91c

Provides bits 63:32 of the AXI address.

Table 736: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 3 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x920

Provides bits 31:0 of the AXI address.

Table 737: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 3 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x924

Provides bits 63:32 of the AXI address.

Table 738: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 3 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x928

Provides bits 31:0 of the AXI address.

Table 739: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 3 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x92c

Provides bits 63:32 of the AXI address.

Table 740: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 3 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x930

Provides bits 31:0 of the AXI address.

Table 741: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 3 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x934

Provides bits 63:32 of the AXI address.

Table 742: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x938

Provides bits 31:0 of the AXI address.

Table 743: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x93c

Provides bits 63:32 of the AXI address.

Table 744: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 4 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x940

Provides bits 31:0 of the AXI address.

Table 745: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 4 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x944

Provides bits 63:32 of the AXI address.

Table 746: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 4 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x948

Provides bits 31:0 of the AXI address.

Table 747: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 4 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x94c

Provides bits 63:32 of the AXI address.

Table 748: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 4 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x950

Provides bits 31:0 of the AXI address.

Table 749: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 4 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x954

Provides bits 63:32 of the AXI address.

Table 750: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 4 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x958

Provides bits 31:0 of the AXI address.

Table 751: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 4 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x95c

Provides bits 63:32 of the AXI address.

Table 752: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 4 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x960

Provides bits 31:0 of the AXI address.

Table 753: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 4 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x964

Provides bits 63:32 of the AXI address.

Table 754: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 4 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x968

Provides bits 31:0 of the AXI address.

Table 755: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 4 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x96c

Provides bits 63:32 of the AXI address.

Table 756: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 4 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x970

Provides bits 31:0 of the AXI address.

Table 757: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 4 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x974

Provides bits 63:32 of the AXI address.

Table 758: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x978

Provides bits 31:0 of the AXI address.

Table 759: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x97c

Provides bits 63:32 of the AXI address.

Table 760: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 5 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x980

Provides bits 31:0 of the AXI address.

Table 761: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 5 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x984

Provides bits 63:32 of the AXI address.

Table 762: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 5 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x988

Provides bits 31:0 of the AXI address.

Table 763: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 5 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x98c

Provides bits 63:32 of the AXI address.

Table 764: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 5 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x990

Provides bits 31:0 of the AXI address.

Table 765: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 5 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x994

Provides bits 63:32 of the AXI address.

Table 766: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 5 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x998

Provides bits 31:0 of the AXI address.

Table 767: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 5 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x99c

Provides bits 63:32 of the AXI address.

Table 768: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 5 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x9a0

Provides bits 31:0 of the AXI address.

Table 769: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 5 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x9a4

Provides bits 63:32 of the AXI address.

Table 770: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 5 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x9a8

Provides bits 31:0 of the AXI address.

Table 771: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 5 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x9ac

Provides bits 63:32 of the AXI address.

Table 772: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 5 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x9b0

Provides bits 31:0 of the AXI address.

Table 773: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 5 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x9b4

Provides bits 63:32 of the AXI address.

Table 774: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x9b8

Provides bits 31:0 of the AXI address.

Table 775: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x9bc

Provides bits 63:32 of the AXI address.

Table 776: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 6 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x9c0

Provides bits 31:0 of the AXI address.

Table 777: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 6 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x9c4

Provides bits 63:32 of the AXI address.

Table 778: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 6 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x9c8

Provides bits 31:0 of the AXI address.

Table 779: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 6 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x9cc

Provides bits 63:32 of the AXI address.

Table 780: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 6 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x9d0

Provides bits 31:0 of the AXI address.

Table 781: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 6 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x9d4

Provides bits 63:32 of the AXI address.

Table 782: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 6 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x9d8

Provides bits 31:0 of the AXI address.

Table 783: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 6 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x9dc

Provides bits 63:32 of the AXI address.

Table 784: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 6 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x9e0

Provides bits 31:0 of the AXI address.

Table 785: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 6 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x9e4

Provides bits 63:32 of the AXI address.

Table 786: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 6 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x9e8

Provides bits 31:0 of the AXI address.

Table 787: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 6 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x9ec

Provides bits 63:32 of the AXI address.

Table 788: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 6 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x9f0

Provides bits 31:0 of the AXI address.

Table 789: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 6 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x9f4

Provides bits 63:32 of the AXI address.

Table 790: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x9f8

Provides bits 31:0 of the AXI address.

Table 791: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x9fc

Provides bits 63:32 of the AXI address.

Table 792: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 7 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa00

Provides bits 31:0 of the AXI address.

Table 793: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 7 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa04

Provides bits 63:32 of the AXI address.

Table 794: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 7 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa08

Provides bits 31:0 of the AXI address.

Table 795: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 7 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa0c

Provides bits 63:32 of the AXI address.

Table 796: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 7 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa10

Provides bits 31:0 of the AXI address.

Table 797: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 7 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa14

Provides bits 63:32 of the AXI address.

Table 798: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 7 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa18

Provides bits 31:0 of the AXI address.

Table 799: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 7 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa1c

Provides bits 63:32 of the AXI address.

Table 800: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 7 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa20

Provides bits 31:0 of the AXI address.

Table 801: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 7 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa24

Provides bits 63:32 of the AXI address.

Table 802: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 7 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa28

Provides bits 31:0 of the AXI address.

Table 803: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 7 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa2c

Provides bits 63:32 of the AXI address.

Table 804: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 7 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa30

Provides bits 31:0 of the AXI address.

Table 805: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 7 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa34

Provides bits 63:32 of the AXI address.

Table 806: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xa38

Provides bits 31:0 of the AXI address.

Table 807: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xa3c

Provides bits 63:32 of the AXI address.

Table 808: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 8 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa40

Provides bits 31:0 of the AXI address.

Table 809: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 8 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa44

Provides bits 63:32 of the AXI address.

Table 810: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 8 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa48

Provides bits 31:0 of the AXI address.

Table 811: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 8 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa4c

Provides bits 63:32 of the AXI address.

Table 812: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 8 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa50

Provides bits 31:0 of the AXI address.

Table 813: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 8 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa54

Provides bits 63:32 of the AXI address.

Table 814: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 8 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa58

Provides bits 31:0 of the AXI address.

Table 815: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 8 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa5c

Provides bits 63:32 of the AXI address.

Table 816: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 8 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa60

Provides bits 31:0 of the AXI address.

Table 817: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 8 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa64

Provides bits 63:32 of the AXI address.

Table 818: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 8 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa68

Provides bits 31:0 of the AXI address.

Table 819: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 8 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa6c

Provides bits 63:32 of the AXI address.

Table 820: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 8 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa70

Provides bits 31:0 of the AXI address.

Table 821: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 8 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa74

Provides bits 63:32 of the AXI address.

Table 822: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xa78

Provides bits 31:0 of the AXI address.

Table 823: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xa7c

Provides bits 63:32 of the AXI address.

Table 824: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 9 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa80

Provides bits 31:0 of the AXI address.

Table 825: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 9 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa84

Provides bits 63:32 of the AXI address.

Table 826: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 9 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa88

Provides bits 31:0 of the AXI address.

Table 827: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 9 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa8c

Provides bits 63:32 of the AXI address.

Table 828: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 9 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa90

Provides bits 31:0 of the AXI address.

Table 829: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 9 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa94

Provides bits 63:32 of the AXI address.

Table 830: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 9 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xa98

Provides bits 31:0 of the AXI address.

Table 831: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 9 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xa9c

Provides bits 63:32 of the AXI address.

Table 832: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 9 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xaa0

Provides bits 31:0 of the AXI address.

Table 833: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 9 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xaa4

Provides bits 63:32 of the AXI address.

Table 834: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 9 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xaa8

Provides bits 31:0 of the AXI address.

Table 835: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 9 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xaac

Provides bits 63:32 of the AXI address.

Table 836: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 9 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xab0

Provides bits 31:0 of the AXI address.

Table 837: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 9 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xab4

Provides bits 63:32 of the AXI address.

Table 838: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xab8

Provides bits 31:0 of the AXI address.

Table 839: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xabc

Provides bits 63:32 of the AXI address.

Table 840: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 10 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xac0

Provides bits 31:0 of the AXI address.

Table 841: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 10 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xac4

Provides bits 63:32 of the AXI address.

Table 842: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 10 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xac8

Provides bits 31:0 of the AXI address.

Table 843: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 10 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xacc

Provides bits 63:32 of the AXI address.

Table 844: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 10 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xad0

Provides bits 31:0 of the AXI address.

Table 845: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 10 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xad4

Provides bits 63:32 of the AXI address.

Table 846: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 10 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xad8

Provides bits 31:0 of the AXI address.

Table 847: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 10 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xadc

Provides bits 63:32 of the AXI address.

Table 848: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 10 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xae0

Provides bits 31:0 of the AXI address.

Table 849: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 10 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xae4

Provides bits 63:32 of the AXI address.

Table 850: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 10 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xae8

Provides bits 31:0 of the AXI address.

Table 851: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 10 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xaec

Provides bits 63:32 of the AXI address.

Table 852: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 10 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xaf0

Provides bits 31:0 of the AXI address.

Table 853: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 10 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xaf4

Provides bits 63:32 of the AXI address.

Table 854: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xaf8

Provides bits 31:0 of the AXI address.

Table 855: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xafc

Provides bits 63:32 of the AXI address.

Table 856: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 11 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb00

Provides bits 31:0 of the AXI address.

Table 857: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 11 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb04

Provides bits 63:32 of the AXI address.

Table 858: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 11 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb08

Provides bits 31:0 of the AXI address.

Table 859: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 11 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb0c

Provides bits 63:32 of the AXI address.

Table 860: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 11 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb10

Provides bits 31:0 of the AXI address.

Table 861: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 11 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb14

Provides bits 63:32 of the AXI address.

Table 862: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 11 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb18

Provides bits 31:0 of the AXI address.

Table 863: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 11 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb1c

Provides bits 63:32 of the AXI address.

Table 864: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 11 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb20

Provides bits 31:0 of the AXI address.

Table 865: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 11 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb24

Provides bits 63:32 of the AXI address.

Table 866: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 11 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb28

Provides bits 31:0 of the AXI address.

Table 867: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 11 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb2c

Provides bits 63:32 of the AXI address.

Table 868: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 11 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb30

Provides bits 31:0 of the AXI address.

Table 869: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 11 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb34

Provides bits 63:32 of the AXI address.

Table 870: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xb38

Provides bits 31:0 of the AXI address.

Table 871: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xb3c

Provides bits 63:32 of the AXI address.

Table 872: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 12 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb40

Provides bits 31:0 of the AXI address.

Table 873: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 12 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb44

Provides bits 63:32 of the AXI address.

Table 874: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 12 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb48

Provides bits 31:0 of the AXI address.

Table 875: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 12 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb4c

Provides bits 63:32 of the AXI address.

Table 876: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 12 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb50

Provides bits 31:0 of the AXI address.

Table 877: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 12 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb54

Provides bits 63:32 of the AXI address.

Table 878: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 12 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb58

Provides bits 31:0 of the AXI address.

Table 879: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 12 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb5c

Provides bits 63:32 of the AXI address.

Table 880: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 12 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb60

Provides bits 31:0 of the AXI address.

Table 881: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 12 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb64

Provides bits 63:32 of the AXI address.

Table 882: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 12 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb68

Provides bits 31:0 of the AXI address.

Table 883: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 12 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb6c

Provides bits 63:32 of the AXI address.

Table 884: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 12 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb70

Provides bits 31:0 of the AXI address.

Table 885: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 12 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb74

Provides bits 63:32 of the AXI address.

Table 886: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xb78

Provides bits 31:0 of the AXI address.

Table 887: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xb7c

Provides bits 63:32 of the AXI address.

Table 888: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 13 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb80

Provides bits 31:0 of the AXI address.

Table 889: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 13 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb84

Provides bits 63:32 of the AXI address.

Table 890: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 13 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb88

Provides bits 31:0 of the AXI address.

Table 891: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 13 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb8c

Provides bits 63:32 of the AXI address.

Table 892: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 13 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb90

Provides bits 31:0 of the AXI address.

Table 893: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 13 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb94

Provides bits 63:32 of the AXI address.

Table 894: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 13 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xb98

Provides bits 31:0 of the AXI address.

Table 895: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 13 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xb9c

Provides bits 63:32 of the AXI address.

Table 896: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 13 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xba0

Provides bits 31:0 of the AXI address.

Table 897: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 13 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xba4

Provides bits 63:32 of the AXI address.

Table 898: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 13 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xba8

Provides bits 31:0 of the AXI address.

Table 899: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 13 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xbac

Provides bits 63:32 of the AXI address.

Table 900: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 13 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xbb0

Provides bits 31:0 of the AXI address.

Table 901: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 13 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xbb4

Provides bits 63:32 of the AXI address.

Table 902: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xbb8

Provides bits 31:0 of the AXI address.

Table 903: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xbbc

Provides bits 63:32 of the AXI address.

Table 904: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 14 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xbc0

Provides bits 31:0 of the AXI address.

Table 905: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 14 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xbc4

Provides bits 63:32 of the AXI address.

Table 906: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 14 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xbc8

Provides bits 31:0 of the AXI address.

Table 907: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 14 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xbcc

Provides bits 63:32 of the AXI address.

Table 908: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 14 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xbd0

Provides bits 31:0 of the AXI address.

Table 909: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 14 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xbd4

Provides bits 63:32 of the AXI address.

Table 910: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 14 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xbd8

Provides bits 31:0 of the AXI address.

Table 911: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 14 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xbdc

Provides bits 63:32 of the AXI address.

Table 912: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 14 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xbe0

Provides bits 31:0 of the AXI address.

Table 913: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 14 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xbe4

Provides bits 63:32 of the AXI address.

Table 914: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 14 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xbe8

Provides bits 31:0 of the AXI address.

Table 915: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 14 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xbec

Provides bits 63:32 of the AXI address.

Table 916: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 14 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xbf0

Provides bits 31:0 of the AXI address.

Table 917: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 14 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xbf4

Provides bits 63:32 of the AXI address.

Table 918: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xbf8

Provides bits 31:0 of the AXI address.

Table 919: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xbfc

Provides bits 63:32 of the AXI address.

Table 920: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 15 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc00

Provides bits 31:0 of the AXI address.

Table 921: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 15 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc04

Provides bits 63:32 of the AXI address.

Table 922: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 15 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc08

Provides bits 31:0 of the AXI address.

Table 923: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 15 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc0c

Provides bits 63:32 of the AXI address.

Table 924: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 15 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc10

Provides bits 31:0 of the AXI address.

Table 925: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 15 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc14

Provides bits 63:32 of the AXI address.

Table 926: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 15 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc18

Provides bits 31:0 of the AXI address.

Table 927: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 15 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc1c

Provides bits 63:32 of the AXI address.

Table 928: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 15 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc20

Provides bits 31:0 of the AXI address.

Table 929: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 15 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc24

Provides bits 63:32 of the AXI address.

Table 930: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 15 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc28

Provides bits 31:0 of the AXI address.

Table 931: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 15 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc2c

Provides bits 63:32 of the AXI address.

Table 932: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 15 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc30

Provides bits 31:0 of the AXI address.

Table 933: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 15 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc34

Provides bits 63:32 of the AXI address.

Table 934: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xc38

Provides bits 31:0 of the AXI address.

Table 935: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xc3c

Provides bits 63:32 of the AXI address.

Table 936: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 16 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc40

Provides bits 31:0 of the AXI address.

Table 937: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 16 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc44

Provides bits 63:32 of the AXI address.

Table 938: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 16 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc48

Provides bits 31:0 of the AXI address.

Table 939: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 16 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc4c

Provides bits 63:32 of the AXI address.

Table 940: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 16 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc50

Provides bits 31:0 of the AXI address.

Table 941: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 16 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc54

Provides bits 63:32 of the AXI address.

Table 942: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 16 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc58

Provides bits 31:0 of the AXI address.

Table 943: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 16 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc5c

Provides bits 63:32 of the AXI address.

Table 944: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 16 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc60

Provides bits 31:0 of the AXI address.

Table 945: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 16 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc64

Provides bits 63:32 of the AXI address.

Table 946: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 16 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc68

Provides bits 31:0 of the AXI address.

Table 947: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 16 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc6c

Provides bits 63:32 of the AXI address.

Table 948: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 16 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc70

Provides bits 31:0 of the AXI address.

Table 949: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 16 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc74

Provides bits 63:32 of the AXI address.

Table 950: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xc78

Provides bits 31:0 of the AXI address.

Table 951: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xc7c

Provides bits 63:32 of the AXI address.

Table 952: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 17 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc80

Provides bits 31:0 of the AXI address.

Table 953: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 17 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc84

Provides bits 63:32 of the AXI address.

Table 954: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 17 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc88

Provides bits 31:0 of the AXI address.

Table 955: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 17 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc8c

Provides bits 63:32 of the AXI address.

Table 956: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 17 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc90

Provides bits 31:0 of the AXI address.

Table 957: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 17 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc94

Provides bits 63:32 of the AXI address.

Table 958: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 17 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xc98

Provides bits 31:0 of the AXI address.

Table 959: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 17 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xc9c

Provides bits 63:32 of the AXI address.

Table 960: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 17 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xca0

Provides bits 31:0 of the AXI address.

Table 961: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 17 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xca4

Provides bits 63:32 of the AXI address.

Table 962: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 17 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xca8

Provides bits 31:0 of the AXI address.

Table 963: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 17 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xcac

Provides bits 63:32 of the AXI address.

Table 964: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 17 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xcb0

Provides bits 31:0 of the AXI address.

Table 965: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 17 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xcb4

Provides bits 63:32 of the AXI address.

Table 966: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xcb8

Provides bits 31:0 of the AXI address.

Table 967: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xcbc

Provides bits 63:32 of the AXI address.

Table 968: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 18 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xcc0

Provides bits 31:0 of the AXI address.

Table 969: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 18 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xcc4

Provides bits 63:32 of the AXI address.

Table 970: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 18 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xcc8

Provides bits 31:0 of the AXI address.

Table 971: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 18 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xccc

Provides bits 63:32 of the AXI address.

Table 972: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 18 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xcd0

Provides bits 31:0 of the AXI address.

Table 973: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 18 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xcd4

Provides bits 63:32 of the AXI address.

Table 974: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 18 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xcd8

Provides bits 31:0 of the AXI address.

Table 975: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 18 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xcdc

Provides bits 63:32 of the AXI address.

Table 976: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 18 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xce0

Provides bits 31:0 of the AXI address.

Table 977: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 18 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xce4

Provides bits 63:32 of the AXI address.

Table 978: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 18 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xce8

Provides bits 31:0 of the AXI address.

Table 979: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 18 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xcec

Provides bits 63:32 of the AXI address.

Table 980: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 18 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xcf0

Provides bits 31:0 of the AXI address.

Table 981: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 18 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xcf4

Provides bits 63:32 of the AXI address.

Table 982: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xcf8

Provides bits 31:0 of the AXI address.

Table 983: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xcfc

Provides bits 63:32 of the AXI address.

Table 984: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 19 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd00

Provides bits 31:0 of the AXI address.

Table 985: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 19 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd04

Provides bits 63:32 of the AXI address.

Table 986: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 19 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd08

Provides bits 31:0 of the AXI address.

Table 987: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 19 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd0c

Provides bits 63:32 of the AXI address.

Table 988: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 19 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd10

Provides bits 31:0 of the AXI address.

Table 989: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 19 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd14

Provides bits 63:32 of the AXI address.

Table 990: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 19 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd18

Provides bits 31:0 of the AXI address.

Table 991: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 19 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd1c

Provides bits 63:32 of the AXI address.

Table 992: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 19 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd20

Provides bits 31:0 of the AXI address.

Table 993: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 19 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd24

Provides bits 63:32 of the AXI address.

Table 994: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 19 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd28

Provides bits 31:0 of the AXI address.

Table 995: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 19 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd2c

Provides bits 63:32 of the AXI address.

Table 996: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 19 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd30

Provides bits 31:0 of the AXI address.

Table 997: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 19 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd34

Provides bits 63:32 of the AXI address.

Table 998: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xd38

Provides bits 31:0 of the AXI address.

Table 999: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xd3c

Provides bits 63:32 of the AXI address.

Table 1000: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 20 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd40

Provides bits 31:0 of the AXI address.

Table 1001: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 20 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd44

Provides bits 63:32 of the AXI address.

Table 1002: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 20 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd48

Provides bits 31:0 of the AXI address.

Table 1003: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 20 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd4c

Provides bits 63:32 of the AXI address.

Table 1004: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 20 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd50

Provides bits 31:0 of the AXI address.

Table 1005: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 20 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd54

Provides bits 63:32 of the AXI address.

Table 1006: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 20 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd58

Provides bits 31:0 of the AXI address.

Table 1007: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 20 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd5c

Provides bits 63:32 of the AXI address.

Table 1008: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 20 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd60

Provides bits 31:0 of the AXI address.

Table 1009: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 20 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd64

Provides bits 63:32 of the AXI address.

Table 1010: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 20 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd68

Provides bits 31:0 of the AXI address.

Table 1011: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 20 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd6c

Provides bits 63:32 of the AXI address.

Table 1012: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 20 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd70

Provides bits 31:0 of the AXI address.

Table 1013: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 20 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd74

Provides bits 63:32 of the AXI address.

Table 1014: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xd78

Provides bits 31:0 of the AXI address.

Table 1015: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xd7c

Provides bits 63:32 of the AXI address.

Table 1016: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 21 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd80

Provides bits 31:0 of the AXI address.

Table 1017: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 21 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd84

Provides bits 63:32 of the AXI address.

Table 1018: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 21 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd88

Provides bits 31:0 of the AXI address.

Table 1019: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 21 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd8c

Provides bits 63:32 of the AXI address.

Table 1020: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 21 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd90

Provides bits 31:0 of the AXI address.

Table 1021: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 21 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd94

Provides bits 63:32 of the AXI address.

Table 1022: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 21 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xd98

Provides bits 31:0 of the AXI address.

Table 1023: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 21 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xd9c

Provides bits 63:32 of the AXI address.

Table 1024: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 21 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xda0

Provides bits 31:0 of the AXI address.

Table 1025: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 21 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xda4

Provides bits 63:32 of the AXI address.

Table 1026: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 21 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xda8

Provides bits 31:0 of the AXI address.

Table 1027: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 21 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xdac

Provides bits 63:32 of the AXI address.

Table 1028: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 21 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xdb0

Provides bits 31:0 of the AXI address.

Table 1029: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 21 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xdb4

Provides bits 63:32 of the AXI address.

Table 1030: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xdb8

Provides bits 31:0 of the AXI address.

Table 1031: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xdbc

Provides bits 63:32 of the AXI address.

Table 1032: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 22 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xdc0

Provides bits 31:0 of the AXI address.

Table 1033: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 22 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xdc4

Provides bits 63:32 of the AXI address.

Table 1034: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 22 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xdc8

Provides bits 31:0 of the AXI address.

Table 1035: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 22 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xdcc

Provides bits 63:32 of the AXI address.

Table 1036: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 22 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xdd0

Provides bits 31:0 of the AXI address.

Table 1037: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 22 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xdd4

Provides bits 63:32 of the AXI address.

Table 1038: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 22 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xdd8

Provides bits 31:0 of the AXI address.

Table 1039: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 22 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xddc

Provides bits 63:32 of the AXI address.

Table 1040: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 22 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xde0

Provides bits 31:0 of the AXI address.

Table 1041: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 22 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xde4

Provides bits 63:32 of the AXI address.

Table 1042: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 22 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xde8

Provides bits 31:0 of the AXI address.

Table 1043: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 22 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xdec

Provides bits 63:32 of the AXI address.

Table 1044: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 22 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xdf0

Provides bits 31:0 of the AXI address.

Table 1045: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 22 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xdf4

Provides bits 63:32 of the AXI address.

Table 1046: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xdf8

Provides bits 31:0 of the AXI address.

Table 1047: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xdfc

Provides bits 63:32 of the AXI address.

Table 1048: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 23 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe00

Provides bits 31:0 of the AXI address.

Table 1049: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 23 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe04

Provides bits 63:32 of the AXI address.

Table 1050: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 23 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe08

Provides bits 31:0 of the AXI address.

Table 1051: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 23 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe0c

Provides bits 63:32 of the AXI address.

Table 1052: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 23 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe10

Provides bits 31:0 of the AXI address.

Table 1053: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 23 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe14

Provides bits 63:32 of the AXI address.

Table 1054: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 23 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe18

Provides bits 31:0 of the AXI address.

Table 1055: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 23 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe1c

Provides bits 63:32 of the AXI address.

Table 1056: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 23 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe20

Provides bits 31:0 of the AXI address.

Table 1057: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 23 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe24

Provides bits 63:32 of the AXI address.

Table 1058: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 23 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe28

Provides bits 31:0 of the AXI address.

Table 1059: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 23 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe2c

Provides bits 63:32 of the AXI address.

Table 1060: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 23 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe30

Provides bits 31:0 of the AXI address.

Table 1061: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 23 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe34

Provides bits 63:32 of the AXI address.

Table 1062: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xe38

Provides bits 31:0 of the AXI address.

Table 1063: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xe3c

Provides bits 63:32 of the AXI address.

Table 1064: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 24 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe40

Provides bits 31:0 of the AXI address.

Table 1065: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 24 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe44

Provides bits 63:32 of the AXI address.

Table 1066: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 24 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe48

Provides bits 31:0 of the AXI address.

Table 1067: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 24 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe4c

Provides bits 63:32 of the AXI address.

Table 1068: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 24 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe50

Provides bits 31:0 of the AXI address.

Table 1069: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 24 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe54

Provides bits 63:32 of the AXI address.

Table 1070: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 24 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe58

Provides bits 31:0 of the AXI address.

Table 1071: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 24 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe5c

Provides bits 63:32 of the AXI address.

Table 1072: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 24 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe60

Provides bits 31:0 of the AXI address.

Table 1073: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 24 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe64

Provides bits 63:32 of the AXI address.

Table 1074: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 24 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe68

Provides bits 31:0 of the AXI address.

Table 1075: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 24 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe6c

Provides bits 63:32 of the AXI address.

Table 1076: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 24 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe70

Provides bits 31:0 of the AXI address.

Table 1077: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 24 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe74

Provides bits 63:32 of the AXI address.

Table 1078: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xe78

Provides bits 31:0 of the AXI address.

Table 1079: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xe7c

Provides bits 63:32 of the AXI address.

Table 1080: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 25 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe80

Provides bits 31:0 of the AXI address.

Table 1081: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 25 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe84

Provides bits 63:32 of the AXI address.

Table 1082: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 25 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe88

Provides bits 31:0 of the AXI address.

Table 1083: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 25 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe8c

Provides bits 63:32 of the AXI address.

Table 1084: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 25 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe90

Provides bits 31:0 of the AXI address.

Table 1085: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 25 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe94

Provides bits 63:32 of the AXI address.

Table 1086: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 25 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xe98

Provides bits 31:0 of the AXI address.

Table 1087: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 25 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xe9c

Provides bits 63:32 of the AXI address.

Table 1088: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 25 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xea0

Provides bits 31:0 of the AXI address.

Table 1089: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 25 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xea4

Provides bits 63:32 of the AXI address.

Table 1090: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 25 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xea8

Provides bits 31:0 of the AXI address.

Table 1091: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 25 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xeac

Provides bits 63:32 of the AXI address.

Table 1092: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 25 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xeb0

Provides bits 31:0 of the AXI address.

Table 1093: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 25 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xeb4

Provides bits 63:32 of the AXI address.

Table 1094: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xeb8

Provides bits 31:0 of the AXI address.

Table 1095: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xebc

Provides bits 63:32 of the AXI address.

Table 1096: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 26 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xec0

Provides bits 31:0 of the AXI address.

Table 1097: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 26 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xec4

Provides bits 63:32 of the AXI address.

Table 1098: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 26 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xec8

Provides bits 31:0 of the AXI address.

Table 1099: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 26 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xecc

Provides bits 63:32 of the AXI address.

Table 1100: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 26 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xed0

Provides bits 31:0 of the AXI address.

Table 1101: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 26 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xed4

Provides bits 63:32 of the AXI address.

Table 1102: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 26 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xed8

Provides bits 31:0 of the AXI address.

Table 1103: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 26 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xedc

Provides bits 63:32 of the AXI address.

Table 1104: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 26 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xee0

Provides bits 31:0 of the AXI address.

Table 1105: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 26 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xee4

Provides bits 63:32 of the AXI address.

Table 1106: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 26 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xee8

Provides bits 31:0 of the AXI address.

Table 1107: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 26 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xeec

Provides bits 63:32 of the AXI address.

Table 1108: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 26 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xef0

Provides bits 31:0 of the AXI address.

Table 1109: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 26 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xef4

Provides bits 63:32 of the AXI address.

Table 1110: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xef8

Provides bits 31:0 of the AXI address.

Table 1111: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xefc

Provides bits 63:32 of the AXI address.

Table 1112: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 27 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf00

Provides bits 31:0 of the AXI address.

Table 1113: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 27 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf04

Provides bits 63:32 of the AXI address.

Table 1114: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 27 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf08

Provides bits 31:0 of the AXI address.

Table 1115: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 27 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf0c

Provides bits 63:32 of the AXI address.

Table 1116: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 27 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf10

Provides bits 31:0 of the AXI address.

Table 1117: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 27 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf14

Provides bits 63:32 of the AXI address.

Table 1118: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 27 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf18

Provides bits 31:0 of the AXI address.

Table 1119: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 27 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf1c

Provides bits 63:32 of the AXI address.

Table 1120: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 27 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf20

Provides bits 31:0 of the AXI address.

Table 1121: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 27 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf24

Provides bits 63:32 of the AXI address.

Table 1122: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 27 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf28

Provides bits 31:0 of the AXI address.

Table 1123: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 27 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf2c

Provides bits 63:32 of the AXI address.

Table 1124: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 27 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf30

Provides bits 31:0 of the AXI address.

Table 1125: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 27 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf34

Provides bits 63:32 of the AXI address.

Table 1126: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xf38

Provides bits 31:0 of the AXI address.

Table 1127: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xf3c

Provides bits 63:32 of the AXI address.

Table 1128: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 28 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf40

Provides bits 31:0 of the AXI address.

Table 1129: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 28 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf44

Provides bits 63:32 of the AXI address.

Table 1130: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 28 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf48

Provides bits 31:0 of the AXI address.

Table 1131: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 28 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf4c

Provides bits 63:32 of the AXI address.

Table 1132: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 28 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf50

Provides bits 31:0 of the AXI address.

Table 1133: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 28 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf54

Provides bits 63:32 of the AXI address.

Table 1134: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 28 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf58

Provides bits 31:0 of the AXI address.

Table 1135: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 28 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf5c

Provides bits 63:32 of the AXI address.

Table 1136: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 28 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf60

Provides bits 31:0 of the AXI address.

Table 1137: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 28 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf64

Provides bits 63:32 of the AXI address.

Table 1138: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 28 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf68

Provides bits 31:0 of the AXI address.

Table 1139: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 28 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf6c

Provides bits 63:32 of the AXI address.

Table 1140: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 28 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf70

Provides bits 31:0 of the AXI address.

Table 1141: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 28 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf74

Provides bits 63:32 of the AXI address.

Table 1142: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xf78

Provides bits 31:0 of the AXI address.

Table 1143: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xf7c

Provides bits 63:32 of the AXI address.

Table 1144: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 29 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf80

Provides bits 31:0 of the AXI address.

Table 1145: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 29 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf84

Provides bits 63:32 of the AXI address.

Table 1146: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 29 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf88

Provides bits 31:0 of the AXI address.

Table 1147: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 29 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf8c

Provides bits 63:32 of the AXI address.

Table 1148: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 29 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf90

Provides bits 31:0 of the AXI address.

Table 1149: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 29 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf94

Provides bits 63:32 of the AXI address.

Table 1150: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 29 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xf98

Provides bits 31:0 of the AXI address.

Table 1151: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 29 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xf9c

Provides bits 63:32 of the AXI address.

Table 1152: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 29 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xfa0

Provides bits 31:0 of the AXI address.

Table 1153: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 29 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xfa4

Provides bits 63:32 of the AXI address.

Table 1154: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 29 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xfa8

Provides bits 31:0 of the AXI address.

Table 1155: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 29 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xfac

Provides bits 63:32 of the AXI address.

Table 1156: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 29 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xfb0

Provides bits 31:0 of the AXI address.

Table 1157: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 29 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xfb4

Provides bits 63:32 of the AXI address.

Table 1158: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xfb8

Provides bits 31:0 of the AXI address.

Table 1159: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xfbc

Provides bits 63:32 of the AXI address.

Table 1160: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 30 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xfc0

Provides bits 31:0 of the AXI address.

Table 1161: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 30 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xfc4

Provides bits 63:32 of the AXI address.

Table 1162: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 30 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xfc8

Provides bits 31:0 of the AXI address.

Table 1163: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 30 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xfcc

Provides bits 63:32 of the AXI address.

Table 1164: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 30 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xfd0

Provides bits 31:0 of the AXI address.

Table 1165: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 30 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xfd4

Provides bits 63:32 of the AXI address.

Table 1166: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 30 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xfd8

Provides bits 31:0 of the AXI address.

Table 1167: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 30 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xfdc

Provides bits 63:32 of the AXI address.

Table 1168: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 30 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xfe0

Provides bits 31:0 of the AXI address.

Table 1169: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 30 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xfe4

Provides bits 63:32 of the AXI address.

Table 1170: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 30 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xfe8

Provides bits 31:0 of the AXI address.

Table 1171: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 30 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xfec

Provides bits 63:32 of the AXI address.

Table 1172: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 30 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0xff0

Provides bits 31:0 of the AXI address.

Table 1173: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 30 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0xff4

Provides bits 63:32 of the AXI address.

Table 1174: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0xff8

Provides bits 31:0 of the AXI address.

Table 1175: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0xffc

Provides bits 63:32 of the AXI address.

Table 1176: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 31 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1000

Provides bits 31:0 of the AXI address.

Table 1177: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 31 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1004

Provides bits 63:32 of the AXI address.

Table 1178: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 31 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1008

Provides bits 31:0 of the AXI address.

Table 1179: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 31 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x100c

Provides bits 63:32 of the AXI address.

Table 1180: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 31 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1010

Provides bits 31:0 of the AXI address.

Table 1181: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 31 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1014

Provides bits 63:32 of the AXI address.

Table 1182: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 31 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1018

Provides bits 31:0 of the AXI address.

Table 1183: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 31 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x101c

Provides bits 63:32 of the AXI address.

Table 1184: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 31 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1020

Provides bits 31:0 of the AXI address.

Table 1185: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 31 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1024

Provides bits 63:32 of the AXI address.

Table 1186: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 31 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1028

Provides bits 31:0 of the AXI address.

Table 1187: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 31 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x102c

Provides bits 63:32 of the AXI address.

Table 1188: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 31 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1030

Provides bits 31:0 of the AXI address.

Table 1189: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 31 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1034

Provides bits 63:32 of the AXI address.

Table 1190: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1038

Provides bits 31:0 of the AXI address.

Table 1191: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x103c

Provides bits 63:32 of the AXI address.

Table 1192: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 32 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1040

Provides bits 31:0 of the AXI address.

Table 1193: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 32 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1044

Provides bits 63:32 of the AXI address.

Table 1194: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 32 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1048

Provides bits 31:0 of the AXI address.

Table 1195: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 32 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x104c

Provides bits 63:32 of the AXI address.

Table 1196: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 32 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1050

Provides bits 31:0 of the AXI address.

Table 1197: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 32 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1054

Provides bits 63:32 of the AXI address.

Table 1198: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 32 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1058

Provides bits 31:0 of the AXI address.

Table 1199: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 32 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x105c

Provides bits 63:32 of the AXI address.

Table 1200: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 32 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1060

Provides bits 31:0 of the AXI address.

Table 1201: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 32 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1064

Provides bits 63:32 of the AXI address.

Table 1202: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 32 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1068

Provides bits 31:0 of the AXI address.

Table 1203: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 32 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x106c

Provides bits 63:32 of the AXI address.

Table 1204: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 32 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1070

Provides bits 31:0 of the AXI address.

Table 1205: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 32 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1074

Provides bits 63:32 of the AXI address.

Table 1206: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1078

Provides bits 31:0 of the AXI address.

Table 1207: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x107c

Provides bits 63:32 of the AXI address.

Table 1208: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 33 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1080

Provides bits 31:0 of the AXI address.

Table 1209: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 33 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1084

Provides bits 63:32 of the AXI address.

Table 1210: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 33 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1088

Provides bits 31:0 of the AXI address.

Table 1211: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 33 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x108c

Provides bits 63:32 of the AXI address.

Table 1212: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 33 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1090

Provides bits 31:0 of the AXI address.

Table 1213: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 33 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1094

Provides bits 63:32 of the AXI address.

Table 1214: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 33 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1098

Provides bits 31:0 of the AXI address.

Table 1215: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 33 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x109c

Provides bits 63:32 of the AXI address.

Table 1216: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 33 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x10a0

Provides bits 31:0 of the AXI address.

Table 1217: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 33 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x10a4

Provides bits 63:32 of the AXI address.

Table 1218: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 33 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x10a8

Provides bits 31:0 of the AXI address.

Table 1219: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 33 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x10ac

Provides bits 63:32 of the AXI address.

Table 1220: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 33 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x10b0

Provides bits 31:0 of the AXI address.

Table 1221: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 33 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x10b4

Provides bits 63:32 of the AXI address.

Table 1222: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x10b8

Provides bits 31:0 of the AXI address.

Table 1223: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x10bc

Provides bits 63:32 of the AXI address.

Table 1224: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 34 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x10c0

Provides bits 31:0 of the AXI address.

Table 1225: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 34 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x10c4

Provides bits 63:32 of the AXI address.

Table 1226: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 34 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x10c8

Provides bits 31:0 of the AXI address.

Table 1227: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 34 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x10cc

Provides bits 63:32 of the AXI address.

Table 1228: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 34 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x10d0

Provides bits 31:0 of the AXI address.

Table 1229: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 34 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x10d4

Provides bits 63:32 of the AXI address.

Table 1230: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 34 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x10d8

Provides bits 31:0 of the AXI address.

Table 1231: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 34 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x10dc

Provides bits 63:32 of the AXI address.

Table 1232: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 34 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x10e0

Provides bits 31:0 of the AXI address.

Table 1233: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 34 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x10e4

Provides bits 63:32 of the AXI address.

Table 1234: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 34 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x10e8

Provides bits 31:0 of the AXI address.

Table 1235: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 34 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x10ec

Provides bits 63:32 of the AXI address.

Table 1236: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 34 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x10f0

Provides bits 31:0 of the AXI address.

Table 1237: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 34 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x10f4

Provides bits 63:32 of the AXI address.

Table 1238: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x10f8

Provides bits 31:0 of the AXI address.

Table 1239: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x10fc

Provides bits 63:32 of the AXI address.

Table 1240: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 35 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1100

Provides bits 31:0 of the AXI address.

Table 1241: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 35 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1104

Provides bits 63:32 of the AXI address.

Table 1242: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 35 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1108

Provides bits 31:0 of the AXI address.

Table 1243: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 35 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x110c

Provides bits 63:32 of the AXI address.

Table 1244: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 35 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1110

Provides bits 31:0 of the AXI address.

Table 1245: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 35 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1114

Provides bits 63:32 of the AXI address.

Table 1246: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 35 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1118

Provides bits 31:0 of the AXI address.

Table 1247: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 35 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x111c

Provides bits 63:32 of the AXI address.

Table 1248: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 35 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1120

Provides bits 31:0 of the AXI address.

Table 1249: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 35 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1124

Provides bits 63:32 of the AXI address.

Table 1250: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 35 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1128

Provides bits 31:0 of the AXI address.

Table 1251: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 35 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x112c

Provides bits 63:32 of the AXI address.

Table 1252: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 35 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1130

Provides bits 31:0 of the AXI address.

Table 1253: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 35 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1134

Provides bits 63:32 of the AXI address.

Table 1254: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1138

Provides bits 31:0 of the AXI address.

Table 1255: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x113c

Provides bits 63:32 of the AXI address.

Table 1256: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 36 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1140

Provides bits 31:0 of the AXI address.

Table 1257: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 36 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1144

Provides bits 63:32 of the AXI address.

Table 1258: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 36 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1148

Provides bits 31:0 of the AXI address.

Table 1259: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 36 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x114c

Provides bits 63:32 of the AXI address.

Table 1260: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 36 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1150

Provides bits 31:0 of the AXI address.

Table 1261: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 36 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1154

Provides bits 63:32 of the AXI address.

Table 1262: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 36 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1158

Provides bits 31:0 of the AXI address.

Table 1263: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 36 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x115c

Provides bits 63:32 of the AXI address.

Table 1264: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 36 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1160

Provides bits 31:0 of the AXI address.

Table 1265: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 36 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1164

Provides bits 63:32 of the AXI address.

Table 1266: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 36 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1168

Provides bits 31:0 of the AXI address.

Table 1267: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 36 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x116c

Provides bits 63:32 of the AXI address.

Table 1268: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 36 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1170

Provides bits 31:0 of the AXI address.

Table 1269: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 36 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1174

Provides bits 63:32 of the AXI address.

Table 1270: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1178

Provides bits 31:0 of the AXI address.

Table 1271: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x117c

Provides bits 63:32 of the AXI address.

Table 1272: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 37 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1180

Provides bits 31:0 of the AXI address.

Table 1273: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 37 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1184

Provides bits 63:32 of the AXI address.

Table 1274: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 37 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1188

Provides bits 31:0 of the AXI address.

Table 1275: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 37 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x118c

Provides bits 63:32 of the AXI address.

Table 1276: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 37 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1190

Provides bits 31:0 of the AXI address.

Table 1277: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 37 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1194

Provides bits 63:32 of the AXI address.

Table 1278: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 37 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1198

Provides bits 31:0 of the AXI address.

Table 1279: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 37 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x119c

Provides bits 63:32 of the AXI address.

Table 1280: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 37 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x11a0

Provides bits 31:0 of the AXI address.

Table 1281: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 37 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x11a4

Provides bits 63:32 of the AXI address.

Table 1282: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 37 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x11a8

Provides bits 31:0 of the AXI address.

Table 1283: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 37 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x11ac

Provides bits 63:32 of the AXI address.

Table 1284: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 37 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x11b0

Provides bits 31:0 of the AXI address.

Table 1285: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 37 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x11b4

Provides bits 63:32 of the AXI address.

Table 1286: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x11b8

Provides bits 31:0 of the AXI address.

Table 1287: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x11bc

Provides bits 63:32 of the AXI address.

Table 1288: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 38 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x11c0

Provides bits 31:0 of the AXI address.

Table 1289: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 38 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x11c4

Provides bits 63:32 of the AXI address.

Table 1290: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 38 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x11c8

Provides bits 31:0 of the AXI address.

Table 1291: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 38 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x11cc

Provides bits 63:32 of the AXI address.

Table 1292: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 38 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x11d0

Provides bits 31:0 of the AXI address.

Table 1293: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 38 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x11d4

Provides bits 63:32 of the AXI address.

Table 1294: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 38 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x11d8

Provides bits 31:0 of the AXI address.

Table 1295: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 38 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x11dc

Provides bits 63:32 of the AXI address.

Table 1296: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 38 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x11e0

Provides bits 31:0 of the AXI address.

Table 1297: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 38 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x11e4

Provides bits 63:32 of the AXI address.

Table 1298: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 38 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x11e8

Provides bits 31:0 of the AXI address.

Table 1299: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 38 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x11ec

Provides bits 63:32 of the AXI address.

Table 1300: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 38 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x11f0

Provides bits 31:0 of the AXI address.

Table 1301: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 38 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x11f4

Provides bits 63:32 of the AXI address.

Table 1302: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x11f8

Provides bits 31:0 of the AXI address.

Table 1303: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x11fc

Provides bits 63:32 of the AXI address.

Table 1304: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 39 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1200

Provides bits 31:0 of the AXI address.

Table 1305: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 39 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1204

Provides bits 63:32 of the AXI address.

Table 1306: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 39 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1208

Provides bits 31:0 of the AXI address.

Table 1307: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 39 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x120c

Provides bits 63:32 of the AXI address.

Table 1308: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 39 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1210

Provides bits 31:0 of the AXI address.

Table 1309: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 39 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1214

Provides bits 63:32 of the AXI address.

Table 1310: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 39 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1218

Provides bits 31:0 of the AXI address.

Table 1311: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 39 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x121c

Provides bits 63:32 of the AXI address.

Table 1312: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 39 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1220

Provides bits 31:0 of the AXI address.

Table 1313: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 39 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1224

Provides bits 63:32 of the AXI address.

Table 1314: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 39 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1228

Provides bits 31:0 of the AXI address.

Table 1315: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 39 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x122c

Provides bits 63:32 of the AXI address.

Table 1316: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 39 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1230

Provides bits 31:0 of the AXI address.

Table 1317: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 39 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1234

Provides bits 63:32 of the AXI address.

Table 1318: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1238

Provides bits 31:0 of the AXI address.

Table 1319: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x123c

Provides bits 63:32 of the AXI address.

Table 1320: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 40 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1240

Provides bits 31:0 of the AXI address.

Table 1321: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 40 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1244

Provides bits 63:32 of the AXI address.

Table 1322: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 40 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1248

Provides bits 31:0 of the AXI address.

Table 1323: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 40 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x124c

Provides bits 63:32 of the AXI address.

Table 1324: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 40 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1250

Provides bits 31:0 of the AXI address.

Table 1325: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 40 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1254

Provides bits 63:32 of the AXI address.

Table 1326: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 40 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1258

Provides bits 31:0 of the AXI address.

Table 1327: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 40 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x125c

Provides bits 63:32 of the AXI address.

Table 1328: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 40 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1260

Provides bits 31:0 of the AXI address.

Table 1329: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 40 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1264

Provides bits 63:32 of the AXI address.

Table 1330: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 40 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1268

Provides bits 31:0 of the AXI address.

Table 1331: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 40 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x126c

Provides bits 63:32 of the AXI address.

Table 1332: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 40 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1270

Provides bits 31:0 of the AXI address.

Table 1333: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 40 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1274

Provides bits 63:32 of the AXI address.

Table 1334: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1278

Provides bits 31:0 of the AXI address.

Table 1335: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x127c

Provides bits 63:32 of the AXI address.

Table 1336: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 41 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1280

Provides bits 31:0 of the AXI address.

Table 1337: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 41 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1284

Provides bits 63:32 of the AXI address.

Table 1338: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 41 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1288

Provides bits 31:0 of the AXI address.

Table 1339: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 41 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x128c

Provides bits 63:32 of the AXI address.

Table 1340: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 41 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1290

Provides bits 31:0 of the AXI address.

Table 1341: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 41 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1294

Provides bits 63:32 of the AXI address.

Table 1342: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 41 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1298

Provides bits 31:0 of the AXI address.

Table 1343: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 41 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x129c

Provides bits 63:32 of the AXI address.

Table 1344: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 41 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x12a0

Provides bits 31:0 of the AXI address.

Table 1345: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 41 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x12a4

Provides bits 63:32 of the AXI address.

Table 1346: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 41 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x12a8

Provides bits 31:0 of the AXI address.

Table 1347: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 41 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x12ac

Provides bits 63:32 of the AXI address.

Table 1348: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 41 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x12b0

Provides bits 31:0 of the AXI address.

Table 1349: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 41 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x12b4

Provides bits 63:32 of the AXI address.

Table 1350: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x12b8

Provides bits 31:0 of the AXI address.

Table 1351: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x12bc

Provides bits 63:32 of the AXI address..

Table 1352: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 42 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x12c0

Provides bits 31:0 of the AXI address.

Table 1353: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 42 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x12c4

Provides bits 63:32 of the AXI address.

Table 1354: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 42 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x12c8

Provides bits 31:0 of the AXI address.

Table 1355: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 42 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x12cc

Provides bits 63:32 of the AXI address.

Table 1356: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 42 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x12d0

Provides bits 31:0 of the AXI address.

Table 1357: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 42 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x12d4

Provides bits 63:32 of the AXI address.

Table 1358: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 42 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x12d8

Provides bits 31:0 of the AXI address.

Table 1359: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 42 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x12dc

Provides bits 63:32 of the AXI address.

Table 1360: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 42 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x12e0

Provides bits 31:0 of the AXI address.

Table 1361: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 42 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x12e4

Provides bits 63:32 of the AXI address.

Table 1362: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 42 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x12e8

Provides bits 31:0 of the AXI address.

Table 1363: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 42 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x12ec

Provides bits 63:32 of the AXI address.

Table 1364: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 42 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x12f0

Provides bits 31:0 of the AXI address.

Table 1365: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 42 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x12f4

Provides bits 63:32 of the AXI address.

Table 1366: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x12f8

Provides bits 31:0 of the AXI address.

Table 1367: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x12fc

Provides bits 63:32 of the AXI address.

Table 1368: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 43 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1300

Provides bits 31:0 of the AXI address.

Table 1369: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 43 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1304

Provides bits 63:32 of the AXI address.

Table 1370: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 43 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1308

Provides bits 31:0 of the AXI address.

Table 1371: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 43 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x130c

Provides bits 63:32 of the AXI address.

Table 1372: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 43 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1310

Provides bits 31:0 of the AXI address.

Table 1373: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 43 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1314

Provides bits 63:32 of the AXI address.

Table 1374: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 43 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1318

Provides bits 31:0 of the AXI address.

Table 1375: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 43 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x131c

Provides bits 63:32 of the AXI address.

Table 1376: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 43 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1320

Provides bits 31:0 of the AXI address.

Table 1377: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 43 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1324

Provides bits 63:32 of the AXI address.

Table 1378: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 43 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1328

Provides bits 31:0 of the AXI address.

Table 1379: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 43 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x132c

Provides bits 63:32 of the AXI address.

Table 1380: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 43 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1330

Provides bits 31:0 of the AXI address.

Table 1381: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 43 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1334

Provides bits 63:32 of the AXI address.

Table 1382: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1338

Provides bits 31:0 of the AXI address.

Table 1383: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x133c

Provides bits 63:32 of the AXI address.

Table 1384: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 44 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1340

Provides bits 31:0 of the AXI address.

Table 1385: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 44 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1344

Provides bits 63:32 of the AXI address.

Table 1386: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 44 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1348

Provides bits 31:0 of the AXI address.

Table 1387: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 44 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x134c

Provides bits 63:32 of the AXI address.

Table 1388: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 44 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1350

Provides bits 31:0 of the AXI address.

Table 1389: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 44 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1354

Provides bits 63:32 of the AXI address.

Table 1390: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 44 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1358

Provides bits 31:0 of the AXI address.

Table 1391: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 44 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x135c

Provides bits 63:32 of the AXI address.

Table 1392: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 44 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1360

Provides bits 31:0 of the AXI address.

Table 1393: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 44 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1364

Provides bits 63:32 of the AXI address.

Table 1394: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 44 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1368

Provides bits 31:0 of the AXI address.

Table 1395: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 44 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x136c

Provides bits 63:32 of the AXI address.

Table 1396: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 44 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1370

Provides bits 31:0 of the AXI address.

Table 1397: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 44 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1374

Provides bits 63:32 of the AXI address.

Table 1398: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1378

Provides bits 31:0 of the AXI address.

Table 1399: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x137c

Provides bits 63:32 of the AXI address.

Table 1400: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 45 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1380

Provides bits 31:0 of the AXI address.

Table 1401: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 45 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1384

Provides bits 63:32 of the AXI address.

Table 1402: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 45 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1388

Provides bits 31:0 of the AXI address.

Table 1403: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 45 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x138c

Provides bits 63:32 of the AXI address.

Table 1404: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 45 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1390

Provides bits 31:0 of the AXI address.

Table 1405: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 45 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1394

Provides bits 63:32 of the AXI address.

Table 1406: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 45 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1398

Provides bits 31:0 of the AXI address.

Table 1407: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 45 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x139c

Provides bits 63:32 of the AXI address.

Table 1408: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 45 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x13a0

Provides bits 31:0 of the AXI address.

Table 1409: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 45 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x13a4

Provides bits 63:32 of the AXI address.

Table 1410: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 45 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x13a8

Provides bits 31:0 of the AXI address.

Table 1411: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 45 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x13ac

Provides bits 63:32 of the AXI address.

Table 1412: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 45 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x13b0

Provides bits 31:0 of the AXI address.

Table 1413: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 45 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x13b4

Provides bits 63:32 of the AXI address.

Table 1414: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x13b8

Provides bits 31:0 of the AXI address.

Table 1415: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x13bc

Provides bits 63:32 of the AXI address.

Table 1416: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 46 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x13c0

Provides bits 31:0 of the AXI address.

Table 1417: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 46 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x13c4

Provides bits 63:32 of the AXI address.

Table 1418: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 46 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x13c8

Provides bits 31:0 of the AXI address.

Table 1419: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 46 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x13cc

Provides bits 63:32 of the AXI address.

Table 1420: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 46 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x13d0

Provides bits 31:0 of the AXI address.

Table 1421: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 46 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x13d4

Provides bits 63:32 of the AXI address.

Table 1422: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 46 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x13d8

Provides bits 31:0 of the AXI address.

Table 1423: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 46 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x13dc

Provides bits 63:32 of the AXI address.

Table 1424: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 46 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x13e0

Provides bits 31:0 of the AXI address.

Table 1425: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 46 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x13e4

Provides bits 63:32 of the AXI address.

Table 1426: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 46 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x13e8

Provides bits 31:0 of the AXI address.

Table 1427: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 46 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x13ec

Provides bits 63:32 of the AXI address.

Table 1428: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 46 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x13f0

Provides bits 31:0 of the AXI address.

Table 1429: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 46 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x13f4

Provides bits 63:32 of the AXI address.

Table 1430: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x13f8

Provides bits 31:0 of the AXI address.

Table 1431: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

13f8

Reserved @0x13fc

Provides bits 63:32 of the AXI address.

Table 1432: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 47 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1400

Provides bits 31:0 of the AXI address.

Table 1433: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 47 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1404

Provides bits 63:32 of the AXI address.

Table 1434: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 47 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1408

Provides bits 31:0 of the AXI address.

Table 1435: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 47 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x140c

Provides bits 63:32 of the AXI address.

Table 1436: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 47 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1410

Provides bits 31:0 of the AXI address.

Table 1437: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 47 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1414

Provides bits 63:32 of the AXI address.

Table 1438: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 47 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1418

Provides bits 31:0 of the AXI address.

Table 1439: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 47 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x141c

Provides bits 63:32 of the AXI address.

Table 1440: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 47 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1420

Provides bits 31:0 of the AXI address.

Table 1441: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 47 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1424

Provides bits 63:32 of the AXI address.

Table 1442: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 47 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1428

Provides bits 31:0 of the AXI address.

Table 1443: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 47 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x142c

Provides bits 63:32 of the AXI address.

Table 1444: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 47 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1430

Provides bits 31:0 of the AXI address.

Table 1445: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 47 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1434

Provides bits 63:32 of the AXI address.

Table 1446: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1438

Provides bits 31:0 of the AXI address.

Table 1447: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x143c

Provides bits 63:32 of the AXI address.

Table 1448: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 48 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1440

Provides bits 31:0 of the AXI address.

Table 1449: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 48 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1444

Provides bits 63:32 of the AXI address.

Table 1450: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 48 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1448

Provides bits 31:0 of the AXI address.

Table 1451: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 48 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x144c

Provides bits 63:32 of the AXI address.

Table 1452: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 48 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1450

Provides bits 31:0 of the AXI address.

Table 1453: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 48 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1454

Provides bits 63:32 of the AXI address.

Table 1454: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 48 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1458

Provides bits 31:0 of the AXI address.

Table 1455: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 48 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x145c

Provides bits 63:32 of the AXI address.

Table 1456: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 48 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1460

Provides bits 31:0 of the AXI address.

Table 1457: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 48 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1464

Provides bits 63:32 of the AXI address.

Table 1458: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 48 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1468

Provides bits 31:0 of the AXI address.

Table 1459: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 48 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x146c

Provides bits 63:32 of the AXI address.

Table 1460: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 48 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1470

Provides bits 31:0 of the AXI address.

Table 1461: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 48 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1474

Provides bits 63:32 of the AXI address.

Table 1462: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1478

Provides bits 31:0 of the AXI address.

Table 1463: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x147c

Provides bits 63:32 of the AXI address.

Table 1464: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 49 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1480

Provides bits 31:0 of the AXI address.

Table 1465: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 49 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1484

Provides bits 63:32 of the AXI address.

Table 1466: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 49 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1488

Provides bits 31:0 of the AXI address.

Table 1467: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 49 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x148c

Provides bits 63:32 of the AXI address.

Table 1468: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 49 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1490

Provides bits 31:0 of the AXI address.

Table 1469: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 49 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1494

Provides bits 63:32 of the AXI address.

Table 1470: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 49 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1498

Provides bits 31:0 of the AXI address.

Table 1471: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 49 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x149c

Provides bits 63:32 of the AXI address.

Table 1472: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 49 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x14a0

Provides bits 31:0 of the AXI address.

Table 1473: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 49 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x14a4

Provides bits 63:32 of the AXI address.

Table 1474: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 49 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x14a8

Provides bits 31:0 of the AXI address.

Table 1475: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 49 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x14ac

Provides bits 63:32 of the AXI address.

Table 1476: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 49 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x14b0

Provides bits 31:0 of the AXI address.

Table 1477: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 49 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x14b4

Provides bits 63:32 of the AXI address.

Table 1478: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x14b8

Provides bits 31:0 of the AXI address.

Table 1479: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x14bc

Provides bits 63:32 of the AXI address.

Table 1480: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 50 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x14c0

Provides bits 31:0 of the AXI address.

Table 1481: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 50 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x14c4

Provides bits 63:32 of the AXI address.

Table 1482: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 50 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x14c8

Provides bits 31:0 of the AXI address.

Table 1483: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 50 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x14cc

Provides bits 63:32 of the AXI address.

Table 1484: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 50 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x14d0

Provides bits 31:0 of the AXI address.

Table 1485: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 50 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x14d4

Provides bits 63:32 of the AXI address.

Table 1486: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 50 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x14d8

Provides bits 31:0 of the AXI address.

Table 1487: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 50 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x14dc

Provides bits 63:32 of the AXI address.

Table 1488: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 50 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x14e0

Provides bits 31:0 of the AXI address.

Table 1489: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 50 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x14e4

Provides bits 63:32 of the AXI address.

Table 1490: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 50 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x14e8

Provides bits 31:0 of the AXI address.

Table 1491: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 50 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x14ec

Provides bits 63:32 of the AXI address.

Table 1492: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 50 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x14f0

Provides bits 31:0 of the AXI address.

Table 1493: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 50 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x14f4

Provides bits 63:32 of the AXI address.

Table 1494: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x14f8

Provides bits 31:0 of the AXI address.

Table 1495: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x14fc

Provides bits 63:32 of the AXI address.

Table 1496: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 51 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1500

Provides bits 31:0 of the AXI address.

Table 1497: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 51 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1504

Provides bits 63:32 of the AXI address.

Table 1498: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 51 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1508

Provides bits 31:0 of the AXI address.

Table 1499: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 51 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x150c

Provides bits 63:32 of the AXI address.

Table 1500: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 51 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1510

Provides bits 31:0 of the AXI address.

Table 1501: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 51 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1514

Provides bits 63:32 of the AXI address.

Table 1502: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 51 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1518

Provides bits 31:0 of the AXI address.

Table 1503: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 51 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x151c

Provides bits 63:32 of the AXI address.

Table 1504: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 51 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1520

Provides bits 31:0 of the AXI address.

Table 1505: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 51 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1524

Provides bits 63:32 of the AXI address.

Table 1506: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 51 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1528

Provides bits 31:0 of the AXI address.

Table 1507: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 51 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x152c

Provides bits 63:32 of the AXI address.

Table 1508: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 51 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1530

Provides bits 31:0 of the AXI address.

Table 1509: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 51 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1534

Provides bits 63:32 of the AXI address.

Table 1510: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1538

Provides bits 31:0 of the AXI address.

Table 1511: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x153c

Provides bits 63:32 of the AXI address.

Table 1512: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 52 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1540

Provides bits 31:0 of the AXI address.

Table 1513: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 52 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1544

Provides bits 63:32 of the AXI address.

Table 1514: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 52 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1548

Provides bits 31:0 of the AXI address.

Table 1515: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 52 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x154c

Provides bits 63:32 of the AXI address.

Table 1516: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 52 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1550

Provides bits 31:0 of the AXI address.

Table 1517: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 52 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1554

Provides bits 63:32 of the AXI address.

Table 1518: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 52 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1558

Provides bits 31:0 of the AXI address.

Table 1519: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 52 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x155c

Provides bits 63:32 of the AXI address.

Table 1520: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 52 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1560

Provides bits 31:0 of the AXI address.

Table 1521: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 52 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1564

Provides bits 63:32 of the AXI address.

Table 1522: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 52 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1568

Provides bits 31:0 of the AXI address.

Table 1523: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 52 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x156c

Provides bits 63:32 of the AXI address.

Table 1524: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 52 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1570

Provides bits 31:0 of the AXI address.

Table 1525: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 52 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1574

Provides bits 63:32 of the AXI address.

Table 1526: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1578

Provides bits 31:0 of the AXI address.

Table 1527: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x157c

Provides bits 63:32 of the AXI address.

Table 1528: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 53 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1580

Provides bits 31:0 of the AXI address.

Table 1529: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 53 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1584

Provides bits 63:32 of the AXI address.

Table 1530: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 53 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1588

Provides bits 31:0 of the AXI address.

Table 1531: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 53 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x158c

Provides bits 63:32 of the AXI address.

Table 1532: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 53 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1590

Provides bits 31:0 of the AXI address.

Table 1533: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 53 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1594

Provides bits 63:32 of the AXI address.

Table 1534: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 53 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1598

Provides bits 31:0 of the AXI address.

Table 1535: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 53 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x159c

Provides bits 63:32 of the AXI address.

Table 1536: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 53 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x15a0

Provides bits 31:0 of the AXI address.

Table 1537: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 53 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x15a4

Provides bits 63:32 of the AXI address.

Table 1538: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 53 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x15a8

Provides bits 31:0 of the AXI address.

Table 1539: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 53 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x15ac

Provides bits 63:32 of the AXI address.

Table 1540: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 53 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x15b0

Provides bits 31:0 of the AXI address.

Table 1541: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 53 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x15b4

Provides bits 63:32 of the AXI address.

Table 1542: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x15b8

Provides bits 31:0 of the AXI address.

Table 1543: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x15bc

Provides bits 63:32 of the AXI address.

Table 1544: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 54 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x15c0

Provides bits 31:0 of the AXI address.

Table 1545: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 54 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x15c4

Provides bits 63:32 of the AXI address.

Table 1546: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 54 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x15c8

Provides bits 31:0 of the AXI address.

Table 1547: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 54 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x15cc

Provides bits 63:32 of the AXI address.

Table 1548: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 54 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x15d0

Provides bits 31:0 of the AXI address.

Table 1549: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 54 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x15d4

Provides bits 63:32 of the AXI address.

Table 1550: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 54 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x15d8

Provides bits 31:0 of the AXI address.

Table 1551: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 54 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x15dc

Provides bits 63:32 of the AXI address.

Table 1552: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 54 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x15e0

Provides bits 31:0 of the AXI address.

Table 1553: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 54 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x15e4

Provides bits 63:32 of the AXI address.

Table 1554: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 54 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x15e8

Provides bits 31:0 of the AXI address.

Table 1555: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 54 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x15ec

Provides bits 63:32 of the AXI address.

Table 1556: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 54 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x15f0

Provides bits 31:0 of the AXI address.

Table 1557: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 54 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x15f4

Provides bits 63:32 of the AXI address.

Table 1558: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x15f8

Provides bits 31:0 of the AXI address.

Table 1559: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x15fc

Provides bits 63:32 of the AXI address.

Table 1560: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 55 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1600

Provides bits 31:0 of the AXI address.

Table 1561: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 55 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1604

Provides bits 63:32 of the AXI address.

Table 1562: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 55 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1608

Provides bits 31:0 of the AXI address.

Table 1563: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 55 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x160c

Provides bits 63:32 of the AXI address.

Table 1564: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 55 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1610

Provides bits 31:0 of the AXI address.

Table 1565: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 55 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1614

Provides bits 63:32 of the AXI address.

Table 1566: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 55 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1618

Provides bits 31:0 of the AXI address.

Table 1567: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 55 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x161c

Provides bits 63:32 of the AXI address.

Table 1568: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 55 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1620

Provides bits 31:0 of the AXI address.

Table 1569: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 55 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1624

Provides bits 63:32 of the AXI address.

Table 1570: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 55 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1628

Provides bits 31:0 of the AXI address.

Table 1571: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 55 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x162c

Provides bits 63:32 of the AXI address.

Table 1572: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 55 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1630

Provides bits 31:0 of the AXI address.

Table 1573: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 55 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1634

Provides bits 63:32 of the AXI address.

Table 1574: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1638

Provides bits 31:0 of the AXI address.

Table 1575: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x163c

Provides bits 63:32 of the AXI address.

Table 1576: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 56 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1640

Provides bits 31:0 of the AXI address.

Table 1577: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 56 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1644

Provides bits 63:32 of the AXI address.

Table 1578: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 56 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1648

Provides bits 31:0 of the AXI address.

Table 1579: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 56 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x164c

Provides bits 63:32 of the AXI address.

Table 1580: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 56 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1650

Provides bits 31:0 of the AXI address.

Table 1581: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 56 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1654

Provides bits 63:32 of the AXI address.

Table 1582: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 56 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1658

Provides bits 31:0 of the AXI address.

Table 1583: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 56 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x165c

Provides bits 63:32 of the AXI address.

Table 1584: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 56 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1660

Provides bits 31:0 of the AXI address.

Table 1585: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 56 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1664

Provides bits 63:32 of the AXI address.

Table 1586: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 56 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1668

Provides bits 31:0 of the AXI address.

Table 1587: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 56 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x166c

Provides bits 63:32 of the AXI address.

Table 1588: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 56 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1670

Provides bits 31:0 of the AXI address.

Table 1589: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 56 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1674

Provides bits 63:32 of the AXI address.

Table 1590: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1678

Provides bits 31:0 of the AXI address.

Table 1591: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x167c

Provides bits 63:32 of the AXI address.

Table 1592: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 57 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1680

Provides bits 31:0 of the AXI address.

Table 1593: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 57 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1684

Provides bits 63:32 of the AXI address.

Table 1594: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 57 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1688

Provides bits 31:0 of the AXI address.

Table 1595: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 57 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x168c

Provides bits 63:32 of the AXI address.

Table 1596: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 57 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1690

Provides bits 31:0 of the AXI address.

Table 1597: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 57 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1694

Provides bits 63:32 of the AXI address.

Table 1598: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 57 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1698

Provides bits 31:0 of the AXI address.

Table 1599: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 57 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x169c

Provides bits 63:32 of the AXI address.

Table 1600: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 57 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x16a0

Provides bits 31:0 of the AXI address.

Table 1601: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 57 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x16a4

Provides bits 63:32 of the AXI address.

Table 1602: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 57 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x16a8

Provides bits 31:0 of the AXI address.

Table 1603: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 57 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x16ac

Provides bits 63:32 of the AXI address.

Table 1604: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 57 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x16b0

Provides bits 31:0 of the AXI address.

Table 1605: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 57 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x16b4

Provides bits 63:32 of the AXI address.

Table 1606: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x16b8

Provides bits 31:0 of the AXI address.

Table 1607: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x16bc

Provides bits 63:32 of the AXI address.

Table 1608: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 58 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x16c0

Provides bits 31:0 of the AXI address.

Table 1609: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 58 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x16c4

Provides bits 63:32 of the AXI address.

Table 1610: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 58 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x16c8

Provides bits 31:0 of the AXI address.

Table 1611: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 58 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x16cc

Provides bits 63:32 of the AXI address.

Table 1612: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 58 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x16d0

Provides bits 31:0 of the AXI address.

Table 1613: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 58 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x16d4

Provides bits 63:32 of the AXI address.

Table 1614: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 58 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x16d8

Provides bits 31:0 of the AXI address.

Table 1615: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 58 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x16dc

Provides bits 63:32 of the AXI address.

Table 1616: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 58 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x16e0

Provides bits 31:0 of the AXI address.

Table 1617: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 58 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x16e4

Provides bits 63:32 of the AXI address.

Table 1618: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 58 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x16e8

Provides bits 31:0 of the AXI address.

Table 1619: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 58 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x16ec

Provides bits 63:32 of the AXI address.

Table 1620: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 58 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x16f0

Provides bits 31:0 of the AXI address.

Table 1621: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 58 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x16f4

Provides bits 63:32 of the AXI address.

Table 1622: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x16f8

Provides bits 31:0 of the AXI address.

Table 1623: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x16fc

Provides bits 63:32 of the AXI address.

Table 1624: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 59 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1700

Provides bits 31:0 of the AXI address.

Table 1625: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 59 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1704

Provides bits 63:32 of the AXI address.

Table 1626: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 59 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1708

Provides bits 31:0 of the AXI address.

Table 1627: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 59 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x170c

Provides bits 63:32 of the AXI address.

Table 1628: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 59 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1710

Provides bits 31:0 of the AXI address.

Table 1629: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 59 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1714

Provides bits 63:32 of the AXI address.

Table 1630: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 59 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1718

Provides bits 31:0 of the AXI address.

Table 1631: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 59 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x171c

Provides bits 63:32 of the AXI address.

Table 1632: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 59 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1720

Provides bits 31:0 of the AXI address.

Table 1633: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 59 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1724

Provides bits 63:32 of the AXI address.

Table 1634: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 59 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1728

Provides bits 31:0 of the AXI address.

Table 1635: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 59 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x172c

Provides bits 63:32 of the AXI address.

Table 1636: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 59 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1730

Provides bits 31:0 of the AXI address.

Table 1637: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 59 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1734

Provides bits 63:32 of the AXI address.

Table 1638: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1738

Provides bits 31:0 of the AXI address.

Table 1639: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x173c

Provides bits 63:32 of the AXI address.

Table 1640: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 60 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1740

Provides bits 31:0 of the AXI address.

Table 1641: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 60 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1744

Provides bits 63:32 of the AXI address.

Table 1642: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 60 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1748

Provides bits 31:0 of the AXI address.

Table 1643: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 60 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x174c

Provides bits 63:32 of the AXI address.

Table 1644: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 60 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1750

Provides bits 31:0 of the AXI address.

Table 1645: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 60 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1754

Provides bits 63:32 of the AXI address.

Table 1646: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 60 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1758

Provides bits 31:0 of the AXI address.

Table 1647: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 60 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x175c

Provides bits 63:32 of the AXI address.

Table 1648: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 60 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1760

Provides bits 31:0 of the AXI address.

Table 1649: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 60 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1764

Provides bits 63:32 of the AXI address.

Table 1650: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 60 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1768

Provides bits 31:0 of the AXI address.

Table 1651: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 60 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x176c

Provides bits 63:32 of the AXI address.

Table 1652: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 60 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1770

Provides bits 31:0 of the AXI address.

Table 1653: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 60 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1774

Provides bits 63:32 of the AXI address.

Table 1654: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1778

Provides bits 31:0 of the AXI address.

Table 1655: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x177c

Provides bits 63:32 of the AXI address.

Table 1656: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 61 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1780

Provides bits 31:0 of the AXI address.

Table 1657: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 61 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1784

Provides bits 63:32 of the AXI address.

Table 1658: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 61 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1788

Provides bits 31:0 of the AXI address.

Table 1659: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 61 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x178c

Provides bits 63:32 of the AXI address.

Table 1660: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 61 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1790

Provides bits 31:0 of the AXI address.

Table 1661: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 61 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1794

Provides bits 63:32 of the AXI address.

Table 1662: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 61 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1798

Provides bits 31:0 of the AXI address.

Table 1663: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 61 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x179c

Provides bits 63:32 of the AXI address.

Table 1664: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 61 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x17a0

Provides bits 31:0 of the AXI address.

Table 1665: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 61 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x17a4

Provides bits 63:32 of the AXI address.

Table 1666: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 61 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x17a8

Provides bits 31:0 of the AXI address.

Table 1667: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 61 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x17ac

Provides bits 63:32 of the AXI address.

Table 1668: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 61 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x17b0

Provides bits 31:0 of the AXI address.

Table 1669: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 61 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x17b4

Provides bits 63:32 of the AXI address.

Table 1670: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x17b8

Provides bits 31:0 of the AXI address.

Table 1671: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x17bc

Provides bits 63:32 of the AXI address.

Table 1672: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 62 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x17c0

Provides bits 31:0 of the AXI address.

Table 1673: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 62 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x17c4

Provides bits 63:32 of the AXI address.

Table 1674: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 62 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x17c8

Provides bits 31:0 of the AXI address.

Table 1675: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 62 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x17cc

Provides bits 63:32 of the AXI address.

Table 1676: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 62 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x17d0

Provides bits 31:0 of the AXI address.

Table 1677: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 62 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x17d4

Provides bits 63:32 of the AXI address.

Table 1678: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 62 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x17d8

Provides bits 31:0 of the AXI address.

Table 1679: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 62 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x17dc

Provides bits 63:32 of the AXI address.

Table 1680: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 62 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x17e0

Provides bits 31:0 of the AXI address.

Table 1681: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 62 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x17e4

Provides bits 63:32 of the AXI address.

Table 1682: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 62 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x17e8

Provides bits 31:0 of the AXI address.

Table 1683: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 62 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x17ec

Provides bits 63:32 of the AXI address.

Table 1684: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 62 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x17f0

Provides bits 31:0 of the AXI address.

Table 1685: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 62 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x17f4

Provides bits 63:32 of the AXI address.

Table 1686: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x17f8

Provides bits 31:0 of the AXI address.

Table 1687: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x17fc

Provides bits 63:32 of the AXI address.

Table 1688: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 63 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1800

Provides bits 31:0 of the AXI address.

Table 1689: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 63 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1804

Provides bits 63:32 of the AXI address.

Table 1690: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 63 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1808

Provides bits 31:0 of the AXI address.

Table 1691: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 63 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x180c

Provides bits 63:32 of the AXI address.

Table 1692: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 63 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1810

Provides bits 31:0 of the AXI address.

Table 1693: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 63 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1814

Provides bits 63:32 of the AXI address.

Table 1694: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 63 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1818

Provides bits 31:0 of the AXI address.

Table 1695: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 63 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x181c

Provides bits 63:32 of the AXI address.

Table 1696: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 63 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1820

Provides bits 31:0 of the AXI address.

Table 1697: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 63 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1824

Provides bits 63:32 of the AXI address.

Table 1698: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 63 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1828

Provides bits 31:0 of the AXI address.

Table 1699: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 63 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x182c

Provides bits 63:32 of the AXI address.

Table 1700: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 63 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1830

Provides bits 31:0 of the AXI address.

Table 1701: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 63 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1834

Provides bits 63:32 of the AXI address.

Table 1702: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1838

Provides bits 31:0 of the AXI address.

Table 1703: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x183c

Provides bits 63:32 of the AXI address.

Table 1704: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 64 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1840

Provides bits 31:0 of the AXI address.

Table 1705: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 64 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1844

Provides bits 63:32 of the AXI address.

Table 1706: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 64 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1848

Provides bits 31:0 of the AXI address.

Table 1707: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 64 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x184c

Provides bits 63:32 of the AXI address.

Table 1708: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 64 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1850

Provides bits 31:0 of the AXI address.

Table 1709: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 64 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1854

Provides bits 63:32 of the AXI address.

Table 1710: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 64 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1858

Provides bits 31:0 of the AXI address.

Table 1711: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 64 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x185c

Provides bits 63:32 of the AXI address.

Table 1712: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 64 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1860

Provides bits 31:0 of the AXI address.

Table 1713: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 64 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1864

Provides bits 63:32 of the AXI address.

Table 1714: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 64 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1868

Provides bits 31:0 of the AXI address.

Table 1715: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 64 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x186c

Provides bits 63:32 of the AXI address.

Table 1716: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 64 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1870

Provides bits 31:0 of the AXI address.

Table 1717: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 64 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1874

Provides bits 63:32 of the AXI address.

Table 1718: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1878

Provides bits 31:0 of the AXI address.

Table 1719: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x187c

Provides bits 63:32 of the AXI address.

Table 1720: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 65 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1880

Provides bits 31:0 of the AXI address.

Table 1721: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 65 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1884

Provides bits 63:32 of the AXI address.

Table 1722: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 65 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1888

Provides bits 31:0 of the AXI address.

Table 1723: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 65 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x188c

Provides bits 63:32 of the AXI address.

Table 1724: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 65 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1890

Provides bits 31:0 of the AXI address.

Table 1725: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 65 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1894

Provides bits 63:32 of the AXI address.

Table 1726: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 65 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1898

Provides bits 31:0 of the AXI address.

Table 1727: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 65 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x189c

Provides bits 63:32 of the AXI address.

Table 1728: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 65 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x18a0

Provides bits 31:0 of the AXI address.

Table 1729: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 65 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x18a4

Provides bits 63:32 of the AXI address.

Table 1730: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 65 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x18a8

Provides bits 31:0 of the AXI address.

Table 1731: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 65 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x18ac

Provides bits 63:32 of the AXI address.

Table 1732: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 65 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x18b0

Provides bits 31:0 of the AXI address.

Table 1733: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 65 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x18b4

Provides bits 63:32 of the AXI address.

Table 1734: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x18b8

Provides bits 31:0 of the AXI address.

Table 1735: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x18bc

Provides bits 63:32 of the AXI address.

Table 1736: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 66 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x18c0

Provides bits 31:0 of the AXI address.

Table 1737: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 66 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x18c4

Provides bits 63:32 of the AXI address.

Table 1738: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 66 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x18c8

Provides bits 31:0 of the AXI address.

Table 1739: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 66 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x18cc

Provides bits 63:32 of the AXI address.

Table 1740: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 66 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x18d0

Provides bits 31:0 of the AXI address.

Table 1741: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 66 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x18d4

Provides bits 63:32 of the AXI address.

Table 1742: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 66 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x18d8

Provides bits 31:0 of the AXI address.

Table 1743: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 66 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x18dc

Provides bits 63:32 of the AXI address.

Table 1744: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 66 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x18e0

Provides bits 31:0 of the AXI address.

Table 1745: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 66 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x18e4

Provides bits 63:32 of the AXI address.

Table 1746: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 66 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x18e8

Provides bits 31:0 of the AXI address.

Table 1747: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 66 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x18ec

Provides bits 63:32 of the AXI address.

Table 1748: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 66 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x18f0

Provides bits 31:0 of the AXI address.

Table 1749: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 66 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x18f4

Provides bits 63:32 of the AXI address.

Table 1750: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x18f8

Provides bits 31:0 of the AXI address.

Table 1751: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x18fc

Provides bits 63:32 of the AXI address.

Table 1752: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 67 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1900

Provides bits 31:0 of the AXI address.

Table 1753: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 67 BAR 0 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1904

Provides bits 63:32 of the AXI address.

Table 1754: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 67 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1908

Provides bits 31:0 of the AXI address.

Table 1755: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 67 BAR 1 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x190c

Provides bits 63:32 of the AXI address.

Table 1756: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 67 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1910

Provides bits 31:0 of the AXI address.

Table 1757: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 67 BAR 2 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1914

Provides bits 63:32 of the AXI address.

Table 1758: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 67 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1918

Provides bits 31:0 of the AXI address.

Table 1759: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 67 BAR 3 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x191c

Provides bits 63:32 of the AXI address.

Table 1760: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 67 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1920

Provides bits 31:0 of the AXI address.

Table 1761: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 67 BAR 4 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1924

Provides bits 63:32 of the AXI address.

Table 1762: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 67 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1928

Provides bits 31:0 of the AXI address.

Table 1763: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 67 BAR 5 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x192c

Provides bits 63:32 of the AXI address.

Table 1764: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Function 67 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 0 [31:0] @0x1930

Provides bits 31:0 of the AXI address.

Table 1765: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Function 67 BAR 6 Endpoint Inbound PCIe to AXI Address Translation Register 1 [63:32] @0x1934

Provides bits 63:32 of the AXI address.

Table 1766: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Reserved @0x1938

Provides bits 31:0 of the AXI address.

Table 1767: addr0

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [31:0] [data]	Bits [31:0] of Address Register for BAR N.	32'h00000000

Reserved @0x193c

Provides bits 63:32 of the AXI address.

Table 1768: addr1

Bits	SW	Name	Description	Reset
31:0	R/W	Address bits [63:32] [data]	Bits [63:32] of AXI Address Register for BAR N.	32'h00000000

Revision History

Table 1769: Document Revision History

Date	Version	Description
December 2025	1.1	Added **Root Port Configuration Register Set** on page 135. (DOC-2831) Updated **Debug Mux Control Register @0x208** on page 196.
July 2024	1.0	Initial release.