CIS

UHD SDI TX Specifications For Elitestek

Revision 1.0

CIS Corporation

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For Elitestek

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1. Introduction

UHD SDI TX is the IP of SDI(Serial Digital Interface) transmitter. It is designed based on the SMPTE (Society of Motion Picture and Television Engineers) standards, and supports HD-SDI, 3G-SDI Level A, 3G-SDI Level B, 6G-SDI type 1 and type 2.

1.1. Features

UHD SDI TX supports the following standards:

- SMPTE ST 292-1 (HD-SDI).
- SMPTE ST 424 (3G-SDI).
- SMPTE ST 425 (3G Level-A/B)
- SMPTE ST 2081-1 (6G-SDI).

UHD SDI TX supports the following functions:

- Generation and insertion of Line Number (LN) packets.
- Generation and insertion of CRC packets.
- Generation and insertion of Video Payload Identification (VPID) packets.
- Insertion of sync-bits in timing reference words in 6G-SDI standards.
- Scrambling and NRZI encoding.
- Dynamically changing SDI modes(6G-SDI, 3G/HD-SDI).

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1.2. Overview

The typical system integration of UHD SDI TX is depicted in Figure 1-1. The video signal output from the User Logic is connected to the UHD SDI TX IP via the SDI Bridge. The SDI Bridge is a circuit that maps the video signal to an SDI data stream defined by the SMPTE standards and is provided as a sample design by CIS. The SDI transmission data encoded in the IP is output through the FPGA's Transceiver.

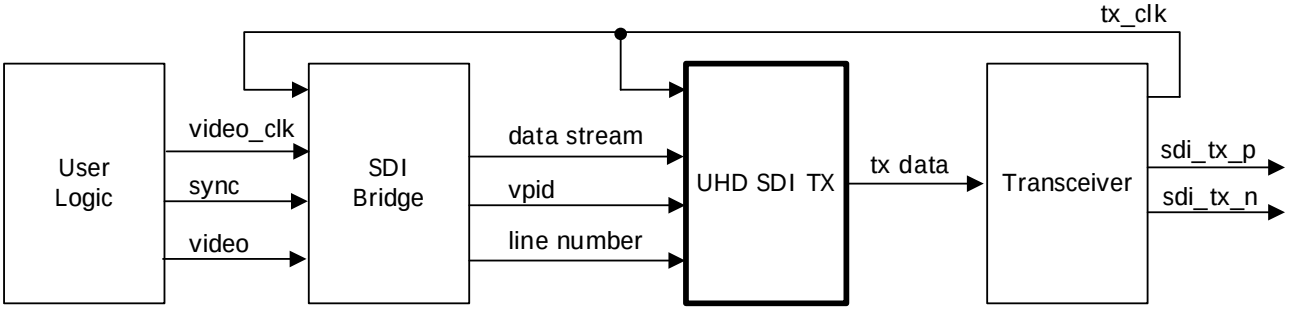

Figure 1-1 System Block Diagram

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2. Interface

2.1. Configuration Parameter

Table 2-1 shows the configurable parameters of the IP.

Table 2-1 Configuration Parameters

Name	Type	Range	Descriptions
DS_NUM	integer	2,4(default)	The maximum number of valid data streams (other than those listed below are not supported) 2 : 3G/HD-SDI 4 : 6G-SDI

2.2. Ports

Table 2-2 I/O ports

Name	Width	I/O	Description
i_clk	1	I	Transmit clock. HD-SDI : 74.25(/1.001)MHz 3G/6G: 148.5(/1.001)MHz
i_rst	1	I	Synchronous reset.(Active High)
o_tx_data[N*10-1:0]	N*10	O	Tx data to transceiver.
i_data_ds[N-1:0][9:0]	N*10	I	Data Stream. [0][9:0] : Data Stream1 [1][9:0] : Data Stream2 … [N-1][9:0] : Data StreamN
i_ln[N-1:0][10:0]	N*11	I	Line Number to be inserted in Data Stream. [0][10:0] : To be inserted in Data Stream1. [1][10:0] : To be inserted in Data Stream2. … [N-1][10:0] : To be inserted in Data StreamN.
i_vpid[N-1:0][31:0]	N*32	I	VPID to be inserted in Data Stream. [7:0] Byte1, [15:8] Byte2, [23:16] Byte3, [31:24] Byte4 [0][31:0] : To be inserted in Data Stream1. [1][31:0] : To be inserted in Data Stream2. … [N-1][31:0] : To be inserted in Data StreamN.
i_vpid_ln_f1[N-1:0][10:0]	N*11	I	Line number for VPID insertion in Data Stream field 1. [0][10:0] : Line number in field 1 for VPID insertion in

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Name	Width	I/O	Description
			Data Stream1. [1][10:0] : Line number in field 1 for VPID insertion in Data Stream2. … [N-1][10:0] : Line number in field 1 for VPID insertion in Data StreamN.
i_vpid_ln_f2[N-1:0][10:0]	N*11	I	Line number for VPID insertion in Data Stream field 2. [0][10:0] : Line number in field 2 for VPID insertion in Data Stream1. [1][10:0] : Line number in field 2 for VPID insertion in Data Stream2. … [N-1][10:0] : Line number in field 2 for VPID insertion in Data StreamN.
i_anc_ds[N-1:0][10:0]	N*10	I	ANC packet. [0][9:0] : ANC packet insertion in DataStream1. [1][9:0] : ANC packet insertion in DataStream2. … [N-1][9:0] : ANC packet insertion in DataStreamN.
i_anc_valid[N-1:0][10:0]	N*10	I	Valid for ANC packet(i_anc_ds) [0] : Valid for i_anc_ds[0]. … [N-1] : Valid for i_anc_ds[N-1].
i_insert_ln_en	1	I	Line Number insertion enable.
i_insert_crc_en	1	I	CRC insertion enable.
i_insert_vpid_en	1	I	VPID insertion enable.
i_sdi_mode[1:0]	2	I	2'b00 : HD/3G-SDI 2'b01 : 6G-SDI
o_sav	1	O	start of line.
o_eav	1	O	end of line.
o_field	1	O	field.
o_version	8	O	version of IP.

※ N is DS_NUM.

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3. Function Description

3.1. Top Diagram

Table 3-1 shows the SDI modes that are supported based on the parameter DS_NUM. Figure 3-1 shows the top diagram of this IP.

Table 3-1 DS_NUM and SDI mode

DS_NUM \ SDI Mode	6G-SDI	3G/HD-SDI
4	○	○
2		○

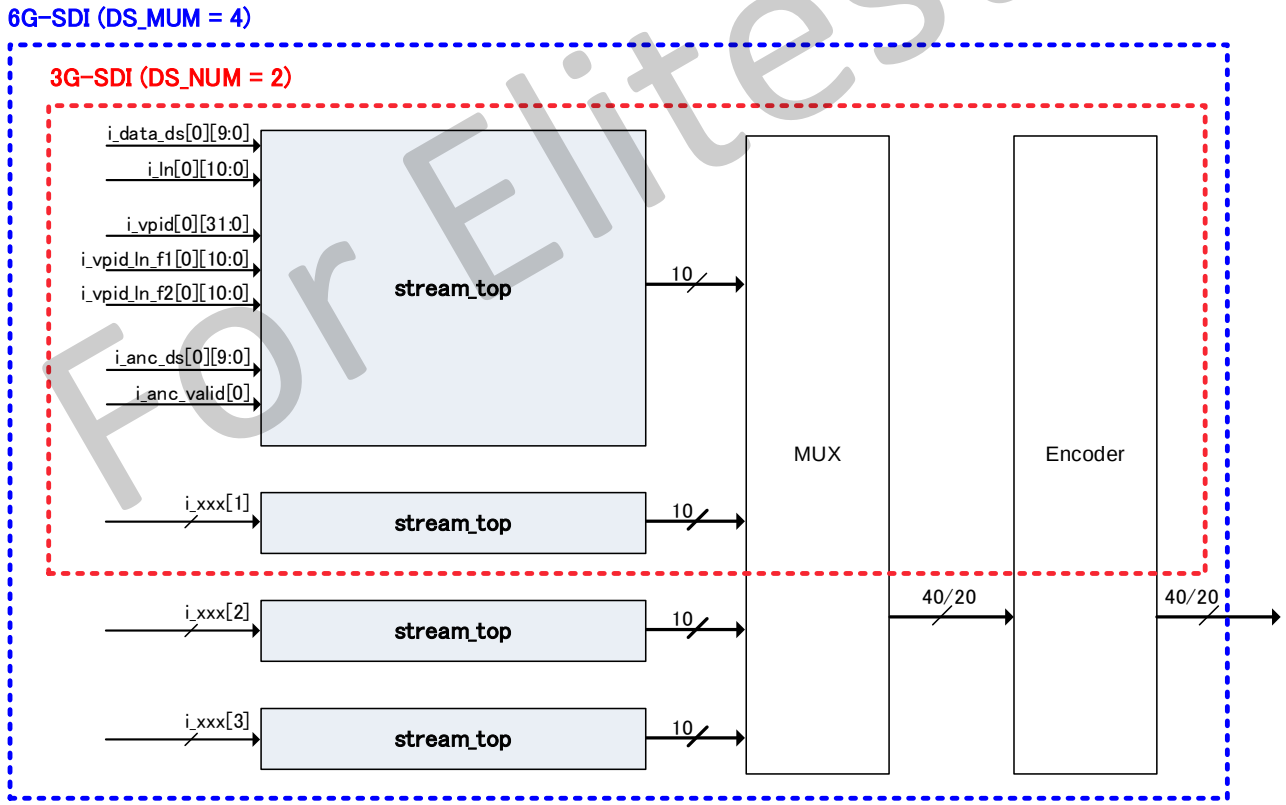

Figure 3-1 Top Diagram

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3.2. Stream Top Diagram

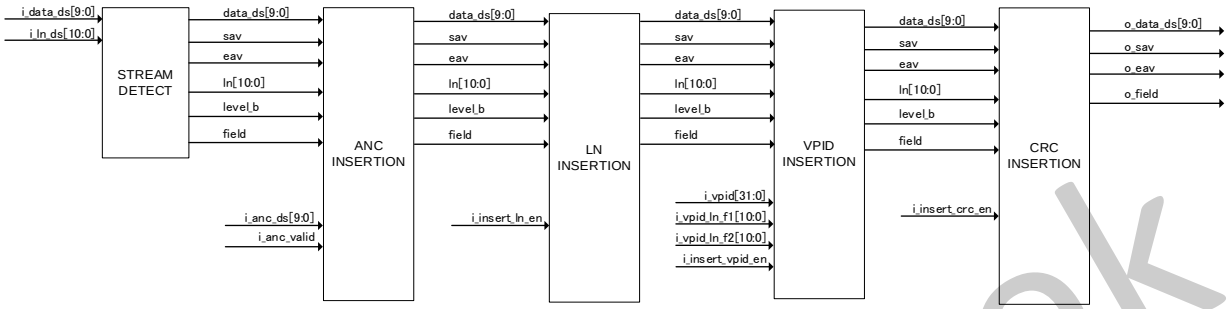

Figure 3-2 stream top diagram

3.3. STREAM DETECT

The SAV, EAV, FIELD and Level-B mode are detected from input data stream. The line number is latched at the timing of the last word of EAV.

3.4. ANC INSERTION

ANC INSERTION inserts the i_anc_ds[*] to i_data_ds[*] when i_anc_valid[*] is high.

Figure 3-3 shows the timing for the input and output of Ancillary Data. For the timing of TRS Code, CRC, and Line Number, please set i_anc_valid[*] to Low.

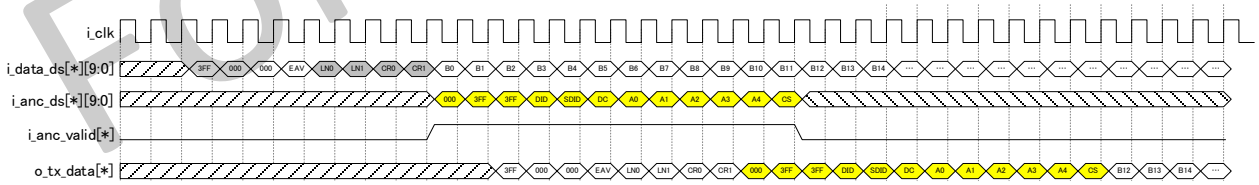

Figure 3-3 Ancillary data

3.5. LN INSERTION

LN INSERTION encodes the line number to LN0/LN1 packets as defined in the SMPTE specification. LN0/LN1 packets are inserted into data stream at the appropriate positions as defined in the SMPTE specification. LN INSERTION performs the line number packet insertion into the data stream when the i_insert_ln_en input is high.。Figure 3-4 and Figure 3-5 show the input and output of i_ln.

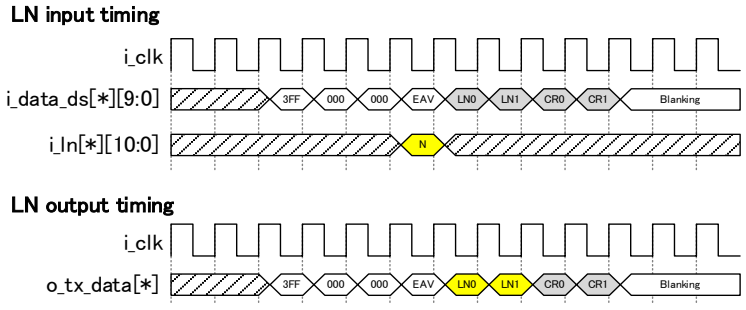

Figure 3-4 3G Level-A, 6G type1 LN input/output timing

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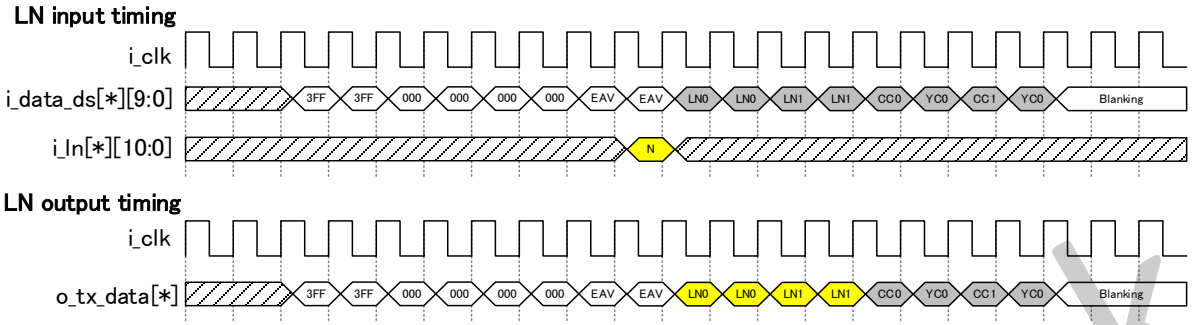

Figure 3-5 3G Level-B, 6G type2 LN input/output timing

3.6. VPID INSERTION

VPID INSERTION generates the VPID packet appropriate format as the SMPTE ST 352. The VPID packet will be inserted at the beginning of the HANC(Blanking) space of the line specified by the i_vpid_ln_f1[*] and i_vpid_ln_f2[*]. i_vpid_ln_f1[*] specifies a line number in field 1. When field 2 in the XYZ word, i_vpid_ln_f2[*] specifies a line number in field 2. VPID INSERTION performs the VPID packet insertion when the i_insert_vpid_en input is high。Figure 3-6 and Figure 3-7 show the insertion timing of the VPID.

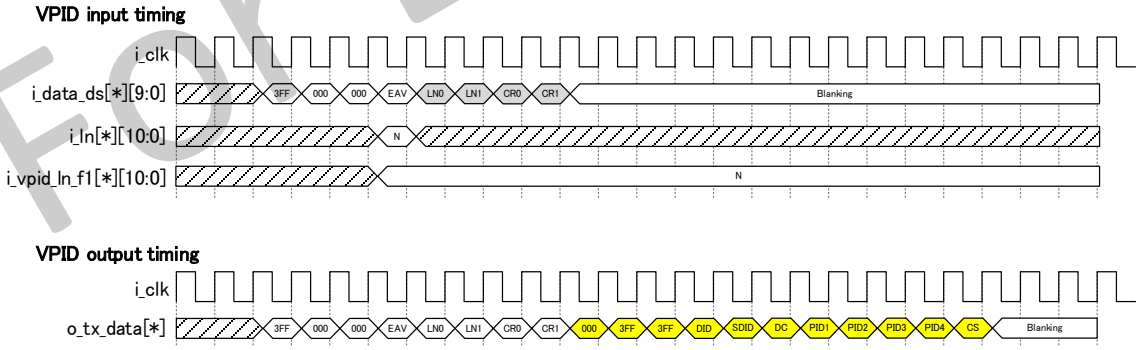

Figure 3-6 3G Level-A, 6G type1 VPID output timing

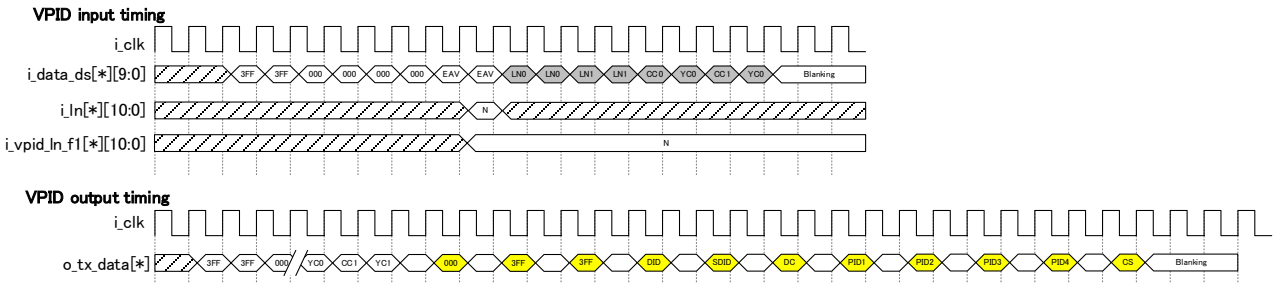

Figure 3-7 3G Level-B, 6G type2 VPID output timing

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3.7. CRC INSERTION

CRC INSERTION computes the 18-bit CRC and encodes the CR0 and CR1 packets as defined in the SMPTE specification. CR0/CR1 packets are inserted to data stream at the appropriate positions as defined in the SMPTE specification. The CRC computation is performed for every line of the data stream.

The CRC generation polynomial is as follows:

$$CRC(X) = X^{18} + X^5 + X^4 + 1$$

3.8. MUX

MUX performs the 10-bit multiplex of data streams as defined in the SMPTE specification. Sync-bit insertion is performed only in 6G-SDI mode.

3.9. Encoder

Encoder performs the scrambling and NRZI encoding. The scrambling is performed as per the scrambling polynomial specified in the SMPTE specification.

$$G_1(X) = X^9 + X^4 + 1$$

The NRZI encoding is performed by SDI NRZI Encoder on the scrambled data. NRZI encoding is performed as per the polynomial specified in the SMPTE specification.

$$G_2(X) = X + 1$$

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4. Timing Diagrams

4.1. 3G-SDI Level-A, 6G-SDI type1

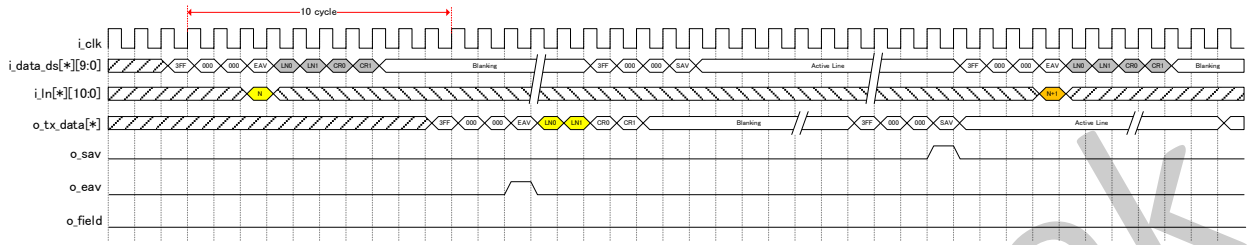

Figure 4-1 3G-SDI Level-A, 6G-SDI type1 input/output timing

4.2. 3G-SDI Level-B, 6G-SDI type2

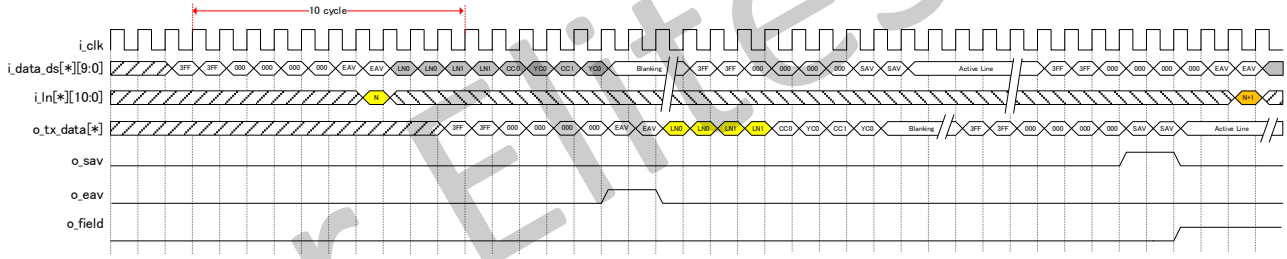

Figure 4-2 3G Level-B, 6G type2 input/output timing

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5. Resource

Table5-1[1] shows the resource usage for each SDI mode.

Table 5-1 resource usage

SDI Standard	DS_NUM	DW[2]	FFs	SRLs	ADDs	LUTs	COMB4s	RAMs	DSPs	Fmax [MHz]
6G-SDI	4	40	1278	0	108	1332	0	0	0	203
3G(HD)-SDI	2	20	623	0	54	603	0	0	0	289

[1]: Synthesis result of Efinity 2024.2 (TJ375N1156X).

[2]: Tx Data Width(bits)

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6. Revision History

6.1. IP History

Date	Version	Descriptions
2025-03-21	01	First Edition.

6.2. Document History

Date	Version	Descriptions
2025-03-21	1.0	First Edition.

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