CIS

UHD SDI TX RX Reference Design User Guide For Elitestek

Revision 1.0

CIS Corporation

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1. Introduction

This user guide explains the functionality of the UHD SDI TX and RX reference design using the Elitestek TJ375N1156X evaluation board. This reference design supports the following features.

- Outputs images generated by the UHD pattern generator through the SDI TX IP. (Chapter 2.3.1)
- Decodes input data from SDI In and outputs it to HDMI and SDI Out. (Chapter 2.3.3)
- SDI TX and RX support 5.94Gbps, 2.97Gbps, and 1.485Gbps.

1.1. Evaluation system

As shown in Figure 1-1, this evaluation system consists of the TJ375N1156X Board, 12G-SDI FMC Card, FMC to QSE Adapter Card (Rev.B), HDMI Connector Daughter Card, and other components. Table 1-1 lists the components of the system evaluation. Since this evaluation system uses serial communication, an application such as Tera Term is required.

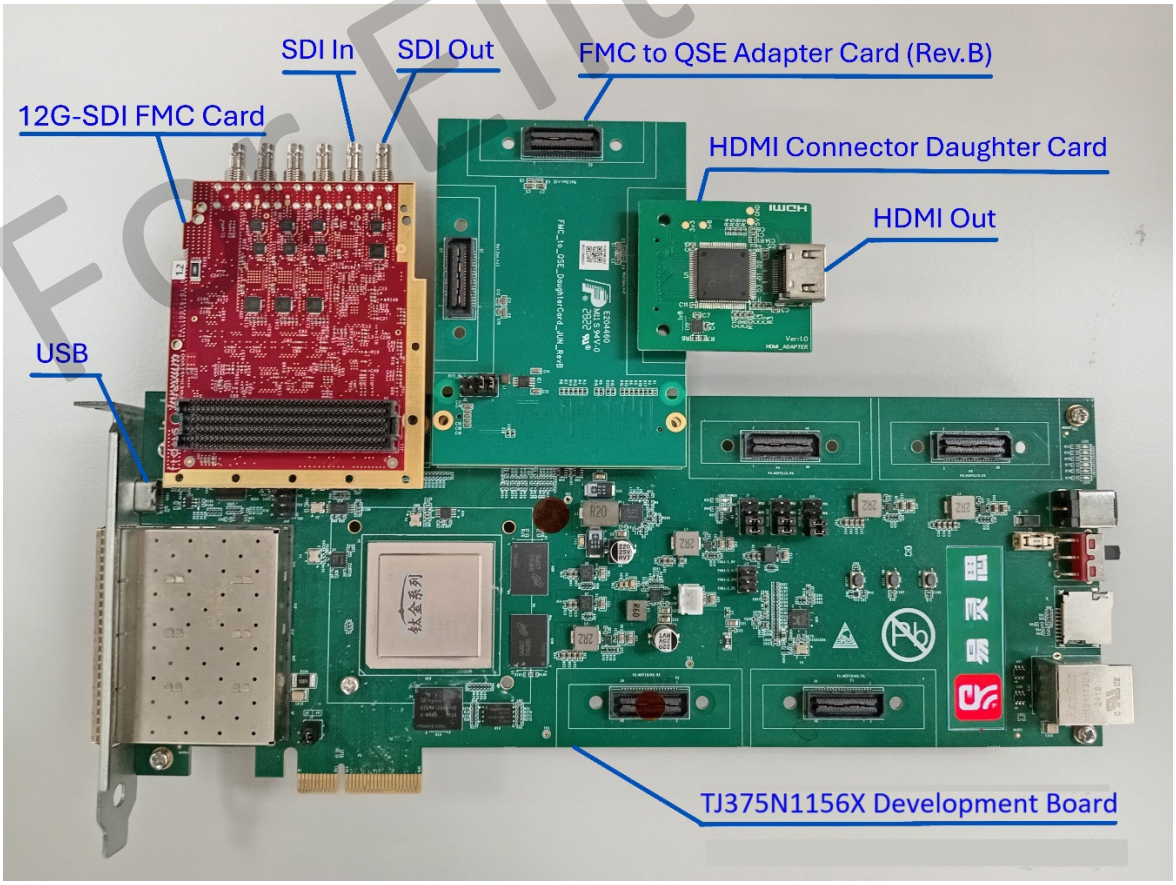

Figure 1-1 Evaluation system

Table 1-1 Components of the evaluation system

No.	Components	Note
1	TJ375N1156X Development Board	- Vendor: Elitestek
2	12G-SDI FMC Card	- Vendor: TOKYO ELECTRON DEVICE
3	FMC to QSE Adapter Card (Rev.B)	- Vendor: Elitestek
4	HDMI Connector Daughter Card	- Vendor: Elitestek
5	HDMI Cable	- The cable needs to support 1080p60
6	SDI Monitor	- e.g. SDI Wave Monitor
7	SDI Cable	- The cable needs to support 6G-SDI
8	SDI Source	- e.g. SDI Camera
9	USB Type-C Cable	
10	AC adaptor	
11	Efinity	- Version : 2024.2 - Patch : 2024.2.294.3.14

1.2. Reference Design Overview

Figure 1-2 shows the block diagram of the reference design. This reference design mainly consists of the 4K Color Bar generation function (sdi_pg_top), SDI output function (sdi_tx_wrapper), SDI input function (sdi_rx_wrapper), HDMI output function (HDMI), and two DDR Controllers (hdmi_ddr_ctrl_top and sdi_ddr_ctrl_top).

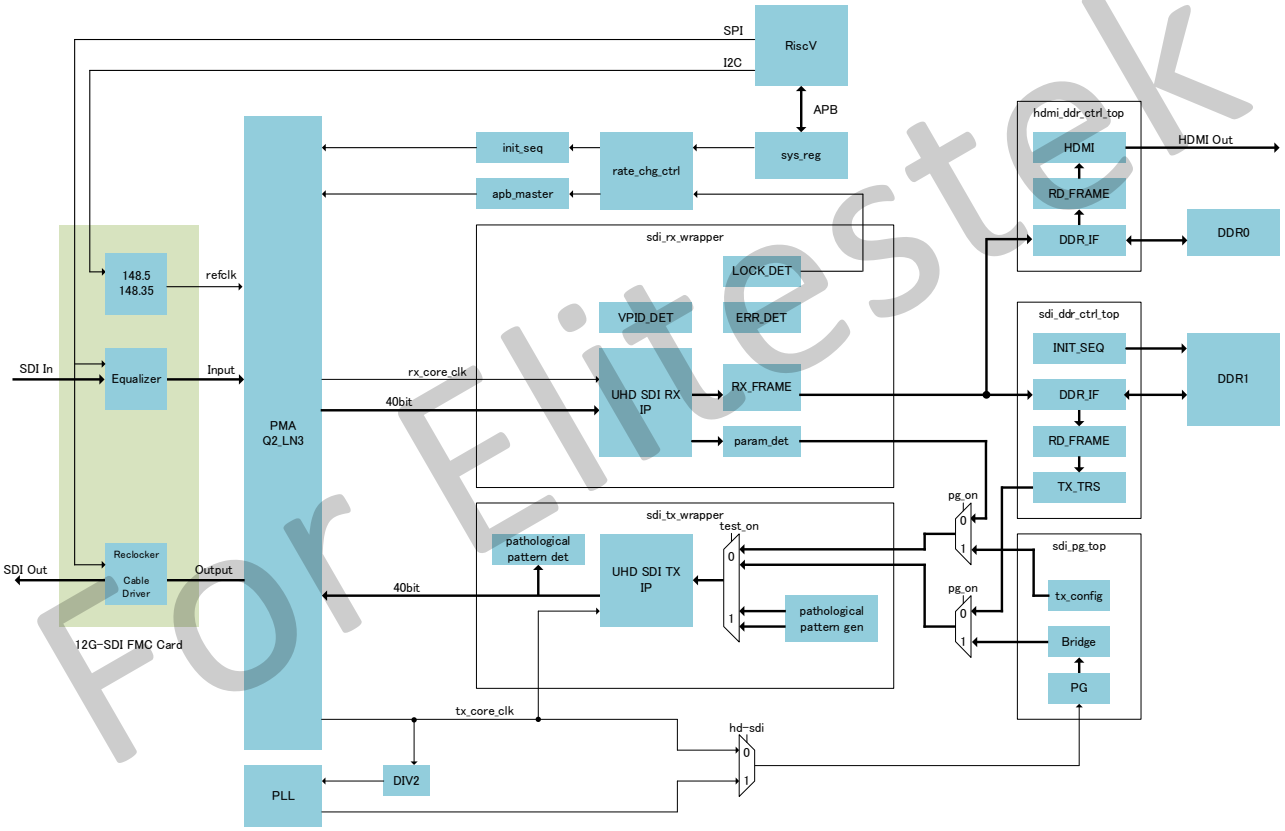

Figure 1-2 Top block diagram

2. Evaluation environment setup

2.1. Jumper settings

Set the jumpers according to Table2-1.

Table 2-1 Jumper settings

Header	Connection	Description
J3	N.C.	VADJ=1.8V
J6	5 and 6 7 and 8	VCCIO_QSE=3.3V
J7	5 and 6 7 and 8	VCCIO_MIPI=1.2V
J18	5 and 6 7 and 8	VCCIO_BL0=3.3V

2.2. FPGA Programming

To use the TJ375N1156X Development Board, you need to install the USB drivers in advance. For installation instructions, please refer to the TJ375N1156X Development Board User Guide. After installing the USB drivers, please follow the steps below to program the reference design.

1. Please ensure that the FMC to QSE Adapter Card(Rev.B) is not connected to J14 (FMCA).
   IMPORTANT : If the FMC to QSE Adapter Card(Rev.B) is connected, programming cannot be performed.
2. Turn on the power of the TJ375N1156X Development Board.
3. Launch the Efinity Programmer.
4. Set the Programming Mode to "SPI Active using JTAG Bridge (new).
5. Select the following Bitstream file.
   (project folder)¥Bitstream¥Combine¥Combine_efx_sdi_rd_v1.hex
   This file is a combination of the FPGA and firmware.
   FPGA(.hex) : 0x0000_0000
   FW(.bin) : 0x0080_0000
6. Click the "Start Program" button to begin the programming process.
7. After the programming is complete, turn off the power of the evaluation board.

2.3. Connection hardware

The reference design has three operating modes. Please connect according to the following for each operating mode.

2.3.1. Color Bar to SDI Monitor

The generated color bar image will be output to SDI Out in the specified format.
This reference design supports 19 different SDI TX formats, all of which can be verified. For details, please refer to section 3.1.Color Bar to SDI Monitor.

1. Connect the 12G-SDI FMC Card to J15 (FMCB) on the TJ375N1156X Development Board.
2. Connect the SDI Out of the 12G-SDI FMC Card (Figure 1-1) to the SDI Monitor.
   (The FMC to QSE Adapter Card is not required.)

2.3.2. Color Bar to HDMI Monitor

The generated color bar image is output to SDI Out in the specified format, and the color bar image input from SDI In is decoded and output to HDMI. This operational mode is recommended when SDI Source and SDI Monitor are not available. For more details, refer to section 3.2.Color Bar to HDMI Monitor.

1. Connect the 12G-SDI FMC Card to J15 (FMCB) on the TJ375N1156X Development Board.
2. Connect J4 (SDI Out) and J5 (SDI In) on the 12G-SDI FMC Card.
3. Connect the FMC to QSE Adapter Card (Rev.B) to J14 (FMCA) on the TJ375N1156X Development Board.
4. Connect the HDMI Out (Figure 1.1) of the HDMI Connector Daughter Card to the HDMI Monitor.

2.3.3. SDI Source to SDI Monitor

The input data from SDI In is decoded and output to SDI Out. If an HDMI Monitor is connected, the data will also be output to HDMI. This operational mode is recommended when outputting images other than color bars. For more details, refer to section 3.3 SDI Source to SDI Monitor.

1. Connect the 12G-SDI FMC Card to J15 (FMCB) on the TJ375N1156X Development Board.
2. Connect SDI Source to J5 (SDI RX) on the 12G-SDI FMC Card.
3. Connect SDI Monitor to J4 (SDI TX) on the 12G-SDI FMC Card.

(If the FMC to QSE Adapter Card, HDMI Connector Daughter Card, and HDMI Monitor are connected, the data will also be output to HDMI.)

3. Running the Design

After turning on the power, set up the serial communication software. Select the available USB serial COM port and configure it with the following settings:

Baud Rate : 115200
Data : 8bit
Parity : None
Stop Bit : 1bit
Flow Control : None

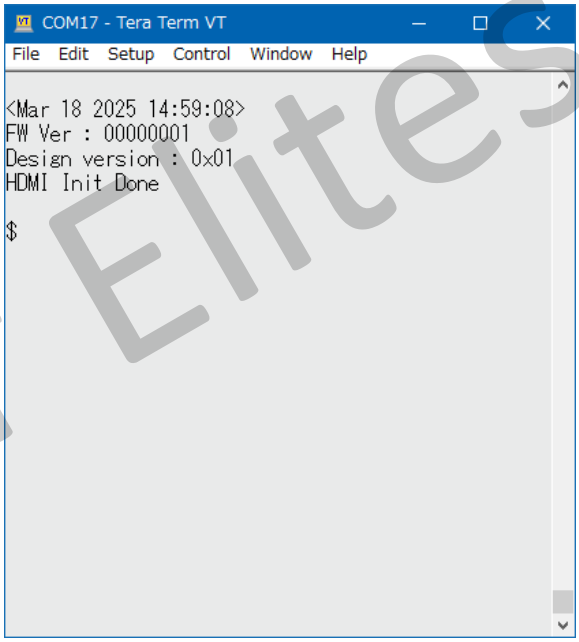

Figure 3-1 Power up log

3.1. Color Bar to SDI Monitor

3.1.1. Data flow

Figure 3-2 shows the data flow from the Color Bar to the SDI Monitor.

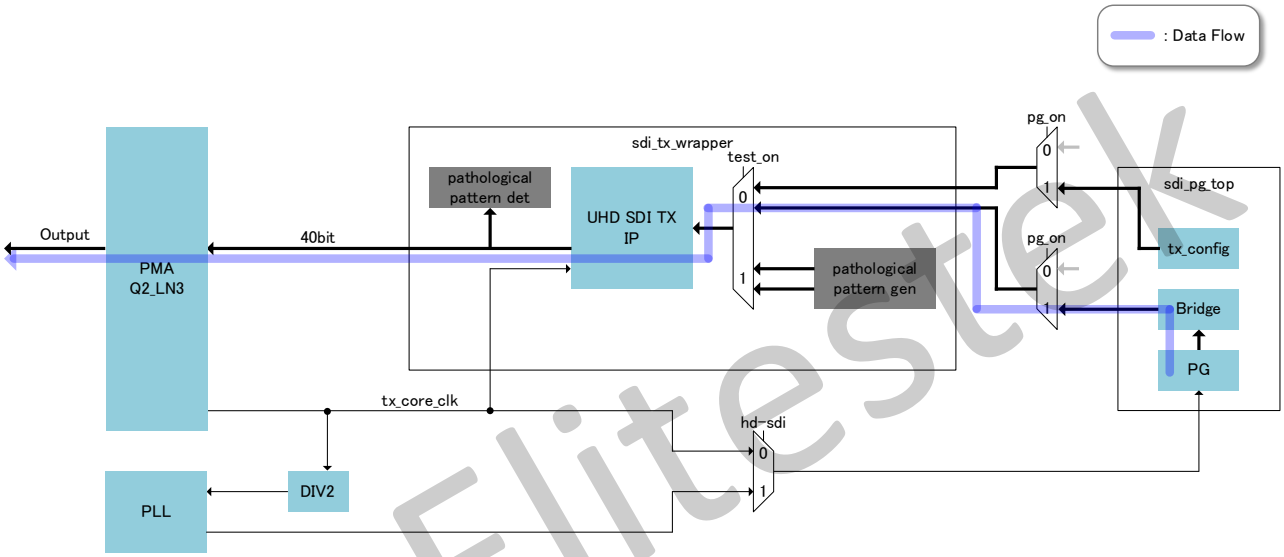

Figure 3-2 Data flow of Color Bar to SDI Out

3.1.2. Configuration

Table 3-1 shows the settings for Color Bar to SDI Monitor.

Table 3-1 Color Bar to SDI Monitor Configuration

Command	Description
`pg on`	The color bar data is input to the sdi_tx_wrapper.
`fmt <Index>`	Switching the output SDI format.

Note: In the reference design, "`pg on`, `fmt 13`" is the default setting, so after power-up, a 1080p60 color bar image will be output to the SDI. For details on the commands, please refer to Section 5.Control Commands.

3.1.3. SDI Out

Table 3-2 shows the supported SDI output formats. The sampling structure only supports YCbCr 4:2:2 (10bit).

Table 3-2 SDI output format

Index	Rate	SDI Format
0	1.485Gbps	1080i50
1	1.485Gbps	1080i59.94
2	1.485Gbps	1080i60

3	1.485Gbps	1080p23.98
4	1.485Gbps	1080p24
5	1.485Gbps	1080p25
6	1.485Gbps	1080p29.97
7	1.485Gbps	1080p30
8	2.97Gbps	1080p50B
9	2.97Gbps	1080p50A
10	2.97Gbps	1080p59.94B
11	2.97Gbps	1080p59.94A
12	2.97Gbps	1080p60B
13	2.97Gbps	1080p60A
14	5.94Gbps	2160P23.98
15	5.94Gbps	2160P24
16	5.94Gbps	2160P25
17	5.94Gbps	2160P29.97
18	5.94Gbps	2160p30

Figure 3-3 shows the color bar image output. The color bar image shifts to the left on a frame-by-frame basis.

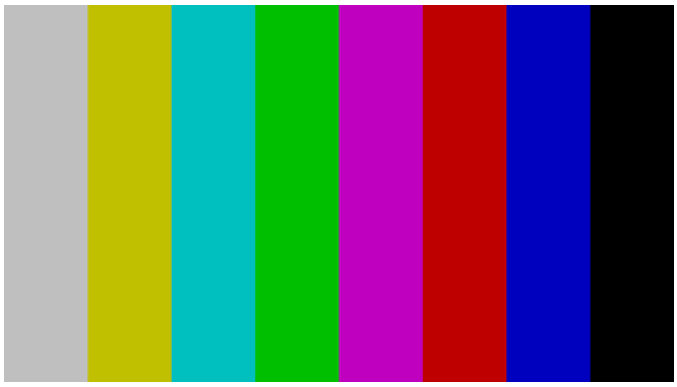

Figure 3-3 Color Bar

3.2. Color Bar to HDMI Monitor

3.2.1. Data flow

Figure 3-4 shows the data flow from the Color Bar to HDMI Out.

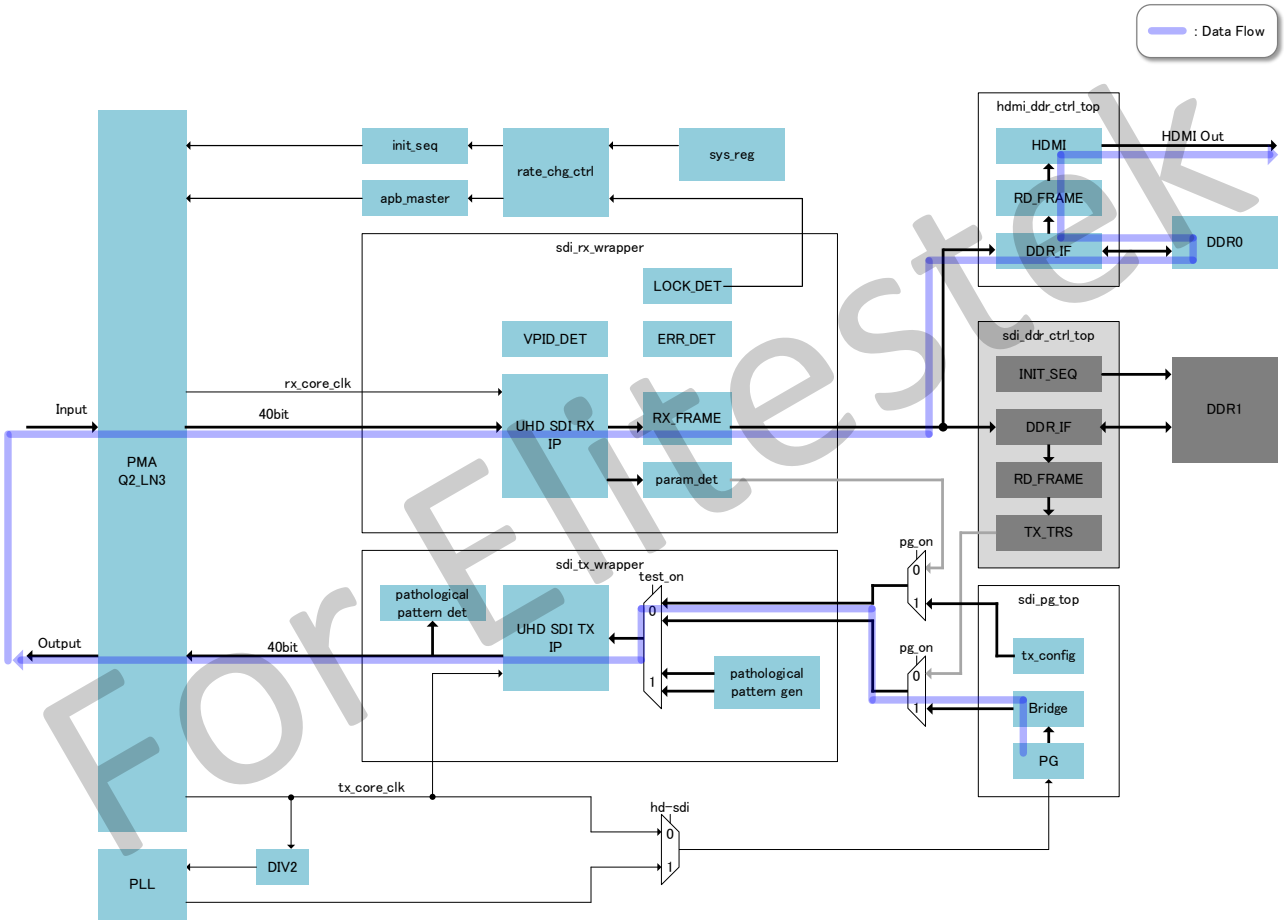

Figure 3-4 Data flow of Color Bar to HDMI Out

3.2.2. Configuration

The configuration for Color Bar to HDMI Monitor is the same as the configuration for Color Bar to SDI Monitor in section 3.1. For details, please refer to section 3.1.2. Configuration.

3.2.3. HDMI Out

In the hdmi_ddr_ctrl_top, after decoding the SDI input data, it writes to the DDR memory and then reads from it to output to HDMI. The HDMI output is fixed at 1920x1080 60fps. If the color bar input is 4K (3840x2160), only substream 1 (out of the 4 substreams in a 2 sample interleave format) will be written to the DDR memory. The hdmi_ddr_ctrl_top does not support 3G-Level B or Interlace format, so for these formats (Index 0, 1, 2, 8, 10, and 12 in Table 3-2), HDMI output is not possible.

3.3. SDI Source to SDI Monitor

3.3.1. Data flow

Figure 3-5 shows the data flow from the SDI Source to the SDI Monitor. If an HDMI Monitor is connected, the data from the SDI Source will also be output to the HDMI.

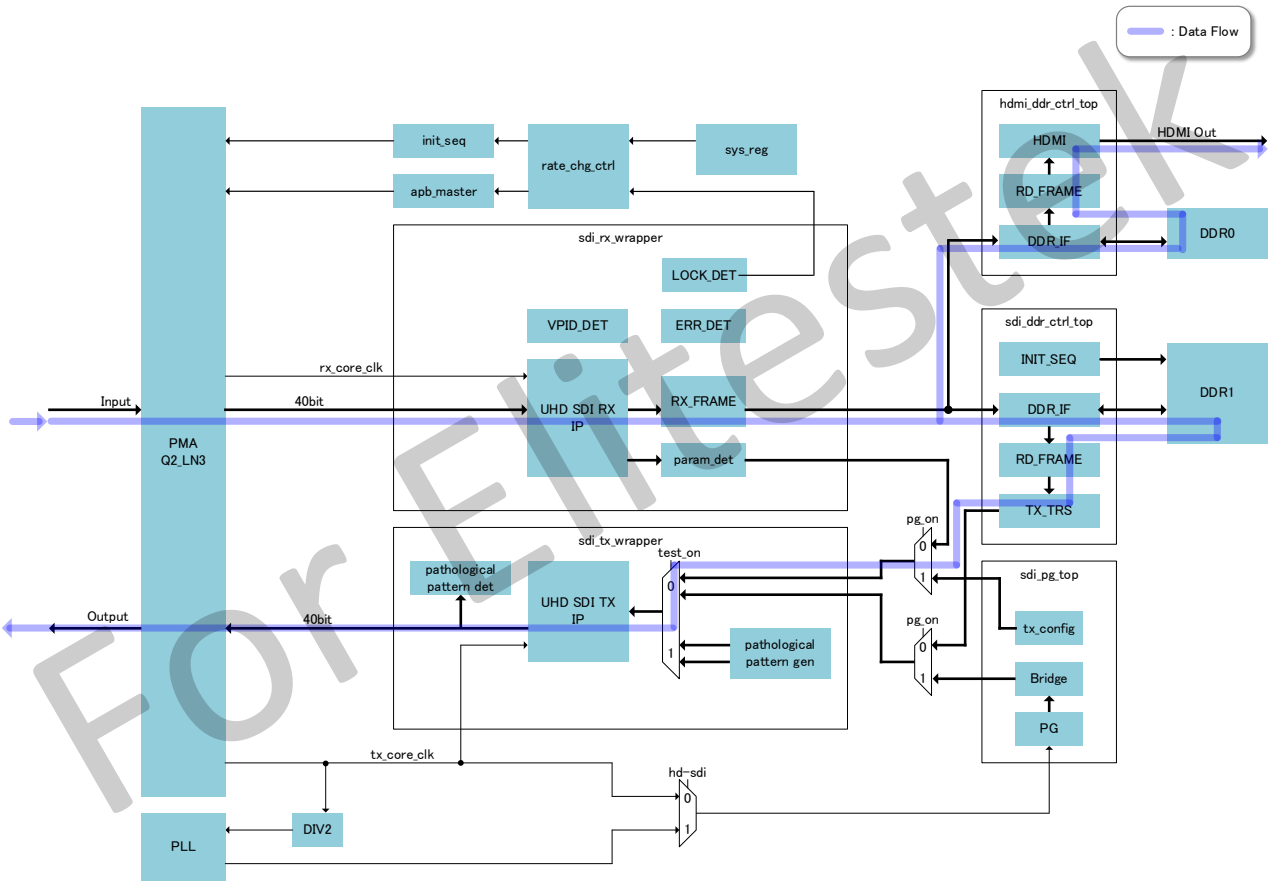

Figure 3-5 Data flow of SDI In to SDI Out

3.3.2. Configuration

Table 3-3 shows the configuration for SDI Source to SDI Monitor.

Table 3-3 SDI Source to SDI Monitor Configuration

Command	Description
`pg off`	The read data from DDR1 is input to the sdi_tx_wrapper.
`refsel <0/1>`	Switching between two PMA reference clocks: 148.5 MHz (0) and 148.35 MHz (1).
`status`	Display status.

The PMA rate will automatically switch between 1.485Gbps, 2.97Gbps and 5.94Gbps until the SDI RX locks. Once the SDI RX locks, the received data will be output to SDI according to the set rate. If the reference clock type of the SDI source differs from the reference clock type input to the PMA, a warning will appear

in the status as shown in Figure 3-6. In this case, the reference clock type input to the PMA must be switched using the command `refsel <0/1>`.

```
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
! Warning : Rx data rate and reference clock is mismatch        !
!          Please use cmd [refsel <0/1>] to change reference clock.!
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
```

Figure 3-6 Warning message

3.3.3. SDI Out

In sdi_ddr_ctrl_top, SDI input data is decoded, written to DDR memory, and then read out and output to SDI. Since sdi_ddr_ctrl_top does not support 3G-Level B or Interlace formats, SDI Out and HDMI output are not available in the case of 3G-Level B and Interlace formats. Information such as the received VPID can be checked via the Command `status`.

3.4. Pathological pattern testing

This function is used when evaluating low-frequency response. When enabled, it generates stress signals for cable equalization and phase-locked loop (PLL) lock-in after SDI encoding, as shown in Figure 3-7.

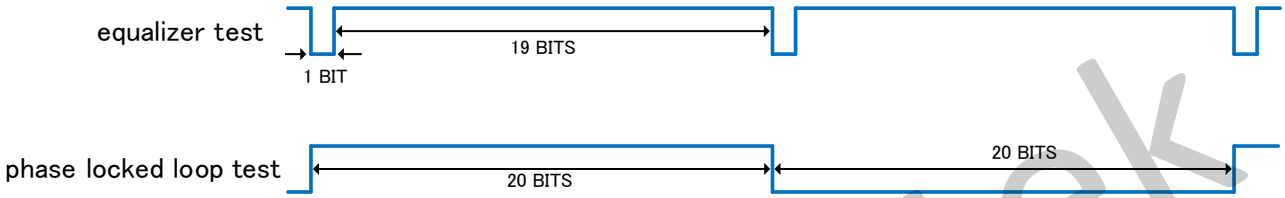

Figure 3-7 Pathological patterns

Figure 3-8 shows the data flow during the pathological pattern test.

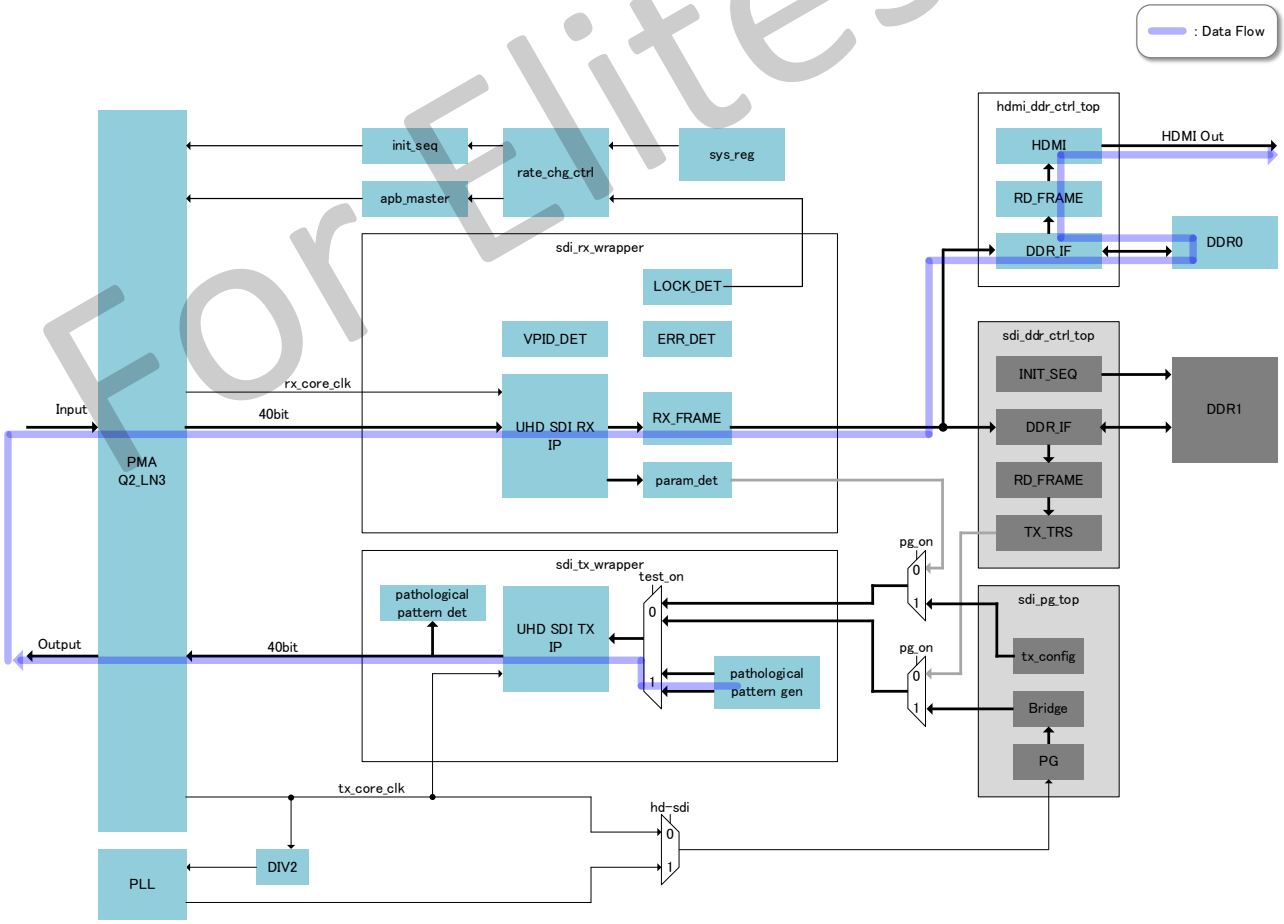

Figure 3-8 Data flow of pathological pattern test

3.4.1. Configuration

Table 3-4 shows the settings for pathological pattern testing.

Table 3-4 Test Configuration

Command	Description
`pg on`	Set the DataRate to manual mode.
`fmt <index>`	Change datarate. 7 : hd-sdi 13 : 3G-SDI 18 : 6G-SDI
`test on`	Pathological pattern on.
`testsel <eq/phase>`	Switching between two pathological patterns.(6G-SDI only) eq: equalizer test signal phase : phase locked loop test signal
`status`	Display status.

Use “`pg on`” and “`fmt <index>`” to set the desired SDI Rate for testing. Enable the Pathological Pattern Generator with “`test on`”.

For HD-SDI and 3G-SDI, one frame simultaneously outputs both the Equalizer Test Signal (at the top of the frame) and the Phase Locked Loop Test Signal (at the bottom of the frame).

For 6G-SDI, you need to manually switch between the Equalizer Test Signal and the Phase Locked Loop Test Signal using “`testsel <eq/phase>`”.

After connecting SDI Out to SDI In, use “`status`” to verify that there are no errors.

Table 3-5 shows the output image of the pathological pattern.

Table 3-5 Output image of the pathological pattern

Format	SDI/HDMI Output Image
HD/3G-SDI	

6G-SDI Equalizer Test Signal	
6G-SDI Phase Locked Loop Test Signal	

3.4.2. Efinity Debugger

Figure 3-9 and Figure 3-10 show the test signals observed using the Efinity Debugger. As shown in Figure 3-8, the 40-bit data "0xFFEFFFFFEFF" is output continuously, and the SDI serial output through the transceiver consists of a repeating pattern of 19 consecutive 1s followed by a single 0.

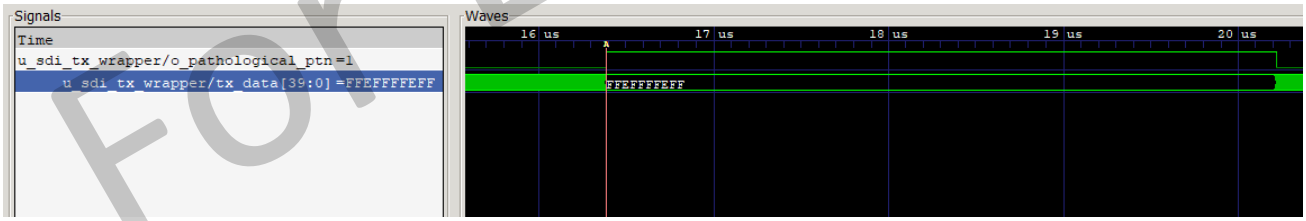

Figure 3-9 Efinity Debugger for equalizer test signal

As shown in Figure 3-10, the 40-bit data "0xFFE00001FF" is output continuously, and the SDI serial output through the transceiver consists of a repeating pattern of 20 consecutive 1s followed by 20 consecutive 0s.

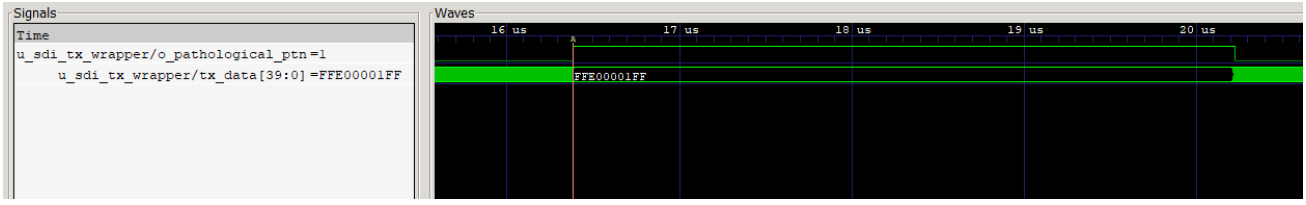

Figure 3-10 Efinity Debugger for phase locked loop test signal

Note : When using the Efinity Debugger, do not connect the HDMI Connector Daughter Card.

3.5. LED indicator

Table 3-6 shows the LED assignment.

Table 3-6 LED Assignment

Name	Assignment	Note
LED1 (green)	pg_on	0: SDI Out from SDI In 1: SDI Out from PG(Color Bar)
LED2 (green)	sdi_rx_align_done	0: Align done of SDI RX is Low. 1: Align done of SDI RX is High.
LED3 (green)	rx_clock_divider	6G-SDI/3G-SDI：1s Low <-> 1s High HD-SDI：2s Low <-> 2s High
LED4 (green)	sdi_rx_lock	0: SDI RX is unlock 1: SDI RX is lock
LED5 (red)	pma_rate[0]	pma_rate[1:0] 2'b00: 1.485 Gbps 2'b01: 2.97 Gbps 2'b10: 5.94 Gbps
LED6 (red)	pma_rate[1]	

4. Reference Design Details

4.1. SDI TX

Figure 4-1 shows the block diagram of SDI TX.

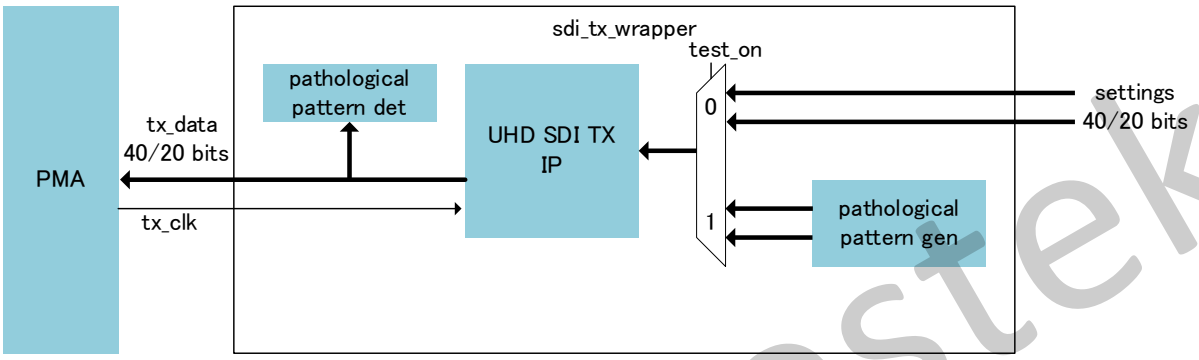

Figure 4-1 SDI TX Block Diagram

The functions of each block are as follows:

- **UHD SDI TX IP**

  CIS's UHD SDI TX IP.

- **Pathological pattern gen**

  This block generates pathological patterns. Table 4-1 shows the Output Format corresponding to each SDI Rate.

Table 4-1 output format for pathological pattern

SDI Rate	Output Format
HD-SDI	1080p30
3G-SDI	1080p60 Level-A
6G-SDI	2160p30 type1

- **Pathological pattern det**

  Detects pathological patterns from encoded data and generates a trigger for observation.

Table 4-2 shows the SDI Mode and Clock frequencies.

Table 4-2 SDI TX Mode and clock frequency

SDI Mode	PMA Preset	tx_clk[MHz]	input data width
6G-SDI	5.94-148.5-40 bits	148.5	40 bits
3G-SDI	2.97-148.5-20 bits	148.5	20 bits
HD-SDI	1.485-148.5-20 bits	74.25	20 bits

Note : When the PMA reference clock is 1000/1001, the clock frequency in Table 4-1 will be 1000/1001.

4.2. SDI RX

Figure 4-2 shows the Block Diagram of the SDI RX.

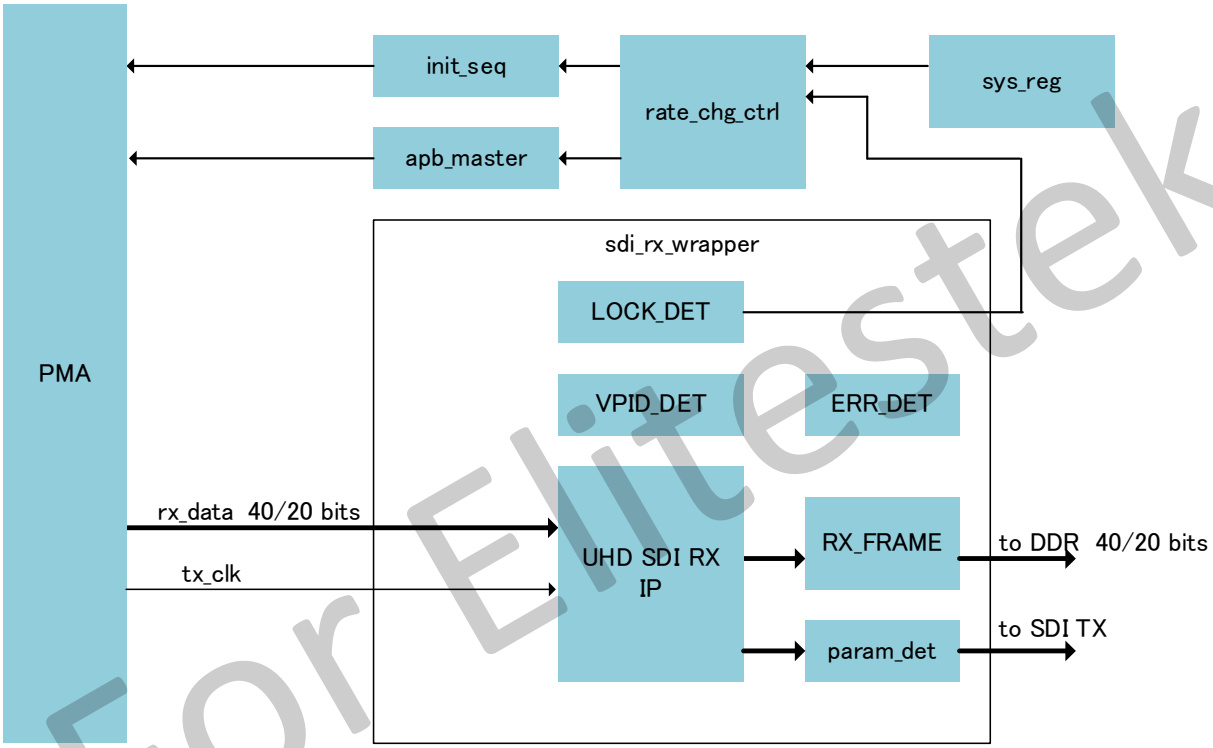

Figure 4-2 SDI RX Block Diagram

The functions of each block are as follows:

- **UHD SDI RX IP**

  CIS's UHD SDI RX IP.

- **RX_FRAME**

  Converts the decoded data into a format that can be written to DDR memory.

- **VPID_DET**

  Latches the received VPID.

- **LOCK_DET**

  Detects SDI LOCK. If the TRS Code is detected at a constant period, it is considered locked.

- **ERR_DET**

It detects CRC errors and Illegal Codes. If data other than the TRS Code is 10'h000, 10'h001, 10'h002, 10'h003, 10'h3FC, 10'h3FD, 10'h3FE, or 10'h3FF, it is considered an Illegal Code.

- **param_det**

  Detects the H total and V total of the received video data.

- **init_seq**

  The execution of the PMA Power-Up Sequence.

- **apb_master**

  Setting the specified rate(Preset) in the PMA.

- **rate_chg_ctrl**

  Control the apb_master. In Auto Mode (pg off), switch between four PMA presets until the sdi_rx_lock becomes high. In Manual Mode (pg on), set the specified PMA preset to the PMA.

Table 4-3 shows the SDI RX Mode and Clock Frequency.

Table 4-3 SDI RX Mode and clock frequency

SDI Mode	PMA Preset	rx_clk[MHz]	output data width
6G-SDI	5.94-148.5-40 bits	148.5	40 bits
3G-SDI	2.97-148.5-20 bits	148.5	20 bits
HD-SDI	1.485-148.5-20 bits	74.25	20 bits

Note : When the PMA reference clock is 1000/1001, the clock frequency in Table 4-2 will be 1000/1001.

4.3. Pattern generator

Figure 4-4 shows the block diagram of the pattern generator. Table 4-3 shows the SDI mode and the frequency of the vid_clk.

Table 4-4 Video clock frequency

SDI Mode	tx_clk	tx_core_clk	vid_ref_clk	i_vid_clk	vid_clk
6G-SDI	148.5	148.5	74.25	297	148.5
3G-SDI	148.5	148.5	74.25	297	148.5
HD-SDI	74.25	74.25	37.125	148.5	148.5

Note : When the PMA reference clock is 1000/1001, the clock frequency in Table 4-3 will be 1000/1001.

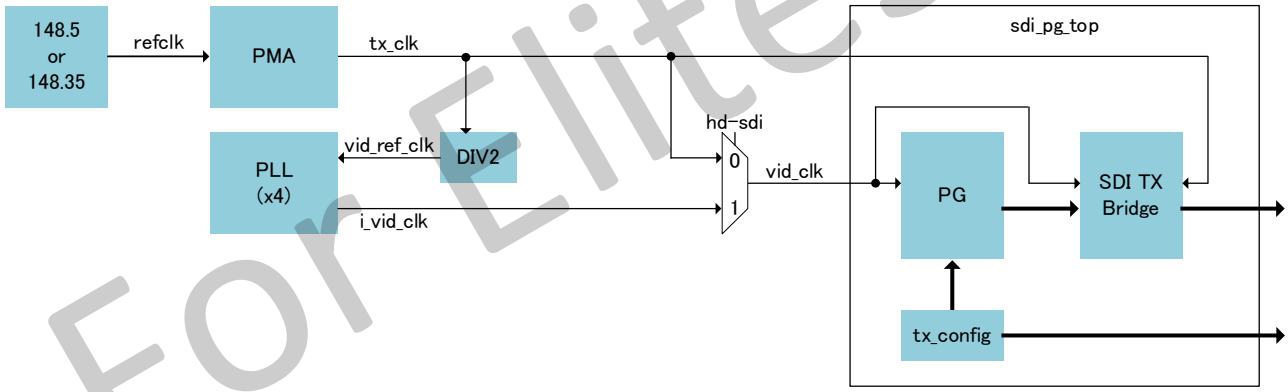

Figure 4-3 Pattern generator Block Diagram

The functions of each block are as follows:

- **PG**

  4K Color bar generation.

- **SDI TX Bridge**

  This is the bridge that converts to the SDI TX data format. For details, please refer to the SDI_TX_Bridge_specifications.

- **tx_config**

  The SDI TX Bridge settings and VPID will be generated according to the output SDI format.

4.4. Clock constraints

Figure 4-4 shows the clock system. In this reference design, the clocks listed below are used, and all of these clocks operate in asynchronous groups.

: io_peripheralClk (from pll)
: i_hdmi_clk (from pll)
: vid_clk (from pll or divider)
: rx_clk (from pma)
: tx_clk (from pma)

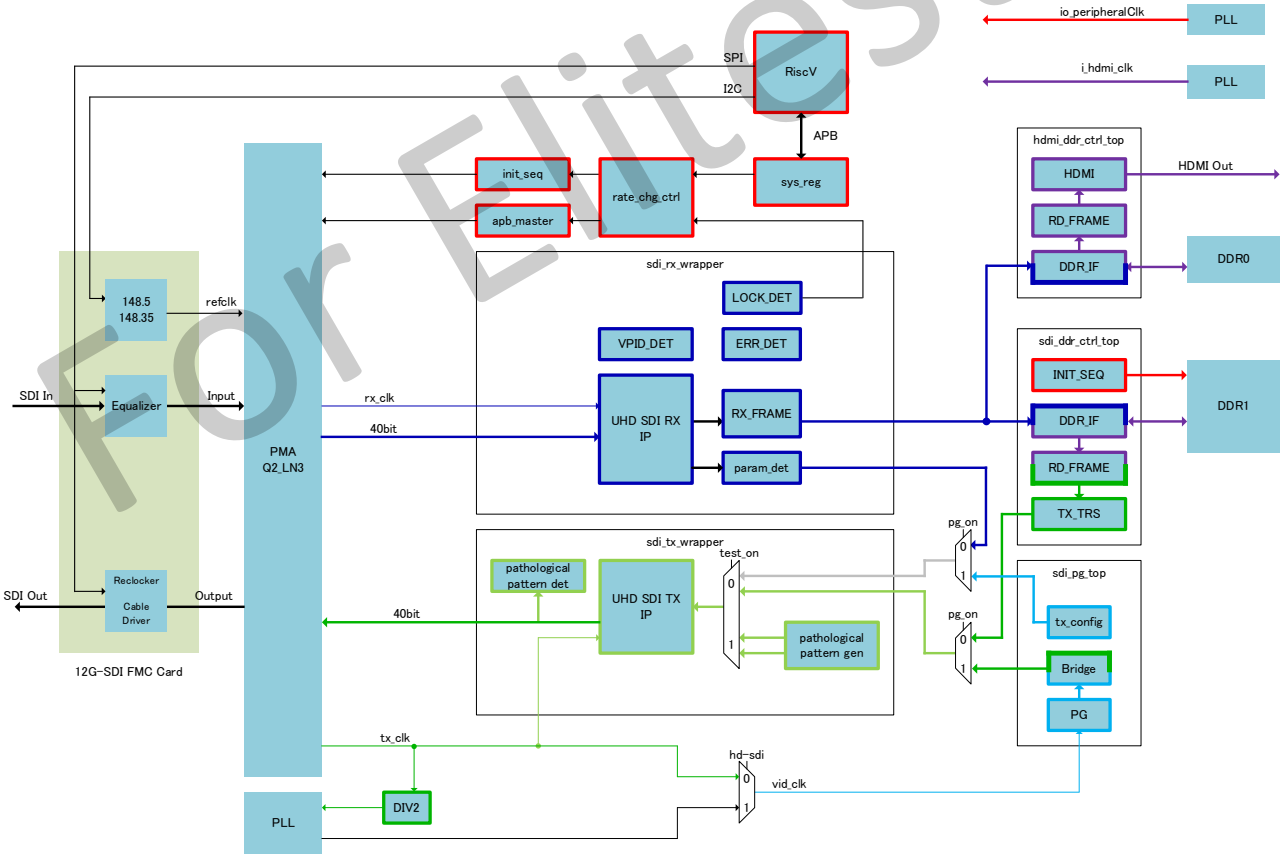

Figure 4-4 Clock system

5. Control Commands

Table 5-1 shows the commands supported by this reference design.

Table 5-1 Command list

Command	Description
r	Read the system registers
w	Write to the system register
rspi	Read 12G-SDI FMC Card registers
wspi	Write to 12G-SDI FMC Card registers
pg	Pattern generator enable/disable
fmt	SDI Output Format
refsel	Switch between reference clocks 148.5MHz and 148.35MHz.
vpid	View the VPID
status	View status
gerr	View SDI RX error counter
wpma	Write to the PMA registers
rpma	Read the PMA registers
dpma	Dump the PMA registers
test	Pathological pattern test on.
testsel	Pathological pattern selector.(6G-only)

5.1. System register access

- Read
  - Command: `r <address>`
  - Return: `<address> : <Hexadecimal> (Decimal)`
- Write
  - Command: `w <address> <value>`
  - Return: `<address> <= <Hexadecimal> (Decimal)`

5.2. 12G-SDI FMC Card register access

- Read
  - Command: `rspi <deviceIndex> <address>`
  - Return: `<address> : <Hexadecimal> (Decimal)`
- Write
  - Command: `wspi <deviceIndex> <address> <value>`
  - Return: `<deviceIndex>, <address> <= <Hexadecimal> (Decimal)`

Table 5-2 shows the index of the device.

Table 5-2 Index of device

Device	Index
TX Reclocker(M23145G)	0
TX Cable Driver(M23428G)	1
RX Equalizer(M23554G)	2

Note: Please request the register map (datasheet) for each device from the manufacturer's website.

5.3. Pattern generator enable/disable

- Enable
  - Command: `pg on`
  - Return: `Set Pattern Gen to [on]`
- Disable
  - Command: `pg off`
  - Return: `Set Pattern Gen to [off]`
- Get current state
  - Command: `pg`
  - Return: `Pattern Gen is [<Off/On>]`

5.4. SDI Output Format

- Set Format
  - Command: `fmt <Index>` ※ Please refer to Table 3-2 for the index
  - Return: `Set PG to <FormatName> (HDMI Out is <Not> Supported)`
- Get current format
  - Command: `fmt`
  - Return: `PG is <FormatName> (<Index>) (HDMI Out is <Not> Supported)`
- Get all format
  - Command: `fmt list`
  - Return: Table of formats

5.5. Switch reference clock

- Set to 1000/1000
  - Command: `refsel 0`
  - Return: `0 (1000/1000)`
- Set to 1000/1001

- Command: `resel 1`
- Return: `1 (1000/1001)`

5.6. View VPID

- View RX VPID
  - Command: `vpid rx`
  - Return: list of received VPID
- View TX VPID
  - Command: `vpid`
  - Syntax: `vpid tx`
  - Return: list of VPID set on TX

5.7. View Status

- Command: `status <all/pma/pg/rx/tx/hdmi/sys>`
  ※ If there are no arguments, it is treated as "`all`"
- Return: As shown in Table 5-3.

Table 5-3 status message

Log Message	Description
------- PMA ---------------------------	
Rate : 5.94 Gbps	Currently set rate.
Mode : Manual	Rate change mode.
Init Done : 1	State of the power sequence.
Sig Det : 1	Indicates whether RX SIGNAL DETECT is Low or High.
------- Pattern Generator --------------	
Mode : On	State of pattern generator.
Format : 2160P30 (No.18)	Current Pattern generator format.
HDMI Out : Supported	Indicates whether HDMI Out is supported
------- TEST ---------------------------	
Mode : Off	State of Pathological pattern generator.
CASE : -	EQ or Phase Lock signal.
------- SDI RX -------------------------	
Mode : 6G-SDI	SDI RX mode.
Align : 1	State of the align_done.
Align(Timeout): 0	State of the align time out.
Lock : 1	State of the sdi rx lock.
Rate : 1000/1001	Type of the sdi rx freq.

```
  Picture rate  : 30/1.001                  Picture Rate parsed from RX VPID
  Frame Counter : 132                       Frame Counter.(32bits)
  CRC Error     : 0                         Number of detected CRC errors.
                                            (Counters will be cleared after being read)
  Illegal Code  : 0                         Number of detected Illegal Code.
                                            (Counters will be cleared after being read)
  HDMI Out      : Supported
------- SDI TX -------------------------
  Mode          : 6G-SDI                    SDI TX Mode
  Data          : From PG                   SDI TX Data is From PG or SDI RX
------- HDMI -------------------------
  Connected     : Yes                       Indicates whether HDMI Connector Daughter Card is
                                            connected.
------- System -------------------------
 REFCLK SEL     : 1000/1000                 Indicates the type of input reference clock.
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!    Warning Message.
! Warning : Rx data rate and reference clock is mismatch        !
!         Please use cmd [refsel <0/1>] to change reference clock.!
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
```

5.8. View RX error counter

- Command: `gerr`
- Return: CRC Error Counter and Illegal Code Counter
  Counters will be cleared after "`gerr`" command.

5.9. PMA register access

- Read
  - Command: `rpma <address>`
  - Return: `<address> : <value>`
- Write
  - Command: `wpma <address> <value>`
  - Return: None
- Dump registers
  - Command: `dpma <address> <length>`
  - Return: list of <address> and <value>

5.10. Pathological pattern

- Test on
  - Command : test on
  - Return : Set Pathological Pattern to [on]
- Test off
  - Command : test off
  - Return : Set Pathological Pattern to [off]

5.11. Pathological pattern selector

- Phase locked loop test signal
  - Command : testsel phase
  - Return : Set Pathological Pattern to [phase locked loop test signal.]
- Equalizer test signal
  - Command : testsel eq
  - Return : Set Pathological Pattern to [equalizer test signal.]

6. System register map

System register map shown in Table 6-1.

Table 6-1 System register map

Address	Bits	BW	Name	R/W	Default	Description
0000	[0]	1	sdi_pma_pwr_on	RW	0	PMA Powe Seq reset_n. 0 : PMA is reset. 1 : Start Power Up sequence.
0004	[0]	1	sdi_pma_init_done	R	0	PMA Init done
0008	[3:0]	4	sdi_pma_init_state	R	0	PMA Init State
000C	[0]	1	sdi_pma_rx_pcs_rst_n	RW	0	PMA RX PCS RST_N
0010	[0]	1	sdi_pma_tx_pcs_rst_n	RW	0	PMA TX PCS RST_N
0014	[0]	1	sdi_pma_rx_sig_det	R	0	PMA RX SIG DET
0018	[0]	1	user_rx_rst	RW	1	
001C	[0]	1	user_tx_rst	RW	1	
0020	[0]	1	sdi_rx_align_done	R	0	sdi rx align done
0024	[0]	1	sdi_rx_align_timeout	R	0	sdi rx align timeout
0028	[0]	1	clear_align_done	RW	0	clear algin done
002C	[0]	1	sdi_rx_type	R	0	sdi rx type 0 : Normal 1 : 3G-LevelB, 6G type2
0030	[0]	1	sdi_rx_lock	R	0	sdi rx locked
0034	[0]	1	clear_rx_clock	RW	0	clear sdi rx lock
0038	[1:0]	2	sdi_rx_mode	R	0	SDI RX Mode
003C	[1:0]	2	sdi_rx_mode	R	0	SDI TX Mode
0100	[0]	1	vpid_cap_on	RW	0	vpid capture start(rising edge)
0104	[15:0]	16	vpid_capture_done	R	0	vpid capture done. [0] : ds1 field1 [1] : ds2 field1 [2] : ds3 field1 [3] : ds4 field1 [7:4] : Not Used [8] : ds1 field2 [9] : ds2 field2 [10] : ds3 field2 [11]: ds4 filed2

Address	Bits	BW	Name	R/W	Default	Description
						[15:12] : not used
0108	[31:0]	32	ds1_y_field1_vpid	R	0	
010C	[31:0]	32	ds2_y_field1_vpid	R	0	
0110	[31:0]	32	ds3_y_field1_vpid	R	0	
0114	[31:0]	32	ds4_y_field1_vpid	R	0	
0128	[31:0]	32	ds1_y_field2_vpid	R	0	
012C	[31:0]	32	ds2_y_field2_vpid	R	0	
0130	[31:0]	32	ds3_y_field2_vpid	R	0	
0134	[31:0]	32	ds4_y_field2_vpid	R	0	
0148	[10:0]	11	ds1_y_field1_vpidln	R	0	
014C	[10:0]	11	ds2_y_field1_vpidln	R	0	
0150	[10:0]	11	ds3_y_field1_vpidln	R	0	
0154	[10:0]	11	ds4_y_field1_vpidln	R	0	
0168	[10:0]	11	ds1_y_field2_vpidln	R	0	
016C	[10:0]	11	ds2_y_field2_vpidln	R	0	
0170	[10:0]	11	ds3_y_field2_vpidln	R	0	
0174	[10:0]	11	ds4_y_field2_vpidln	R	0	
0188	[0]	1	ds1_y_field1_vpidcs_err	R	0	
018C	[0]	1	ds2_y_field1_vpidcs_err	R	0	
0190	[0]	1	ds3_y_field1_vpidcs_err	R	0	
0194	[0]	1	ds4_y_field1_vpidcs_err	R	0	
01A8	[0]	1	ds1_y_field2_vpidcs_err	R	0	
01AC	[0]	1	ds2_y_field2_vpidcs_err	R	0	
01B0	[0]	1	ds3_y_field2_vpidcs_err	R	0	
01B4	[0]	1	ds4_y_field2_vpidcs_err	R	0	
0200	[0]	1	ddr_write_on	RW	0	sdi and hdmi ddr write on
0204	[0]	1	ddr_read_on	RW	0	sdi and hdmi ddr read on
0208	[0]	1	ddr_tx_force_mode	RW	0	force the sdi tx and hdmi tx data to {force_c, force_y}
020C	[9:0]	10	ddr_tx_force_y	RW	198	
0210	[9:0]	10	ddr_tx_force_c	RW	300	
0214	[15:0]	16	sdi_rx_xtotal	R	0	xtotal of sdi rx
0218	[15:0]	16	sdi_rx_xactive	R	0	xactive of sdi rx
021C	[15:0]	16	sdi_rx_ytotal	R	0	ytotal of sdi rx
0220	[15:0]	16	sdi_rx_yactive	R	0	yactive of sdi rx

Address	Bits	BW	Name	R/W	Default	Description
0300	[0]	1	force_rate_mode	RW	0	force PMA rate Mode 0 : Switch automatically 1 : Switch manually.
0304	[1:0]	2	force_rate	RW	1	PMA Rate 2'b00 : 1.485 Gbps (1.485 - 148.5 - 20 bits) 2'b01 : 2.97 Gbps (2.97 - 148.5 - 20 bits) 2'b10 : 5.94 Gbps (5.94 - 148.5 - 40bits)
0308	[0]	1	force_rate_req	RW	0	Change request (Rising edge)
030C	[0]	1	rate_change_done	R	0	
0310	[1:0]	2	current_rate	R	3	Current pma rate
0314	[7:0]	8	pg_mode	RW	0	Pattern mode: 0 : 1080i50 1 : 1080i59.94 2 : 1080i60 3 : 1080p23.98 4 : 1080p24 5 : 1080p25 6 : 1080p29.97 7 : 1080p30 8 : 1080p50B 9 : 1080p50A 10 : 1080p59.94B 11 : 1080p59.94A 12 : 1080p60B 13 : 1080p60A 14 : 2160P23.98 15 : 2160P24 16 : 2160P25 17 : 2160P29.97 18 : 2160p30
0318	[0]	1	pg_on	RW	0	Pattern generator on
0410	[0]	1	rx_rate_1001	R	0	0 : rx data rate type is

Address	Bits	BW	Name	R/W	Default	Description
						1000/1000 1 : rx data rate type is 1000/1001
0414	[21:0]	22	rx_rate_period	R	0	The counter value of rx_core_clk over 10 ms.
0418	[0]	1	rx_crc_error_cnt_lat	RW	0	Latch the CRC Error counter. latch on register value change.
041C	[0]	1	rx_crc_error_cnt_clr	RW	0	Clear the CRC Error Counter. Clear on register value change.
0420	[31:0]	32	rx_crc_error_cnt	R	0	CRC Error Count. Max : 'd1020 (=255x4)
0424	[0]	1	rx_illegal_code_cnt_lat	RW	0	Latch the Illegal code counter. latch on register value change.
0428	[0]	1	rx_illegal_code_cnt_clr	RW	0	Clear the Illegal code counter. Clear on register value change.
042C	[31:0]	32	rx_illegal_code_cnt	R	0	Illegal Code Counter.
0430	[31:0]	32	rx_changed_vpid	R	0	The latest RX VPID(DS1)
0440	[0]	1	rx_frame_cnt_lat	RW	0	Latch the Frame counter. latch on register value change.
0444	[0]	1	rx_frame_cnt_clr	RW	0	Clear the Frame counter. Clear on register value change.
0448	[31:0]	32	rx_frame_cnt	R	0	Frame counter.
0500	[5:0]	6	led_en	RW	3F	Led output enable.
0504	[0]	1	hdmi_int	R	0	HDMI_INT from FMC Card. 0 : HDMI is connect 1 : HDMI is not connect.
0600	[1:0]	2	fmc_spi_sel	RW	0	12-SDI FMC Card SPI Selector 2'b00 : CH0 (used) 2'b01 : CH1 2'b10 : CH2

Address	Bits	BW	Name	R/W	Default	Description
						2'b11 : CH3
0700	[0]	1	apb_start	RW	0	apb access start.
0704	[0]	1	apb_pwrite	RW	0	apb write
0708	[23:0]	24	apb_paddr	RW	0	apb address
070C	[31:0]	32	apb_pwdata	RW	0	apb wdata
0710	[31:0]	32	apb_prdata	R	0	apb rdata
0714	[0]	1	apb_busy	R	0	apb is busy
0800	[31:0]	32	ds1_tx_vpid	R	0	TX VPID DS1
0804	[31:0]	32	ds2_tx_vpid	R	0	TX VPID DS2
0808	[31:0]	32	ds3_tx_vpid	R	0	TX VPID DS3
080C	[31:0]	32	ds4_tx_vpid	R	0	TX VPID DS4
0820	[10:0]	11	ds1_tx_vpid_ln_f1	R	0	TX VPID LN Field1 DS1
0824	[10:0]	11	ds2_tx_vpid_ln_f1	R	0	TX VPID LN Field1 DS2
0828	[10:0]	11	ds3_tx_vpid_ln_f1	R	0	TX VPID LN Field1 DS3
082C	[10:0]	11	ds4_tx_vpid_ln_f1	R	0	TX VPID LN Field1 DS4
0840	[10:0]	11	ds1_tx_vpid_ln_f2	R	0	TX VPID LN Field2 DS1
0844	[10:0]	11	ds2_tx_vpid_ln_f2	R	0	TX VPID LN Field2 DS2
0848	[10:0]	11	ds3_tx_vpid_ln_f2	R	0	TX VPID LN Field2 DS3
084C	[10:0]	11	ds4_tx_vpid_ln_f2	R	0	TX VPID LN Field2 DS4
0900	[0]	1	pathological_pattern_on	RW	0	Pathological pattern enable
0904	[0]	1	eq_pattern	RW	0	0 : phase locked test 1 : equalizer test
1000	[7:0]	8	version	R	01	Version of design.

7. 12G-FMC Card Pin Table

Table 7-1 shows the pin assignment for the 12G-FMC Card and TJ375N1156X J15 (FMCB).

Table 7-1 12G-FMC Card and FMCB Pin assignment

12G-SDI FMC Card			TJ375N1156X Board (FMCB)		
J10 Pin	**schematics name**	**VITA 57.1**	**schematics name**	**FPGA Pin**	**Pin Name**
SDI Differential Pairs					
C2	CH0_SDI_P	DP0_C2M_P	FMCB_DP0_C2M_P	C23	Q2_TXDP3
C3	CH0_SDI_N	DP0_C2M_N	FMCB_DP0_C2M_N	D23	Q2_TXDN3
A22	CH1_SDI_P	DP1_C2M_P	FMCB_DP1_C2M_P	C21	Q2_TXDP2
A23	CH1_SDI_N	DP1_C2M_N	FMCB_DP1_C2M_N	D21	Q2_TXDN2
A26	CH2_SDI_P	DP2_C2M_P	FMCB_DP2_C2M_P	C19	Q2_TXDP1
A27	CH2_SDI_N	DP2_C2M_N	FMCB_DP2_C2M_N	D19	Q2_TXDN1
A30	CH3_SDI_P	DP3_C2M_P	FMCB_DP3_C2M_P	C17	Q2_TXDP0
A31	CH3_SDI_N	DP3_C2M_N	FMCB_DP3_C2M_N	D17	Q2_TXDN0
C6	CH0_SDO_P	DP0_M2C_P	FMCB_DP0_M2C_P	A24	Q2_RXDP3
C7	CH0_SDO_N	DP0_M2C_N	FMCB_DP0_M2C_N	B24	Q2_RXDN3
A2	CH1_SDO_P	DP1_M2C_P	FMCB_DP1_M2C_P	A22	Q2_RXDP2
A3	CH1_SDO_N	DP1_M2C_N	FMCB_DP1_M2C_N	B22	Q2_RXDN2
A6	CH2_SDO_P	DP2_M2C_P	FMCB_DP2_M2C_P	A20	Q2_RXDP1
A7	CH2_SDO_N	DP2_M2C_N	FMCB_DP2_M2C_N	B20	Q2_RXDN1
A10	CH3_SDO_P	DP3_M2C_P	FMCB_DP3_M2C_P	A18	Q2_RXDP0
A11	CH3_SDO_N	DP3_M2C_N	FMCB_DP3_M2C_N	B18	Q2_RXDN0
SPI and I2C Signals					
D17	F_SPI_MOSI	LA13_P	FMCB_LA13_P	V27	2D_GPIOT_P_41
D18	F_SPI_MISO	LA13_N	FMCB_LA13_N	V26	2D_GPIOT_N_41
D20	F_SPI_SCLK	LA17_CC_P	FMCB_LA17_P	AB28	2D_GPIOT_P_43
D11	F_SPI_S0	LA05_P	FMCB_LA5_P	T32	2C_GPIOT_P_36_CLK19_P
D9	F_SPI_S1	LA01_CC_N	FMCB_LA1_CC_N	N32	2E_GPIOT_N_59
D15	F_SPI_CS1	LA09_N	FMCB_LA9_N	V28	2D_GPIOT_N_49
D14	F_SPI_CS2	LA09_P	FMCB_LA9_P	U28	2D_GPIOT_P_49_EXTFB
D12	F_SPI_CS3	LA05_N	FMCB_LA5_N	U32	2C_GPIOT_N_36_CLK19_N
H13	F_CTL_I2C_SCL	LA07_P	FMCB_LA7_P	R32	2E_GPIOT_P_51
H14	F_CTL_I2C_SDA	LA07_N	FMCB_LA7_N	R31	2E_GPIOT_N_51

12G-SDI FMC Card			TJ375N1156X Board (FMCB)		
J10 Pin	**schematics name**	**VITA 57.1**	**schematics name**	**FPGA Pin**	**Pin Name**
C30	NONE	SCL	FMCB_SCL	L24	TR2_GPIOR_106
C31	NONE	SDA	FMCB_SDA	L22	TR2_GPIOR_103
Video Clocks					
H4	F_CLKOUT1_P	CLK0_M2C_P	FMCB_CLK0_M2C_P	R26	2D_GPIOT_P_37_CLK20_P
H5	F_CLKOUT1_N	CLK0_M2C_N	FMCB_CLK0_M2C_N	T26	2D_GPIOT_P_37_CLK20_N
G2	F_CLKOUT4_P	CLK1_M2C_P	FMCB_CLK1_M2C_P	Y26	2D_GPIOT_P_38_CLK21_P
G3	F_CLKOUT4_N	CLK1_M2C_N	FMCB_CLK1_M2C_N	AA27	2D_GPIOT_N_38_CLK21_N
D4	F_CLKOUT2_P	GBTCLK0_M2C_P	FMCB_GBTCLK_M2C_P	G18	Q2_REFCLK0_P
D5	F_CLKOUT2_N	GBTCLK0_M2C_N	FMCB_GBTCLK_M2C_N	F18	Q2_REFCLK0_N
B20	F_CLKOUT3_P	GBTCLK1_M2C_P		G16	Q2_REFCLK1_P
B21	F_CLKOUT3_N	GBTCLK1_M2C_N		F16	Q2_REFCLK1_N
G15	F_FOUT	LA12_P	FMCB_LA12_P	M33	2E_GPIOT_P_58
G12	F_VOUT	LA08_P	FMCB_LA8_P	P34	2E_GPIOT_P_56
G13	F_HOUT	LA08_N	FMCB_LA8_N	P33	2E_GPIOT_N_56
G21	F_FIN	LA20_P	FMCB_LA20_P	T27	2D_GPIOT_P_47
G18	F_VIN	LA16_P	FMCB_LA16_P	T31	2C_GPIOT_P_35_CLK18_P
G19	F_HIN	LA16_N	FMCB_LA16_N	T30	2C_GPIOT_P_35_CLK18_N
G9	F_FOUT1	LA03_P	FMCB_LA3_P	R34	2E_GPIOT_P_54
G6	F_FOUT2	LA00_CC_P	FMCB_LA0_CC_P	L31	2E_GPIOT_P_62_PLLIN0
G7	F_FOUT3	LA00_CC_N	FMCB_LA0_CC_N	M30	2E_GPIOT_N_62
G10	F_FOUT4	LA03_N	FMCB_LA3_N	R33	2E_GPIOT_N_54
Control and Miscellaneous Signals					
C10	F_XALARM_TX_CH0	LA06_P	FMCB_LA6_P	T29	2C_GPIOT_P_34_CLK17_P
C11	F_XALARM_TX_CH1	LA06_N	FMCB_LA6_N	U30	2C_GPIOT_N_34_CLK17_N
C14	F_XALARM_TX_CH2	LA10_P	FMCB_LA10_P	Y28	2D_GPIOT_P_46
C15	F_XALARM_TX_CH3	LA10_N	FMCB_LA10_N	Y27	2D_GPIOT_N_46
H16	F_XALARM_RX_CH0	LA11_P	FMCB_LA11_P	P31	2E_GPIOT_P_55
H17	F_XALARM_RX_CH1	LA11_N	FMCB_LA11_N	P30	2E_GPIOT_N_55
H19	F_XALARM_RX_CH2	LA15_P	FMCB_LA15_P	P29	2E_GPIOT_P_52
H20	F_XALARM_RX_CH3	LA15_N	FMCB_LA15_N	R29	2E_GPIOT_N_52
G30	F_CH1_DIR	LA29_P	FMCB_LA29_P	N31	2E_GPIOT_P_57
G33	F_CH2_DIR	LA31_P			

12G-SDI FMC Card			TJ375N1156X Board (FMCB)		
J10 Pin	**schematics name**	**VITA 57.1**	**schematics name**	**FPGA Pin**	**Pin Name**
C18	F_CH3_DIR	LA14_P	FMCB_LA14_P	W26	2D_GPIOT_P_44
G16	F_INIT	LA12_N	FMCB_LA12_N	N33	2E_GPIOT_N_58
H7	F_NO_REF	LA02_P	FMCB_LA2_P	T34	2E_GPIOT_P_53
H8	F_NO_ALIGN	LA02_N	FMCB_LA2_N	U34	2E_GPIOT_N_53
H10	F_NO_LOCK	LA04_P	FMCB_LA4_P	U33	2C_GPIOT_P_33_CLK16_P
H1	Not connected	VREF_A_M2C			
K1	Not connected	VREF_B_M2C			
D1	Not connected	PG_C2M	FMCB_C2M_PG	N25	TR1_GPIOR_100
F1	10k to VCC_3V3	PG_M2C			
H2	0 ohm to GND	PRSNT_M2C_N	FMCB_PRSNT	K24	TR2_GPIOR_102
D29	Not connected	TCK	TCK_FMCB		
D30	0 ohm to TDO	TDI	TDO_FPGA	J6	BR4_TDO
D31	0 ohm to TDI	TDO	TDO_FT		
D33	Not connected	TMS	TMS_FMCB		
D34	Not connected	TRST_N			
C34	GA0	GA0	FMCB_GA0	L23	TR2_GPIOR_107
D35	GA1	GA1	FMCB_GA1	K26	TR2_GPIOR_108
J39	Not connected	VIO_B_M2C			
K40	Not connected	VIO_B_M2C			
Power					
C35		12P0V	VCC_12V		
C37		12P0V	VCC_12V		
E39		VADJ	FMC_VADJ		
F40		VADJ	FMC_VADJ		
G39		VADJ	FMC_VADJ		
H40		VADJ	FMC_VADJ		
D32		3P3VAUX	VCC_3V3		
D40		3P3V	VCC_3V3		
C39		3P3V	VCC_3V3		
D36		3P3V	VCC_3V3		
D38		3P3V	VCC_3V3		

8. Revision History

8.1. Design History

Date	Version	Descriptions
2025-03-21	01	First edition

8.2. Document History

Date	Version	Descriptions
2025-03-21	1.0	First edition