CIS

UHD SDI RX Specifications For Elitestek

Revision 1.0

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2025-03-21

Contents

1. Introduction

UHD SDI RX is the IP of SDI(Serial digital Interface) receiver. The IP is designed based on applicable SMPTE(Society of Motion Picture and Television Engineers) standards and supports HD-SDI, 3G-SDI Level-A, 3G-SDI Level-B, 6G-SDI type1 and type2.

1.1. Features

UHD SDI RX supports the following standards:

- SMPTE ST 292-1 (HD-SDI)
- SMPTE ST 424 (3G-SDI)
- SMPTE ST 425 (3G Level-A/B)
- SMPTE ST 2081-1 (6G-SDI)
- SMPTE ST 352 (Payload Identification Codes)

UHD SDI RX supports the following functions:

- Descrambling and NRZI decoding
- Extraction of Line Number(LN)
- Extraction of timing reference signals(TRS)
- CRC checker
- Extraction of Video Payload Identification (VPID)
- Removal of Sync-bit from timing reference words in 6G-SDI standard
- Dynamically changing SDI modes(6G-SDI, 3G/HD-SDI).

1.2. Overview

Figure1-1 shows the system configuration including UHD SDI RX. Table1-1 shows the input data width and input clock frequency for each SDI mode.

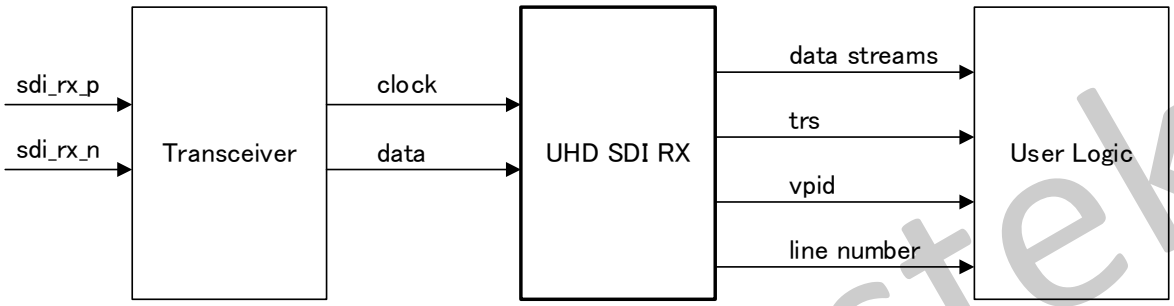


Figure 1-1 System block diagram

Table 1-1 Data Rate and Data Width

SDI Rate	Data Width	Frequency
6G-SDI(5940Mbps)	40	148.5MHz
3G-SDI(2970Mbps)	20	148.5MHz
HD-SDI(1485Mbps)	20	74.25MHz

2. Interface

2.1. Configuration Parameter

Table 2-1 shows the configurable parameters of the IP.

Table 2-1 Configuration Parameters

Name	Type	Range	Descriptions
DS_NUM	integer	2,4(default)	Maximum number of output data streams. (Other configurations are not supported) 2 : 2 Data Stream(Total 20bits) Only supports 3G/HD-SDI 4 : 4 Data Stream(Total 40bits) Supports 6G-SDI, 3G/HD-SDI

2.2. Ports

Table 2-2 I/O ports

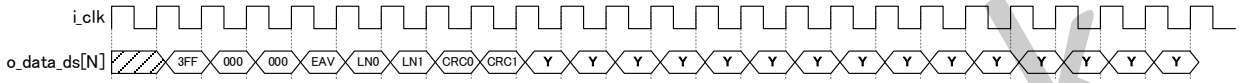
Name	Width[1]	I/O	Description
i_clk	1	I	Receive clock. HD-SDI : 74.25(/1.001)MHz 3G/6G-SDI: 148.5(/1.001)MHz
i_rst	1	I	Synchronous reset.(Active High)
i_sdi_mode	2	I	SDI Mode 2'b00 : 3G/HD-SDI 2'b01 : 6G-SDI
i_rx_data[N*10-1:0]	N*10	I	Receive Data。 Data width according to the SDI mode as follows: ・6G-SDI : [39:0] ・3G/HD-SDI : [19:0]
o_data_ds[N-1:0][9:0]	N*10	O	Data Streams Output. [0][9:0] : Data Stream1 [1][9:0] : Data Stream2 … [N-1][9:0] : Data StreamN Active data streams according to the SDI mode as follows: ・6G-SDI : Data Stream 1 ~ 3 ・3G/HD-SDI : Data Stream 1 ~ 2

Name	Width[1]	I/O	Description
o_ln[N-1:0][10:0]	N*11	O	Line Number [0][10:0] : Line Number of Data Stream1 [1][10:0] : Line Number of Data Stream2 … [N-1][10:0] : Line Number of Data StreamN
o_ln_valid[N-1:0]	N	O	VALID of Line Number
o_vpid_y[N-1:0][31:0]	N*32	O	VPID from Y channel[2] [7:0] Byte1, [15:8] Byte2, [23:16] Byte3, [31:24] Byte4 [0][31:0] : VPID from Data Stream1 [1][31:0] : VPID from Data Stream2 … [N-1][31:0] : VPID from Data StreamN
o_vpid_y_valid[N-1:0]	N	O	VALID of VPID from Y channel[2]
o_vpid_y_cs_error[N-1:0]	N	O	CheckSum Error of VPID from Y channel[2]
o_vpid_c[N-1:0][31:0]	N*32	O	VPID from C channel[2] [7:0] Byte1, [15:8] Byte2, [23:16] Byte3, [31:24] Byte4 [0][31:0] : VPID from Data Stream1 [1][31:0] : VPID from Data Stream2 … [N-1][31:0] : VPID from Data StreamN ※ Active Only on 3G Level-B, 6G type2
o_vpid_c_valid[N-1:0]	N	O	VALID of VPID from C channel[2]
o_vpid_c_cs_error[N-1:0]	N	O	CheckSum Error of VPID from C channel[2]
o_trs	1	O	TRS Flag
o_sav	1	O	SAV Flag
o_eav	1	O	EAV Flag
o_crc_error[N-1:0]	N	O	CRC Error
o_rx_type	1	O	Type of receive 1'b0 : 3G Level-A, 6G Type1 1'b1 : 3G Level-B, 6G Type2
o_align_done	1	O	Word align is done. (Active High)
o_align_timeout	1	O	Time out of word align High when the reference code cannot be detected within a period of 32,768 cycles.
i_clear_align_done	1	I	Clear o_align_done and o_align_timeout

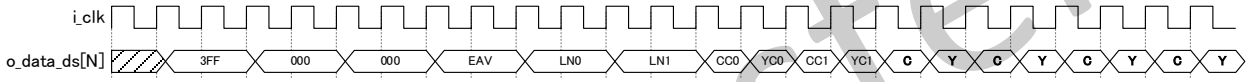
Name	Width[1]	I/O	Description
			(Clear at rising edge of i_clear_align_done)
o_version	8	O	Version of IP

[1]: N is DS_NUM.

[2]: Y channel data at 3G-SDI Level-A and 6G-SDI Type1:



C channel data at 3G-SDI Level-B and 6G-SDI Type2 :



3. Function Description

3.1. Top Diagram

Table 3-1 shows the supported SDI modes based on DS_NUM. Figure 3-1 shows the TOP Block Diagram with DS_NUM set to 8.

Table 3-1 Supported SDI Mode

	i_sdi_mode[1:0]	
DS_NUM	**2'b01**	**2'b00**
4	6G-SDI	3G/HD-SDI
2		3G/HD-SDI

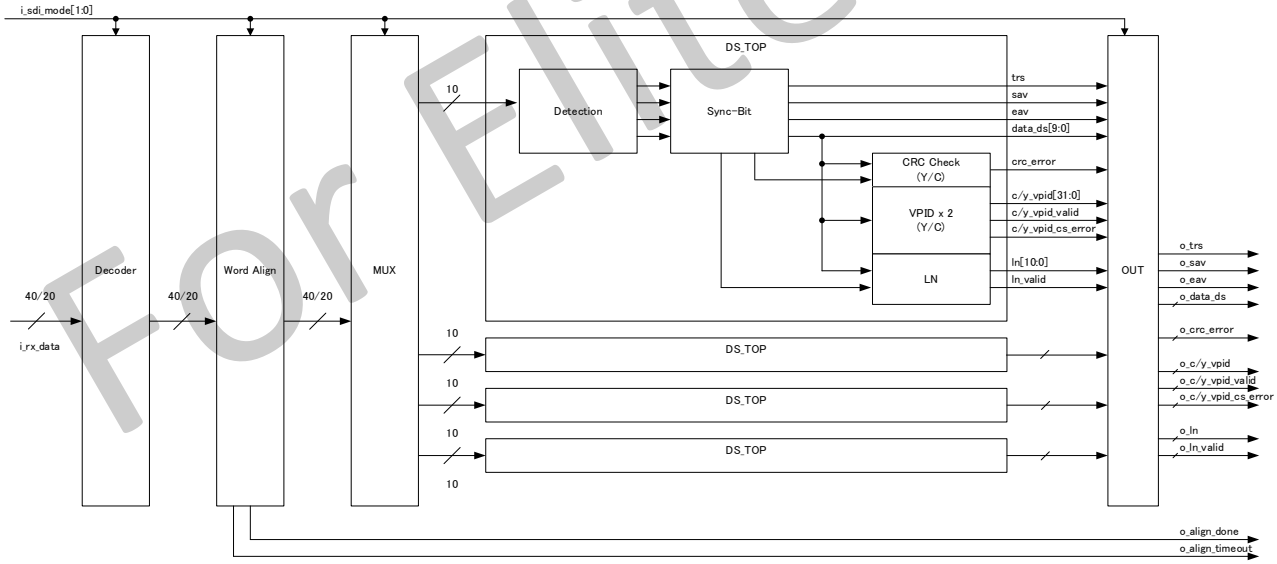


Figure 3-1 Top Diagram (DS_NUM=4)

3.2. Decoder

Decoder performs the descrambling and NRZI decoding on the receive data. The decoding is performed as per the polynomials specified in the SMPTE specification.

$$G_1(X) = X^9 + X^4 + 1$$

$$G_2(X) = X + 1$$

3.3. Word Align

The word boundary alignment is performed by searching the timing reference code("3FF 000 000") in the decoded data and outputs the data in a 10-bit data stream format. When the timing reference code is detected, o_align_done becomes High. If the timing reference code is not detected for a long period (32,768 cycles), o_align_timeout becomes High and automatically goes Low when the timing reference code is detected.

3.4. Mux

MUX performs the 10-bit multiplex of data streams as defined in the SMPTE specification.

3.5. Detection

Detect the TRS/SAV/EAV from the Data Stream and determine whether it is Type 1 (Level-A) or Type 2 (Level-B).

3.6. Sync-Bit

In 6G-SDI mode, removal of Sync-Bit is performed. Convert 10'h002 to 10'h000 and 10'h3FD to 10'h3FF.

3.7. CRC Check

Calculate the 18-bit CRC defined by the SMPTE standards and compare it with the received CRC packets (CR0/CR1). If the calculated CRC differs from the received CRC, o_crc_error becomes High. As shown in Figure 3-2, o_crc_error is a pulse signal that becomes High at the timing when the CRC packet is output.

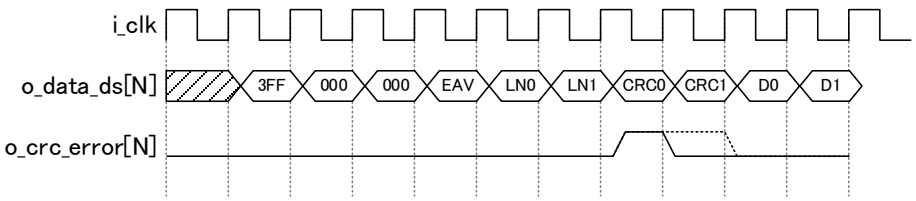


Figure 3-2 o_crc_error Timing

The CRC generation polynomial is as follows:

$$CRC(X) = X^{18} + X^5 + X^4 + 1$$

3.8. VPID

Detect VPID packets compliant with SMPTE ST 352. Output the 4-byte VPID at the timing when o_vpid_y/c_valid is High. Additionally, calculate the checksum from the received VPID and compare it with the received checksum. If the checksums differ, o_vpid_y/c_cs_error becomes High.

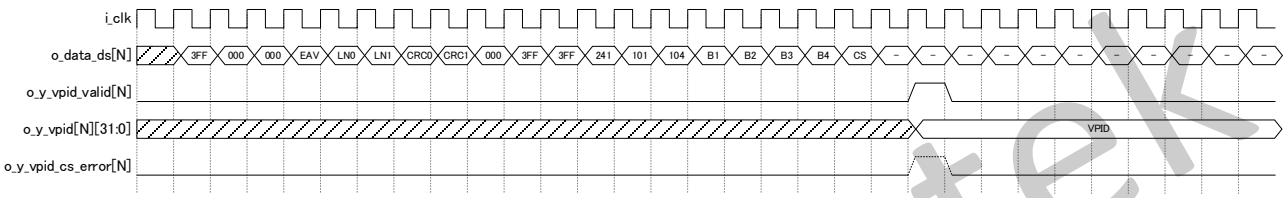


Figure 3-3 VPID Timing for 3G-SDI Level-A, 6G-SDI Type1

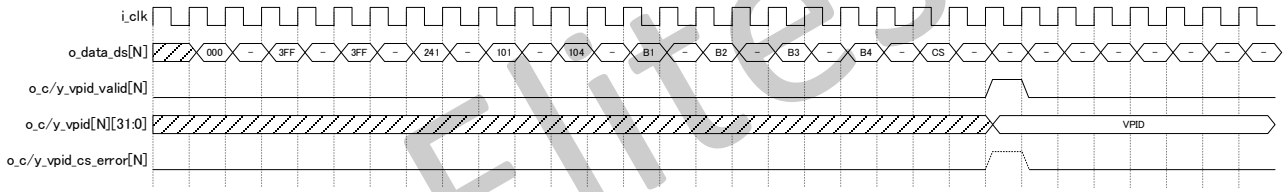


Figure 3-4 VPID Timing for 3G-SDI Level-B, 6G-SDI Type2

3.9. LN(Line Number)

Detect LN0 and LN1 packets from the data stream and decodes the line number data from LN0 and LN1.

4. Timing Diagrams

4.1. 3G-SDI Level-A, 6G-SDI type1

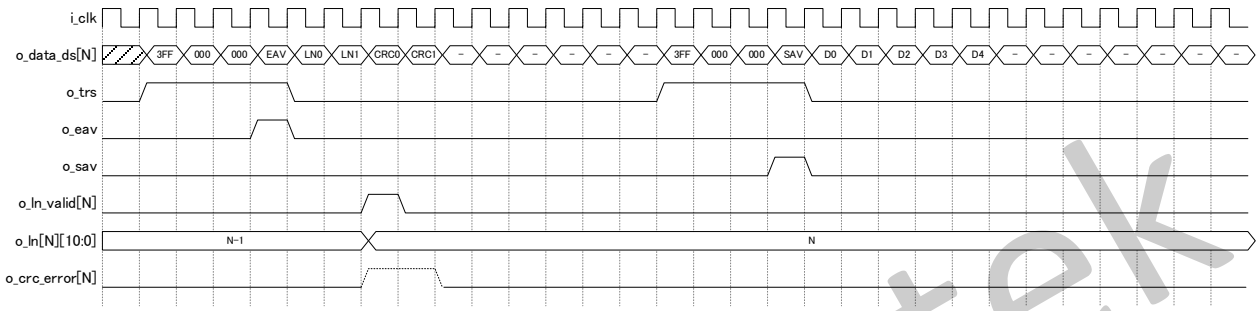


Figure 4-1 3G Level-A, 6G type1 output timing

4.2. 3G-SDI Level-B, 6G-SDI type 2

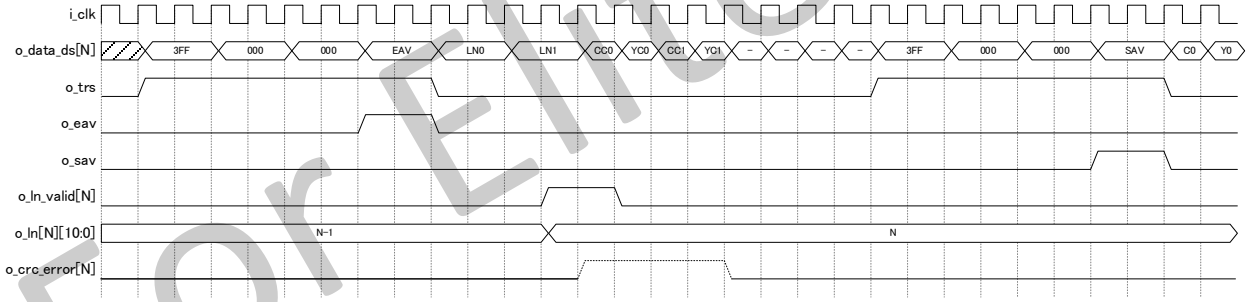


Figure 4-2 3G Level-B, 6G type2 output timing

5. Resource

Table5-1[1]shows the resource usage for each SDI mode.

Table 5-1 resource usage

SDI Standard	DS_NUM	DW[2]	FFs	SRLs	ADDs	LUTs	COMB4s	RAMs	DSPs	Fmax [MHz]
6G-SDI	4	40	1992	16	91	3386	0	0	0	212
3G(HD)-SDI	2	20	991	8	53	1150	0	0	0	186

[1]: Synthesis result of Efinity 2024.2 (TJ375N1156X).

[2]: Rx Data width

6. Revision History

6.1. IP History

Date	Version	Descriptions
2025-03-21	01	First edition

6.2. Document History

Date	Version	Descriptions
2025-03-21	1.0	First edition