CIS

SDI TX Bridge Specifications

Revision 1.0

CIS Corporation

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Contents

1. Introduction

The SDI TX Bridge is a module that converts 4K YCbCr 422 video stream data into SDI data format. It performs various conversions such as 2SI (2 sample interleave) conversion, converting from 4K to FHD, and mapping to 3G-Level B, among other format transformations for the video data from the user logic.

1.1. Features

- Conversion to 12G-SDI 4K 2SI format
- Conversion to 6G-SDI type2 format
- Conversion to FHD from 4K
- Conversion to 3G-Level A and 3G-Level B
- Conversion to HD-SDI interlaced format

1.2. Overview

Figure 1-1 shows a system that incorporates the SDI TX Bridge. The video signal output from the User Logic is connected to the UHD SDI TX IP via the SDI TX Bridge. The UHD SDI TX is a circuit that performs data encoding according to the SMPTE standard, provided by CIS. The encoded SDI transmission data is then output through the FPGA's transceiver.

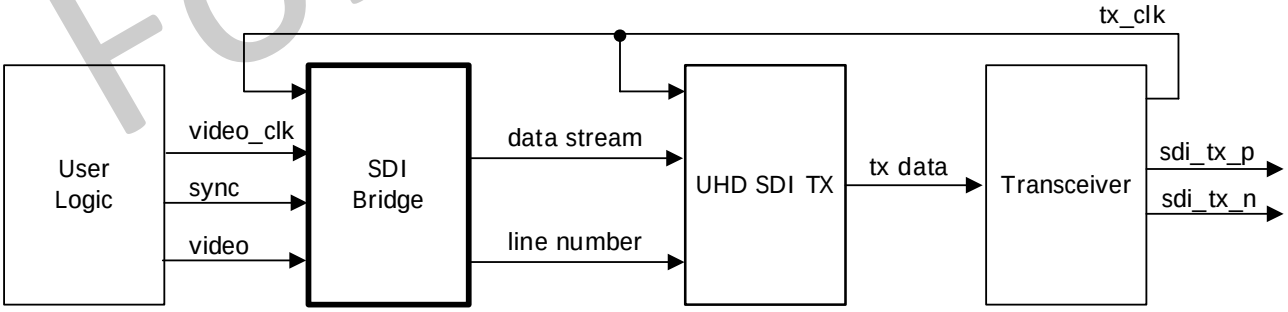

Figure 1-1 System Block Diagram

2. Interface

2.1. Ports

Table 2-1 shows the ports of the SDI TX Bridge.

Table 2-1 I/O Ports

Name	Width	I/O	Description
i_vid_clk	1	I	Video clock. (148.5 MHz) Must be the same Oscillation Source as i_txclk.
i_vid_rst	1	I	Synchronous reset of i_vid_clk.(Active High)
i_txclk	1	I	Transmit clock. 12G-SDI/6G-SDI/3G-SDI：148.5 MHz HD-SDI：74.25MHz
i_txrst	1	I	Synchronous reset of i_txclk.(Active High)
i_vd	1	I	frame start.
i_hd	1	I	line start.
i_field	1	I	frame field.
i_y	10*4	I	input data Y.
i_c	10*4	I	input data CbCr.
ip_mode_hd	1	I	FHD mode enable.
ip_mode_interlace	1	I	Interlaced enable.
ip_level_b	1	I	Level-B enable.
ip_fps_sel	4	I	Frame rate. 0x0:60fps, 0x1:59.94fps, 0x2:50fps, 0x4:30fps, 0x5:29.97fps, 0x6:25fps, 0x8:24fps, 0x9:23.98fps
o_data_ds	8*10	O	Output data stream.
o_version	8	O	Version of IP

3. Function Description

3.1. Top Diagram

Figure 3-1 shows the block diagram of the SDI TX Bridge. The functions of each block are described below.

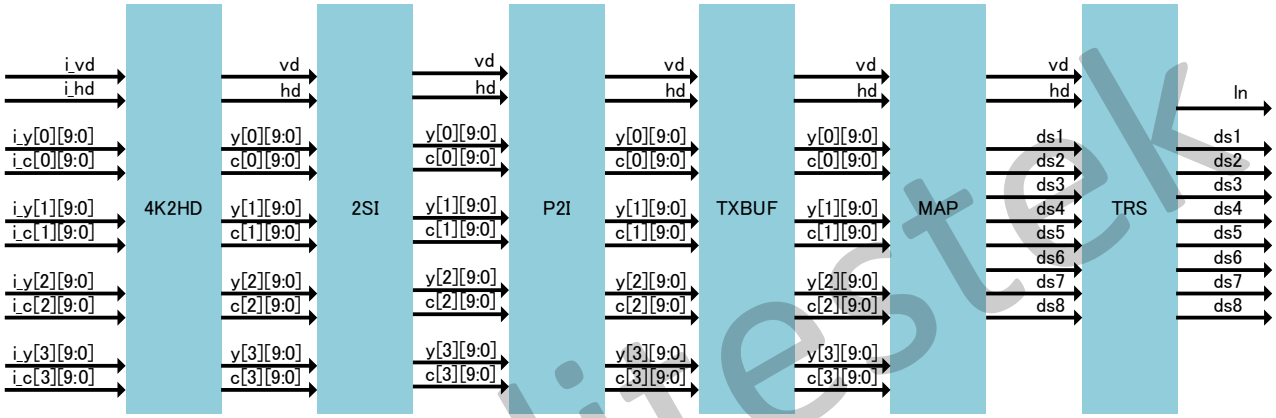

Figure 3-1 Top Block Diagram

3.2. 4K2HD

The 4K2HD converts a 4K (3840x2160) image to FHD (1920x1080) by scaling it down.

3.3. 2SI

In this block, as shown in Figure 3-2, the data is converted into a 2 sample interleave format.

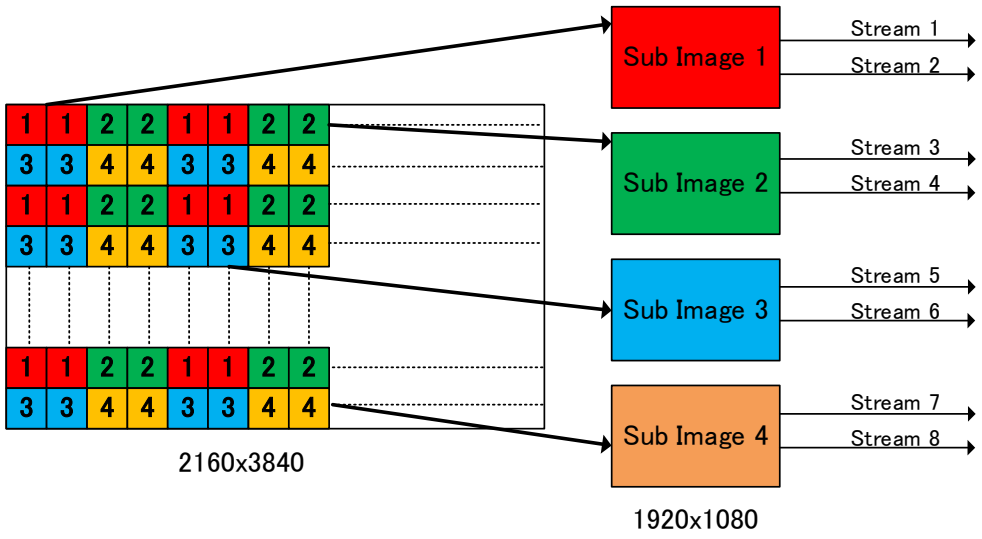

Figure 3-2 2-sample-interleave

3.4. P2I

In this block, a 1920x1080 progressive image is converted to an interlaced format. For Field 1, the conversion is performed as shown in Figure 3-3, and for Field 2, the conversion is done as shown in Figure 3-4.

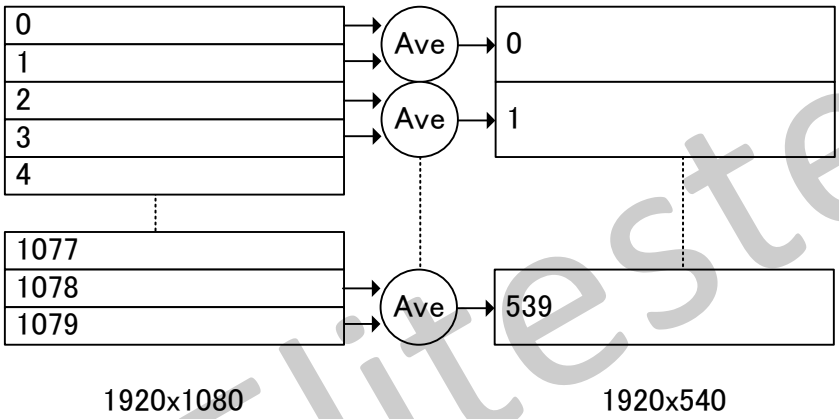

Figure 3-3 Field1 interlace format

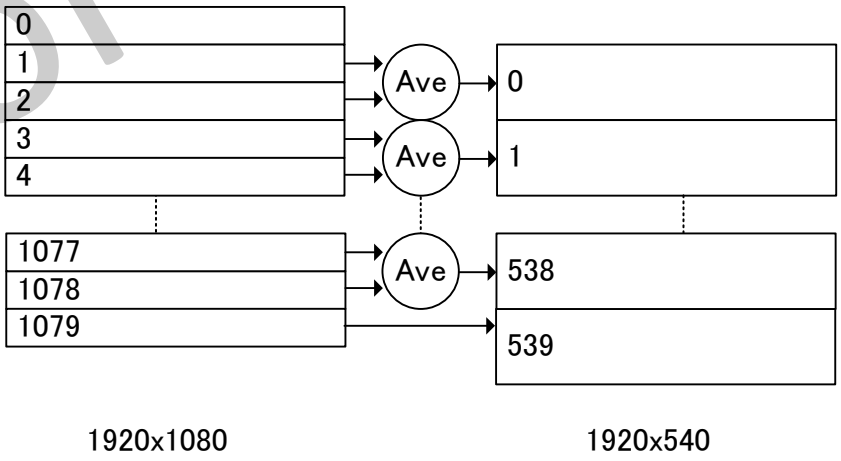

Figure 3-4 Field2 interlace format

3.5. TXBUF

Clock domain crossing from video clock to transmitter's clock. The video clock must originate from the same oscillation source as the transceiver's reference clock.

3.6. MAP

This block performs data mapping according to the SDI standard. It supports 3G-Level B and 6G Type2 formats.

3.7. Input Timing

The image data input to the SDI TX Bridge needs to be divided into four parts as shown in Figure 3-5. The input of the four-divided image data is shown in Figures 3-6 and 3-7.

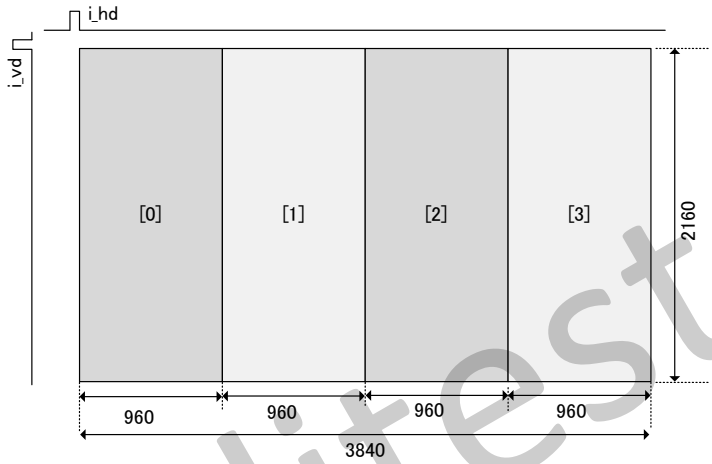

Figure 3-5 Split 4K Image

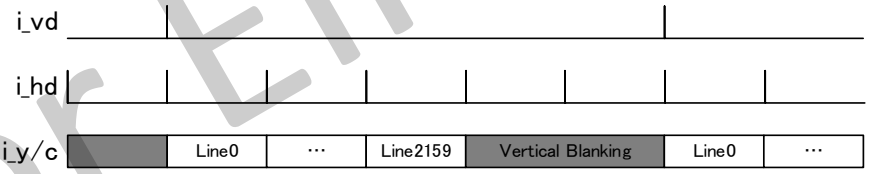

Figure 3-6 Vertical Input Timing

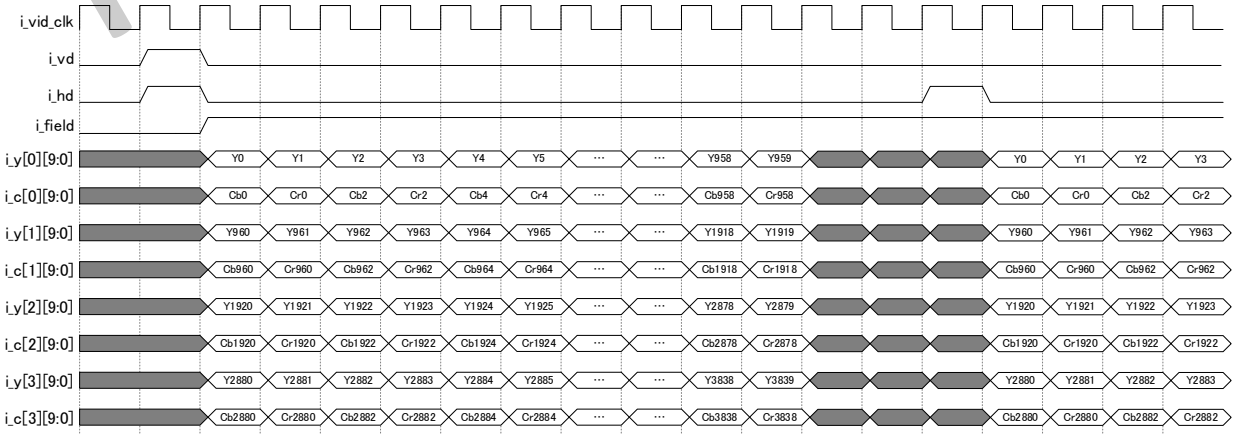

Figure 3-7 Horizontal Input Timing

Notes:

- i_vd must be input on the same cycle as i_hd.
- i_vd and i_hd must have a 1-pulse width.
- i_hd must be input at regular intervals during the vertical blanking period.

3.8. Input Parameters

Table 3-3 shows the clock frequency and parameters corresponding to the output format.

Table 3-1 Input parameters

Format	i_vid_clk[Mhz]	i_txclk[Mhz]	ch	Htotal	Hactive/Ch	Vtotal	Vactive	ip_fps_sel	i_mode_hd	i_mode_interlace	i_level_b
2160p60	148.5	148.5	4	1100	960	2250	2160	0	0	0	0
2160p59.94	148.35	148.35	4	1100	960	2250	2160	1	0	0	0
2160p50	148.5	148.5	4	1320	960	2250	2160	2	0	0	0
2160p30	148.5	148.5	4	2200	960	2250	2160	4	0	0	0
2160p29.97	148.35	148.35	4	2200	960	2250	2160	5	0	0	0
2160p25	148.5	148.5	4	2640	960	2250	2160	6	0	0	0
2160p24	148.5	148.5	4	2750	960	2250	2160	8	0	0	0
2160p23.98	148.35	148.35	4	2750	960	2250	2160	9	0	0	0
1080p60A	148.5	148.5	4	1100	960	2250	2160	0	1	0	0
1080p60B	148.5	148.5	4	1100	960	2250	2160	0	1	0	1
1080p59.94A	148.35	148.35	4	1100	960	2250	2160	1	1	0	0
1080p59.94B	148.5	148.5	4	1100	960	2250	2160	1	1	0	1
1080p50A	148.5	148.5	4	1320	960	2250	2160	2	1	0	0
1080p50B	148.5	148.5	4	1320	960	2250	2160	2	1	0	1
1080p30	148.5	74.25	4	2200	960	2250	2160	4	1	0	0
1080p29.97	148.35	74.175	4	2200	960	2250	2160	5	1	0	0
1080p25	148.5	74.25	4	2640	960	2250	2160	6	1	0	0
1080p24	148.5	74.25	4	2750	960	2250	2160	8	1	0	0
1080p23.98	148.35	74.175	4	2750	960	2250	2160	9	1	0	0
1080i60	148.5	74.25	4	1100	960	2250	2160	0	1	1	0
1080i59.94	148.35	74.175	4	1100	960	2250	2160	1	1	1	0
1080i50	148.5	74.25	4	1320	960	2250	2160	2	1	1	0

Note:

1. H total is the number of clock cycles between i_hd and i_hd.
2. V total is the number of lines between i_vd and i_vd.

4. Revision History

4.1. IP History

Date	Version	Descriptions
2025-03-21	01	First edition

4.2. Document History

Date	Version	Descriptions
2025-03-21	1.0	First edition