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JESD204B Demo MS4 : Elitestek

15th May 2025

XILINX ALLIANCE PROGRAM CERTIFIED

intel FPGA Design Solutions Network Gold

Agenda

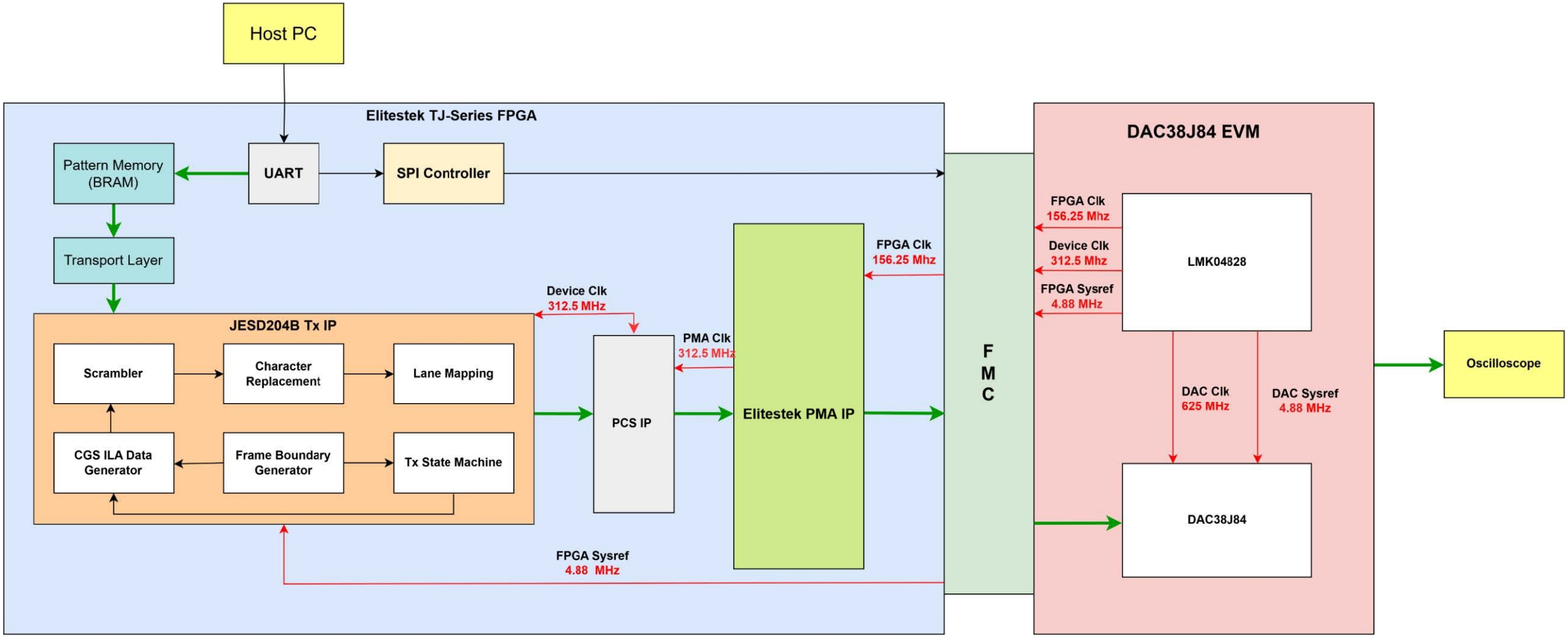
- JESD204B IP Features
- JESD204b Transmitter Block Design Deterministic Latency at 12.5 Gbps
  - JESD204b Transmitter Deterministic Latency Testing Block Design
  - Test Cases
  - Test Procedure and Test Setup
- JESD204b Receiver Deterministic Latency at 12.5 Gbps
  - JESD204b Receiver Deterministic Latency Testing Block Design
  - Test Cases
  - Test Procedure and Test Setup
- Test Results for all the Testing

IP Features

- Design as per JESD204B Standard.
- Supports Data Rate upto 12.5 Gbps
- Supports upto 8 lanes per core (This limitation is due to the Transceivers).
- Supports Transport and Link Layers.
- Supports Subclass 0 and 1.
- Does not support Subclass 2.
- No of Frames per Multiframe (K) = 1 to 32
- No of Samples per Frame (F) = 1 to 256
- Supports Scrambling.
- Supports Initial lane Alignment.
- Supports Character Replacement.
- AXI Stream Data interface.
- AXI Lite Configuration interface.

JESD204B Transmitter

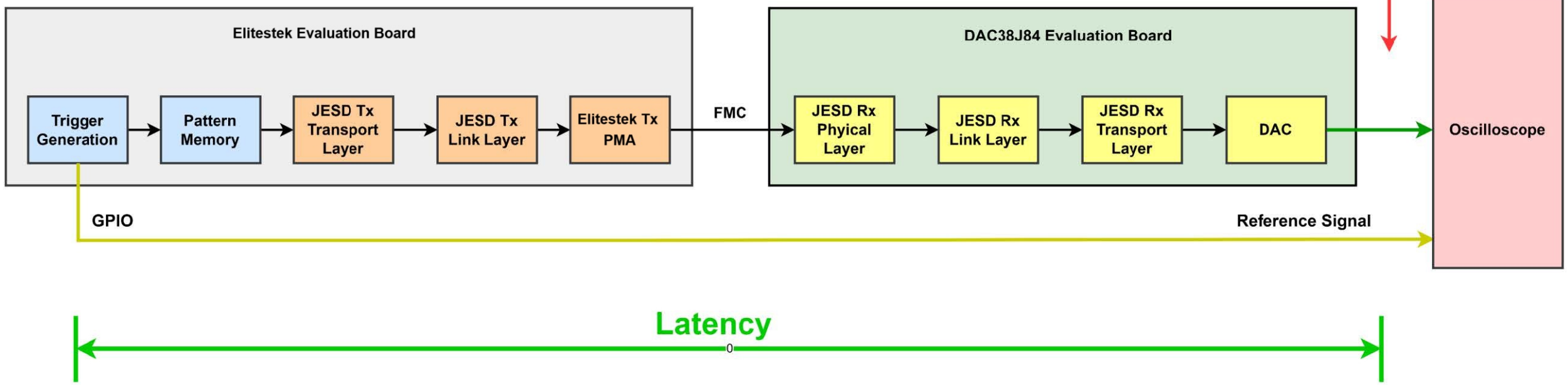
JESD204B Transmitter Block Design at 12.5 Gbps



DAC : Deterministic Latency Testing

- Trigger is generated inside FPGA
- This Trigger is square wave
- Data is sent to JESD IP when the Trigger signal is high.
- Trigger is connected to one channel of Oscilloscope
- Sine Samples are sent from the pattern memory when Trigger is high

- DAC Analog Output
- Sine Samples are output from the DAC
- DAC Output is connected to the second Channel of the scope



Test Cases

DAC Input sampling rate = SerDes Rate / (DAC Resolution after 8b10b * No of converters in a single lane)

DAC Output sampling rate = DAC Input sampling rate * Interpolation Factor

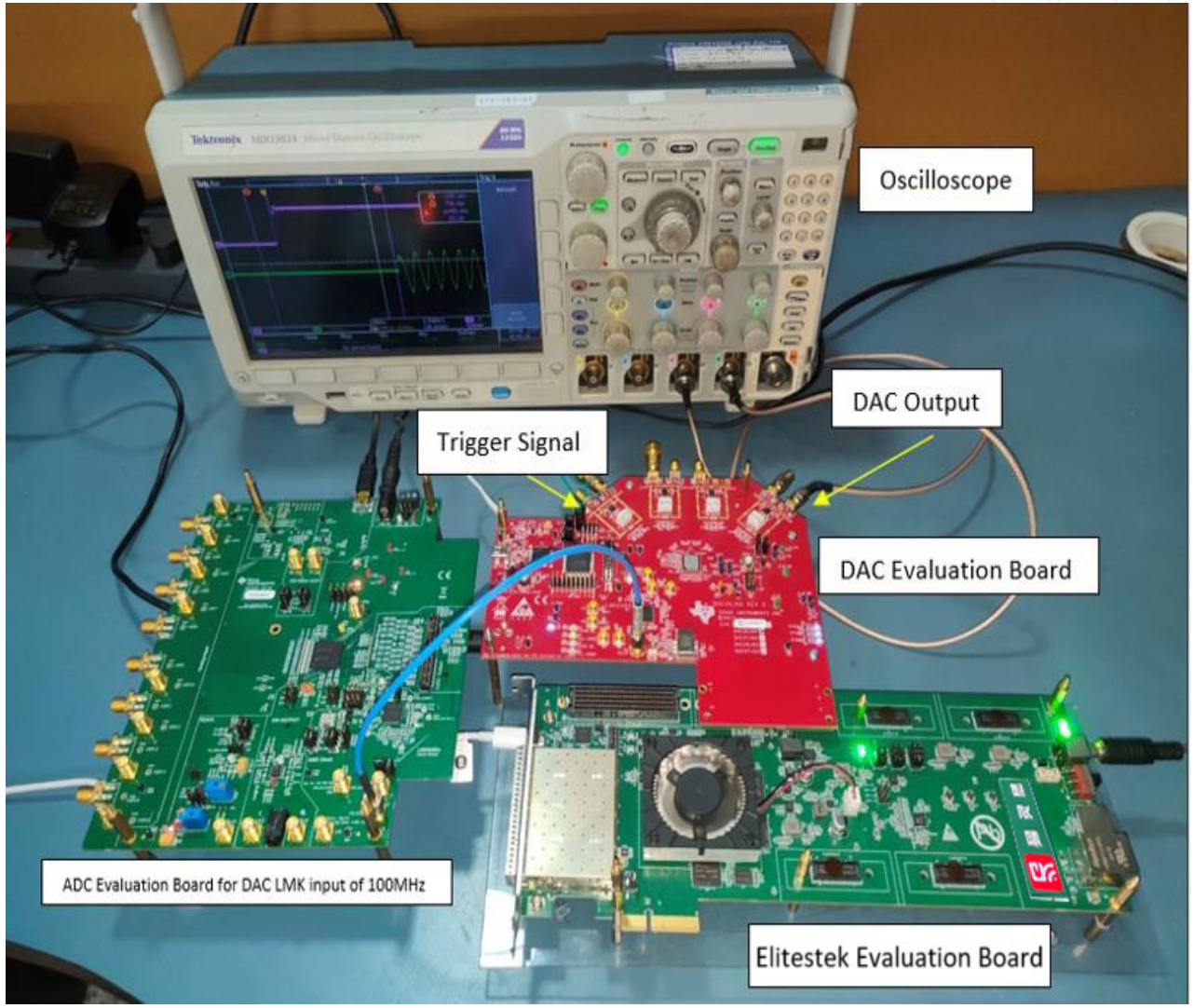
Test Case	Modes (LMF)	Interpolation	No. of converters in single lane	DAC Input Sampling Rate (MSPS)	DAC Output Sampling Rate (MSPS)	LMK Sysref	PLL2 Input Frequency (MHz)
0	442	x1	1	625.00	625.00	Continuous	100.00
1	442	x2	1	625.00	1250.00	Continuous	100.00
2	442	x4	1	625.00	2500.00	Continuous	100.00
3	244	x2	2	312.50	625.00	Continuous	100.00
4	244	x4	2	312.50	1250.00	Continuous	100.00
5	244	x8	2	312.50	2500.00	Continuous	100.00
Deterministic Latency Testing							
6	442	X4	1	625.00	2500.00	Continuous	100.00
Multiple Reset testing							
7	442	X4	1	625.00	2500.00	Continuous	100.00

Test Procedure

Following are the Hardware connection :

1. Connect TI DAC EVM (TI DAC38J84)with the Elitestek TJ-Series Evaluation (TJ375N1156X) Board on J14 FMC Connector(Quad 3)
2. Connect the host PC with the Elitestek TJ-Series Evaluation Board via a USB cable, which can be used as a UART and JTAG
3. Start the Oscilloscope and connect it with DAC EVM through SMA cables
4. Open the Efinity Programmer and program the required bitfile
5. For deterministic latency testing, select the test case number 6
6. Set up the trigger condition in the Oscilloscope

Test Set up



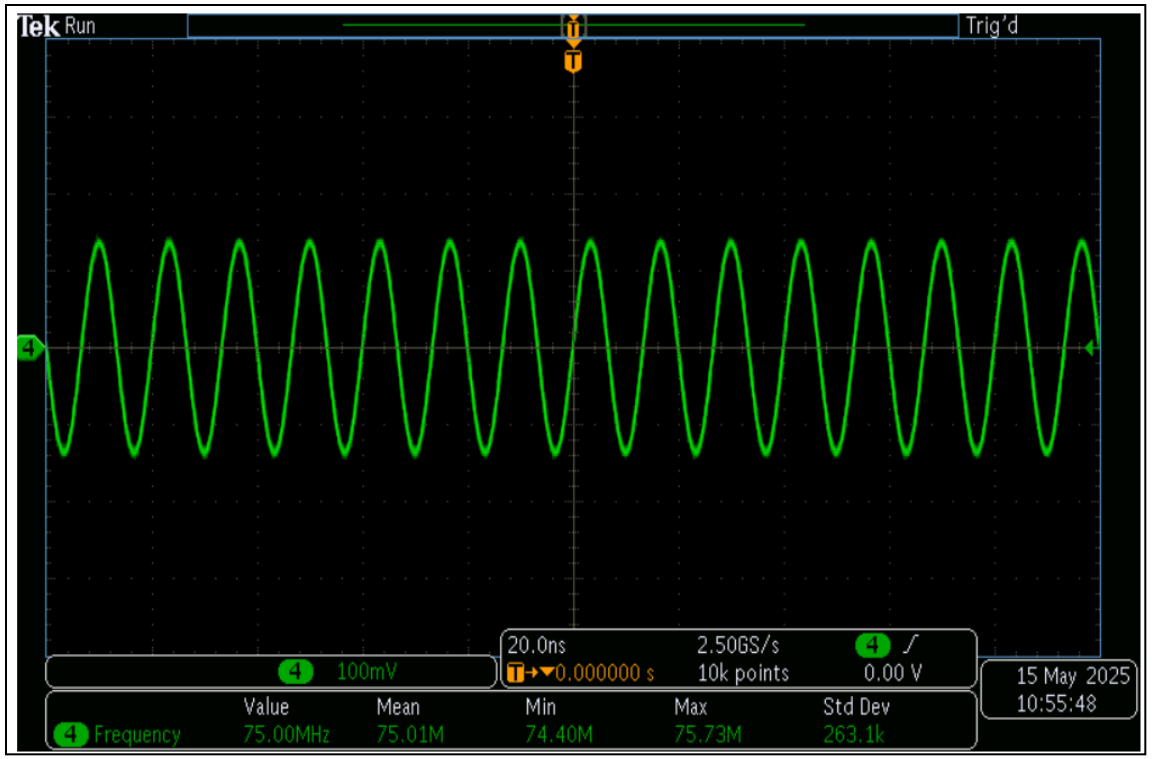
Test Procedure : TCL Script sequence

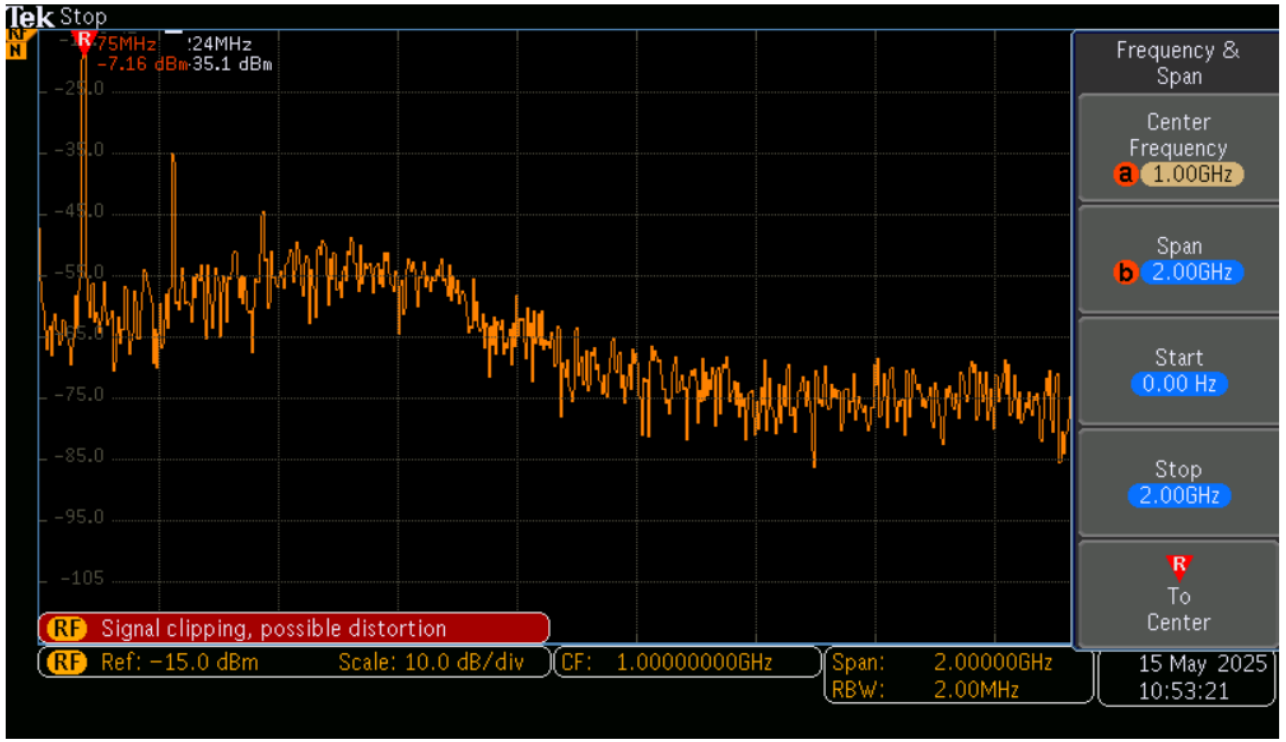
1. Open the TCL IDE from the start menu, by default the required TCL script is sourced
2. The console will display the option to select the testing for the JESD204B Transmitter with DAC 5 Gbps and 12.5 Gbps or JESD204B Receiver with ADC 5Gbps and 12.5Gbps . Select the required option to test the JESD204B Transmitter with DAC at 12.5 Gbps.
3. The user must select the DAC test cases (Modes) and enter a number from 0 to 7 according to the requirement.
4. The second input is the selection of the sub modes,
    - a = Selection of the mode ‘a’ is done when LMK04828 is configured for the first time after being powered up. This mode ensures that LMK04828 is configured so that clocks are available to Elitestek PMA IP, as it requires clocks before bit file configuration to generate the necessary PMA clocks.
    - b = Selection of this mode will run the complete sequence required for the link up of JESD204B TX IP with the DAC and configure the pattern memory with data samples
5. On selection of ‘a’, LMK gets configured.
6. Reprogram the bit file after selection of the ‘a’ mode or in case of MCS file programmed, power cycle only the Elitestek Evaluation board
7. Select the ‘b’ option, which will display the JESD204B lock status and DAC errors
8. Select the input frequency and View the output waveform on the oscilloscope

Test Results

DAC at 12.5 Gbps : Mode : 442 , x2 Interpolation

Input Frequency = 75MHz



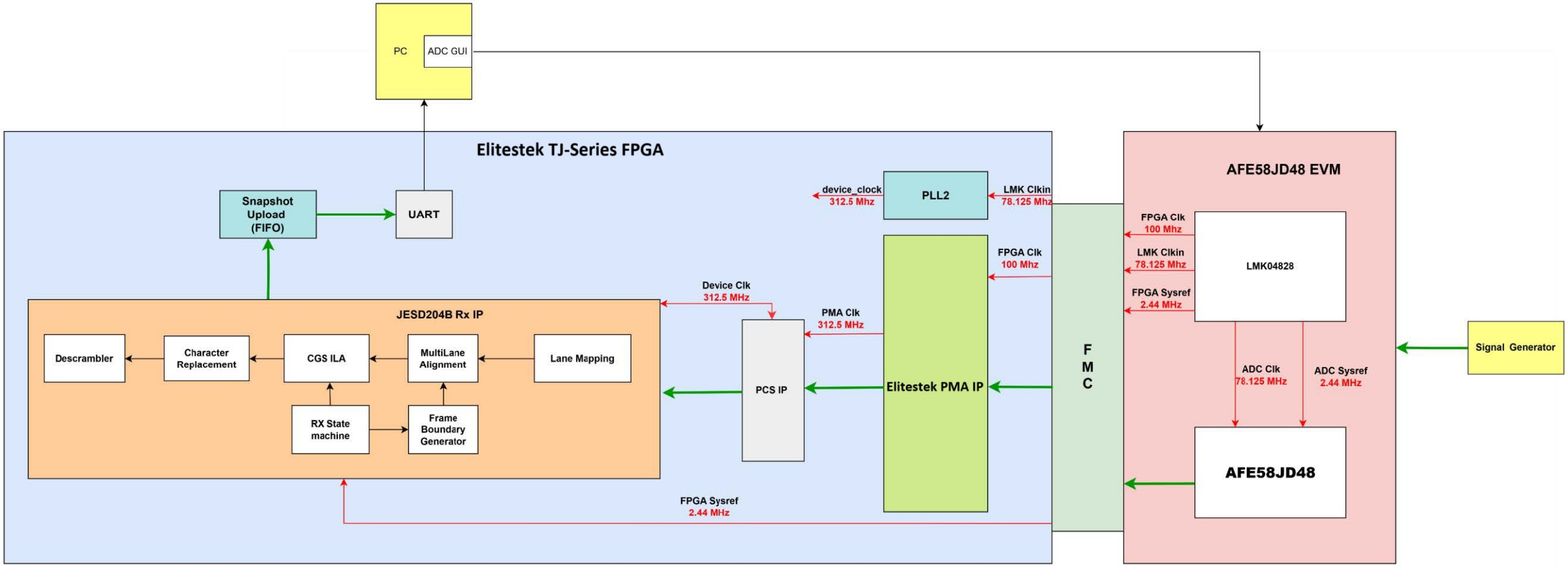


DAC : Deterministic Latency Testing Result at 12.5 Gbps

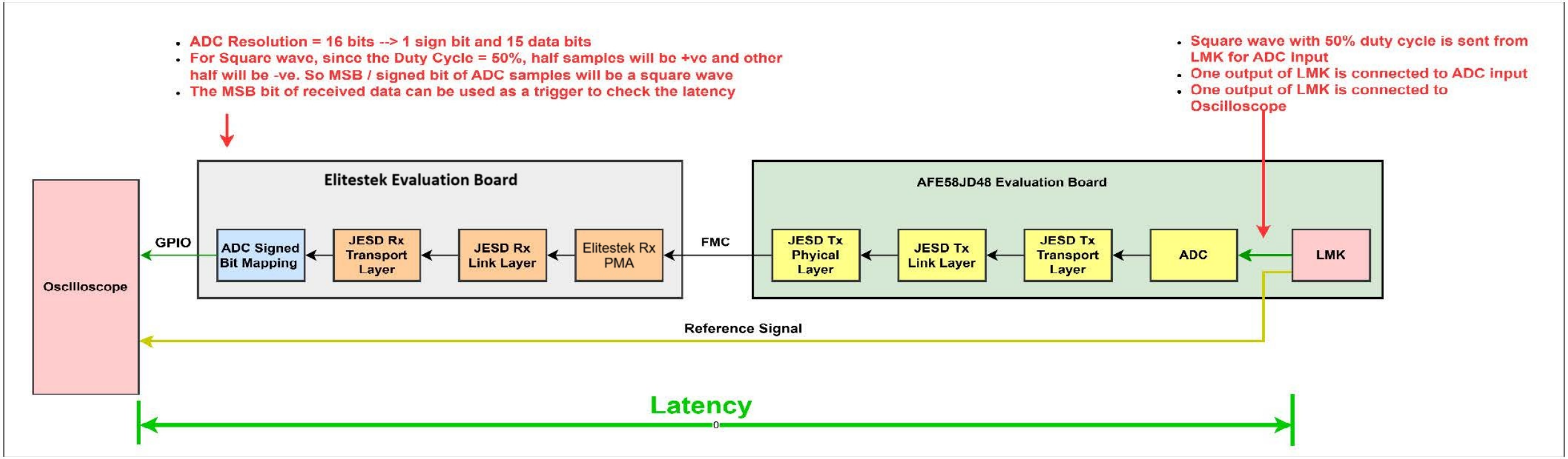
Reset Type	Mode (LMF)	Interpolation	Min Value (ns)	Typical Value (ns)	Max Value (ns)	No. of Iterations	Variation (ps)
Cold	442	x4	324.175	324.241	324.308	30	0.133
Warm	442	x4	324.166	324.241	324.313	30	0.147

JESD204B Receiver

JESD204B Receiver Block Design



ADC : Deterministic Latency Testing



Test Cases

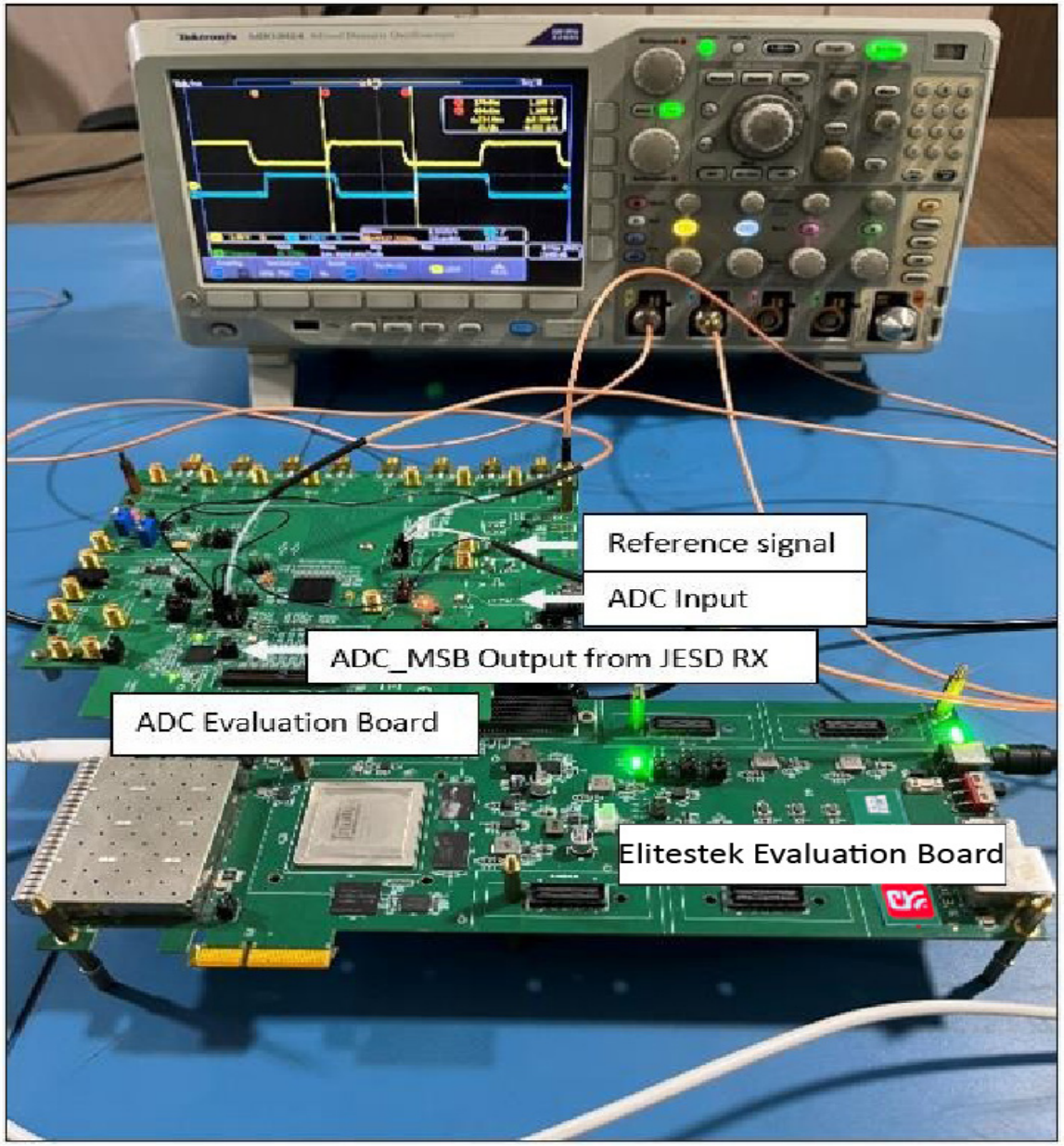
ADC Input sampling rate = SerDes Rate / (ADC Resolution after 8b10b * No of converters in a single lane)

Test Case	Modes (LMF)	No. of converters in single lane	ADC Input Sampling Rate (MSPS)	ADC Output Sampling Rate (MSPS)	LMK Sysref
0	148 (160X)	8	78.125	78.125	Continuous

Test Procedure

1. Connect TI ADC EVM (TI ADS54J66)with the Elitestek TJ-Series Evaluation (TJ375N1156X) Board on J15 FMC Connector
(Quad 2).
2. Connect host PC with Elitestek TJ-Series Evaluation Board via USB cable which can be used as UART and JTAG
3. Start Signal Generator and connect it with ADC EVM through SMA cables.
4. For deterministic latency set up the trigger condition in the Oscilloscope
5. One output of LMK is used for ADC input data generation which will be mapped on ADC0 input and other output is used as reference signal for checking deterministic latency on oscilloscope .
6. The MSB bit of the output data is mapped to the GPIO, which is connected to another channel of the CRO.

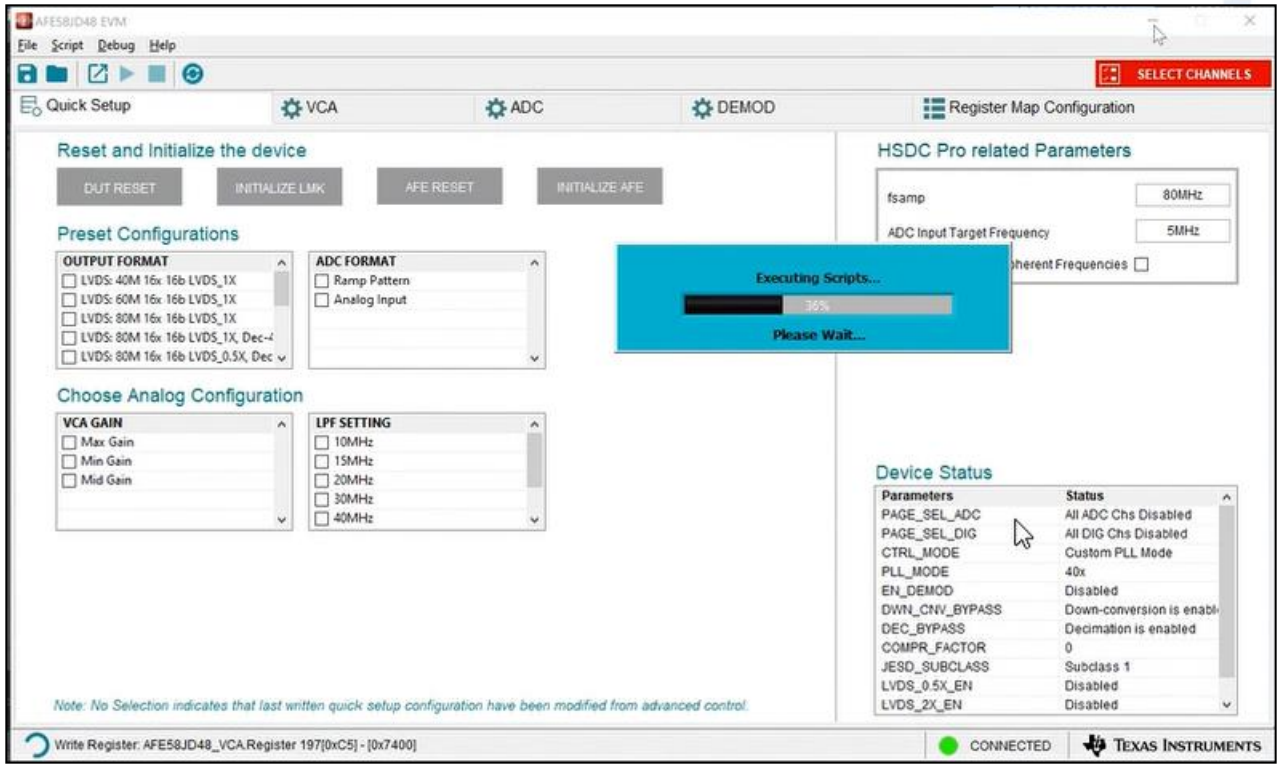
Test Set up



Test Procedure : ADC GUI configuration

1. The ADC is configured through the GUI
2. Open the GUI and load the required configuration (.cfg) file through which we want to operate the ADC eval board GUI (File → Open configuration → file_name.cfg)

Once ADC is configured , program the bit file to the Elitestek evaluation board.



Test Procedure : TCL Script sequence

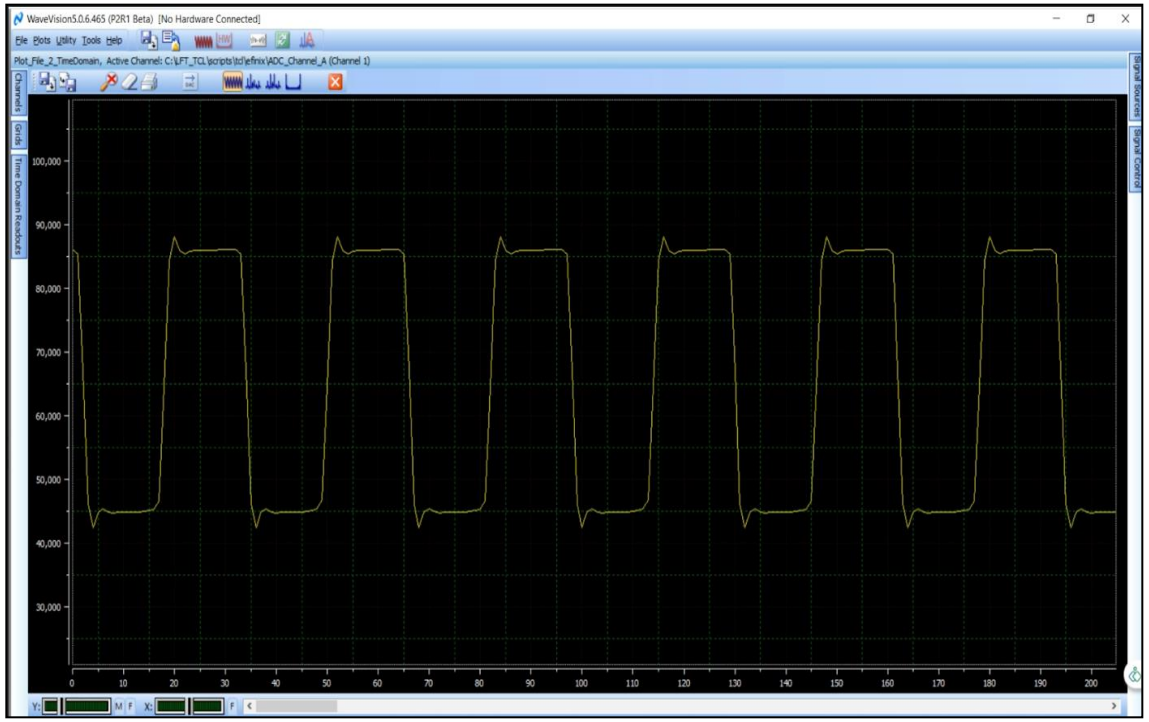
1. Open the TCL IDE from the start menu, by default the required TCL script is sourced
2. The console will display the option to select the testing for the JESD204B Transmitter with DAC 5 Gbps and 12.5 Gbps or JESD204B Receiver 5 Gbps and 12.5 Gbps with ADC. Select required option to test the JESD204B Transmitter with DAC.
3. This script includes the complete sequence from the JESD204B configuration to the capturing of the data through snapshot streaming interface and data decryption for each ADC input
4. After selection of ADC testing the sequence of measuring the clock frequency, JESD204B RX IP configuration for 40X mode and status of errors and link up information are displayed
5. Once link-up is done without any errors, the captured ADC sample data are uploaded to the host PC with user permission, if user wants to upload the data, select option 1
6. Once the decryption is done for captured samples, open the TI wave vision software to view the waveform for the captured file.

ADC : Deterministic Latency Testing Result at 12.5 Gbps

Reset Type	Mode	Min Value (ns)	Typical Value (ns)	Max Value (ns)	No. of Iterations	Variation (ps)
Cold	160X	233.32	233.4	233.47	30	150
Warm	160X	233.34	233.4	233.45	30	110

Captured waveform in TI WaveVision

Input Frequency = 2.44M Hz



Queries ?

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Thank You!

Arpitha Shetty

806, 8th Floor BPTP Park Centra
Sector–30, NH–8 Gurgaon – 122001 Haryana (India)

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