logic fruit Technologies

25th January 2025

JESD204B Demo : Elitestek

XILINX ALLIANCE PROGRAM CERTIFIED

intel FPGA Design Solutions Network Gold

Agenda

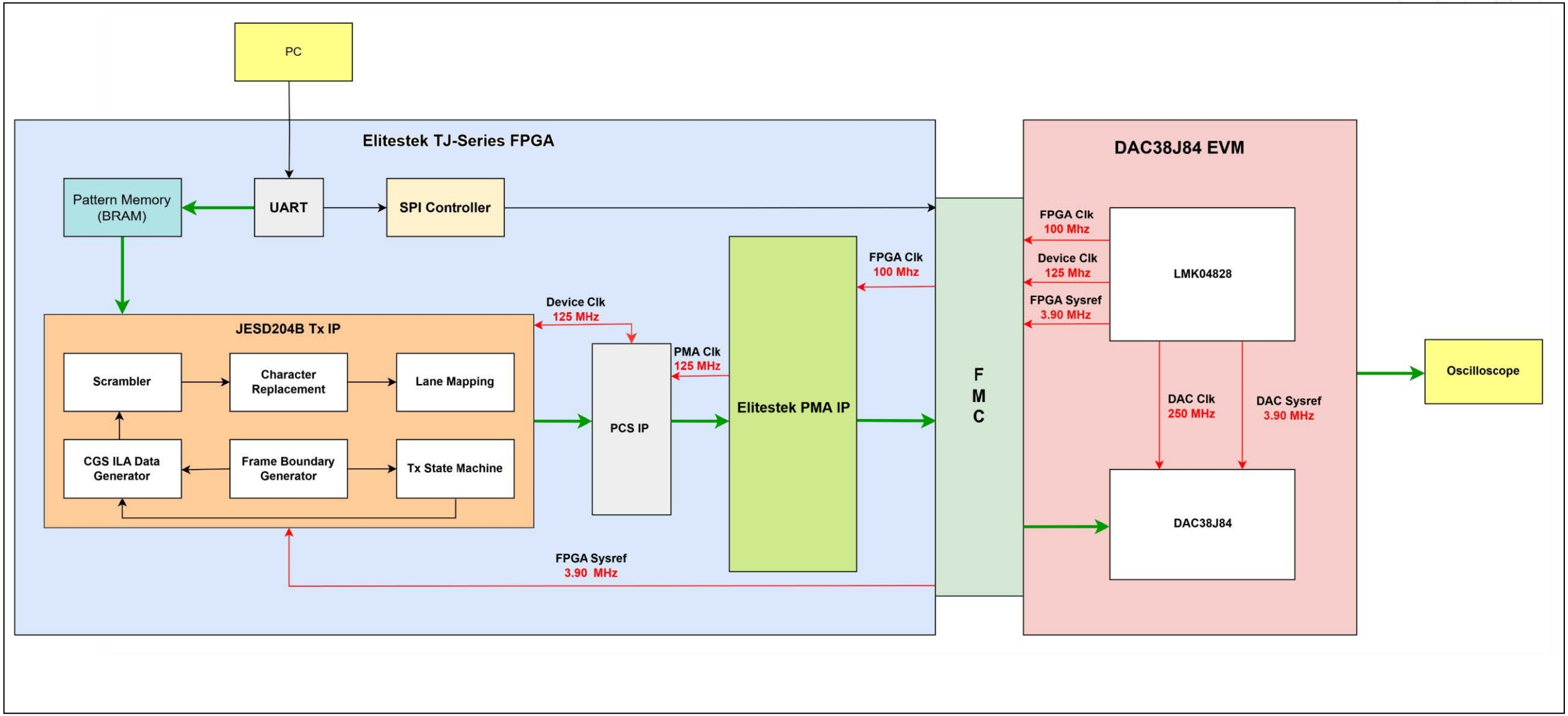
- JESD204B IP Features
- JESD204b Transmitter Porting
  - JESD204b Transmitter Hardware Validation Block Design
  - Test Cases
  - Test Parameters
  - Test Procedure and Test Setup
- JESD204b Receiver Porting
  - JESD204b Receiver Hardware Validation Block Design
  - Test Cases
  - Test Parameters
  - Test Procedure and Test Setup
- JESD204b Transmitter Deterministic Latency
  - JESD204b Transmitter Deterministic Latency Testing Block Design
  - Test Cases
  - Test Parameters
  - Test Procedure and Test Setup
- JESD204b Receiver Deterministic Latency
  - JESD204b Receiver Deterministic Latency Testing Block Design
  - Test Cases
  - Test Parameters
  - Test Procedure and Test Setup
- Test Result for all the Testing

IP Features

- Design as per JESD204B Standard.
- Supports Data Rate upto 12.5 Gbps
- Supports upto 8 lanes per core (This limitation is due to the Transceivers).
- Supports Transport and Link Layers.
- Supports Subclass 0 and 1.
- Does not support Subclass 2.
- No of Frames per Multiframe (K) = 1 to 32
- No of Samples per Frame (F) = 1 to 256
- Supports Scrambling.
- Supports Initial lane Alignment.
- Supports Character Replacement.
- AXI Stream Data interface.
- AXI Lite Configuration interface.

JESD204B Transmitter

JESD204B Transmitter Block Design



Test Cases

DAC Input sampling rate = SerDes Rate / (DAC Resolution after 8b10b * No of converters in a single lane)

DAC Output sampling rate = DAC Input sampling rate * Interpolation Factor

Test Case	Modes (LMF)	Interpolation	No. of converters in single lane	DAC Input Sampling Rate (MSPS)	DAC Output Sampling Rate (MSPS)	LMK Sysref
0	442	x1	1	250.00	250.00	Continuous
1	442	x2	1	250.00	500.00	Continuous
2	442	x4	1	250.00	1000.00	Continuous
3	244	x2	2	125.00	250.00	Continuous
4	244	x4	2	125.00	500.00	Continuous
5	244	x8	2	125.00	1000.00	Continuous
Deterministic Latency Testing						
6	442	X4	1	250.00	1000.00	Pulsed
Multiple Reset testing						
7	442	X4	1	250.00	1000.00	Pulsed

Test Parameters

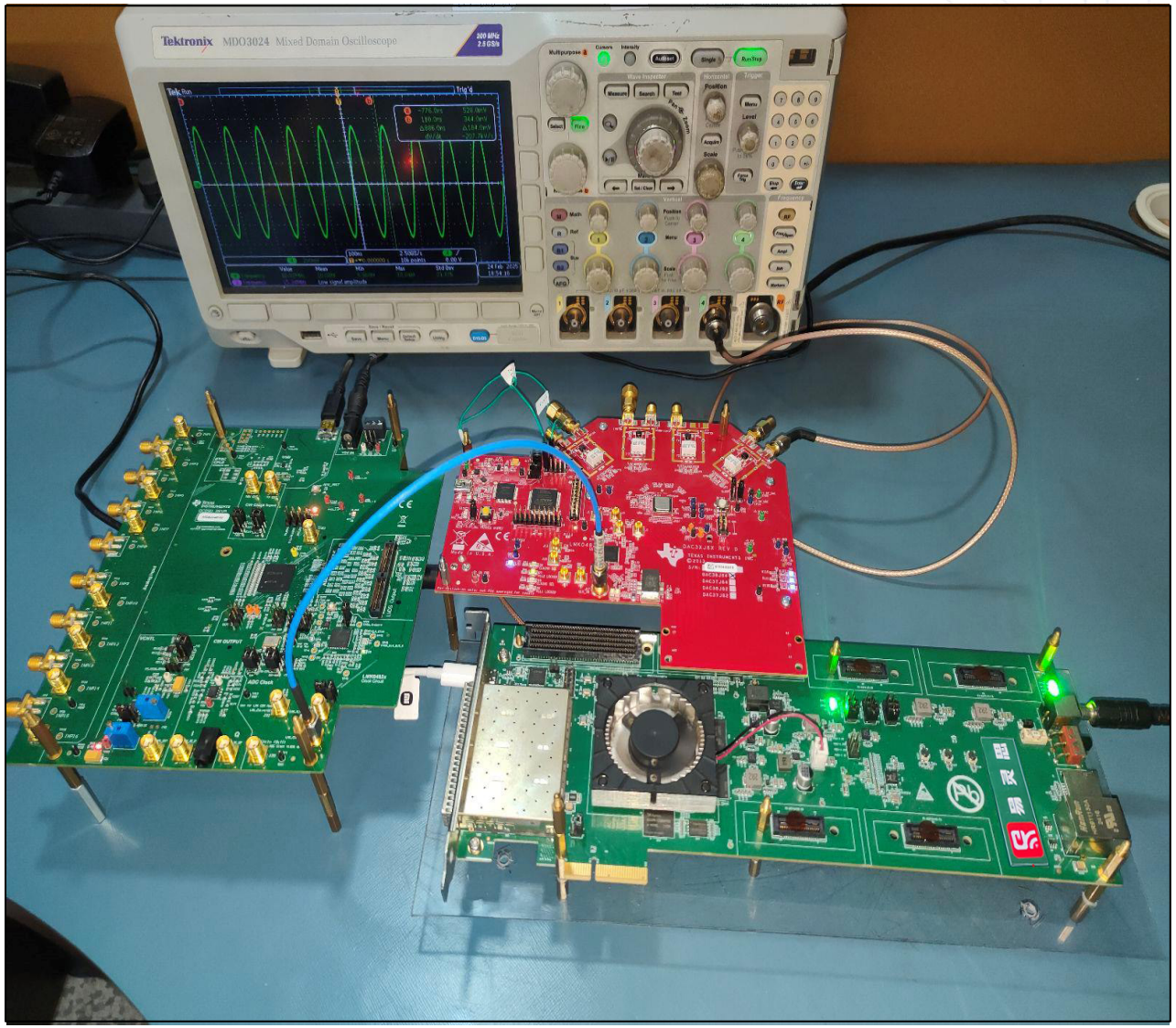
- Serdes Rate = 5 Gbps
- FPGA JESD204B Clock = 125 MHz
- FPGA Reference Clock = 100 MHz
- FPGA Sysref = 3.90 MHz
- DAC Clock = 250 MHz
- DAC Sysref = 3.90625 MHz
- No of Frames per MultiFrame (K) =32
- Test Pattern
  - Channel A : 10 Mhz Sine wave.
  - Channel C : 10 MHz Sine wave.

Test Procedure

Following are the Hardware connection :

1. Connect TI DAC EVM (TI DAC38J84)with the Elitestek TJ-Series Evaluation (TJ375N1156X) Board on J14 FMC Connector(Quad 3)
2. Connect host PC with Elitestek TJ-Series Evaluation Board via USB cable which can be used as UART and JTAG
3. Start the Oscilloscope and connect it with DAC EVM through SMA cables.
4. Open the Efinity Programmer and program the required bitfile.

Test Set up



Test Procedure : TCL Script sequence

1. Open the TCL IDE from the start menu, by default the required TCL script is sourced
2. The console will display the option to select the testing for the JESD204B Transmitter with DAC or JESD204B Receiver with ADC. Select option 1 to test the JESD204B Transmitter with DAC.
3. The user must select the DAC test cases (Modes) and enter a number from 0 to 7 according to the requirement.
4. The second input is the selection of the sub modes,
    - a = Selection of the mode ‘a’ is done when LMK04828 is configured for the first time after being powered up. This mode ensures that LMK04828 is configured so that clocks are available to Elitestek PMA IP, as it requires clocks before bit file configuration to generate the necessary PMA clocks.
    - b = Selection of this mode will run the complete sequence required for the link up of JESD204B TX IP with the DAC and configure the pattern memory with data samples
5. On selection of ‘a’, LMK gets configured.
6. Reprogram the bit file after selection of the ‘a’ mode or in case of MCS file programmed, power cycle only the Elitestek Evaluation board
7. Select the ‘b’ option, this will display the JESD204B lock status and DAC errors
8. Select the input frequency
9. View the output waveform on the oscilloscope

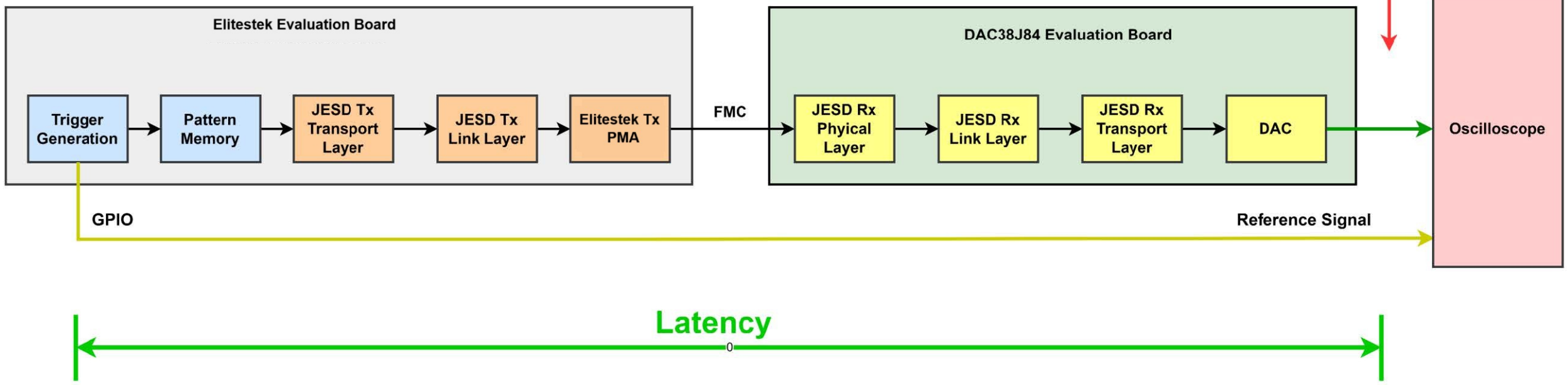
Test Results Ch A - 10 MHz & Ch C - 10 MHz

JESD204B Transmitter DETERMINISTIC LATENCY TESTING

DAC : Deterministic Latency Testing

- Trigger is generated inside FPGA
- This Trigger is square wave
- Data is sent to JESD IP when the Trigger signal is high.
- Trigger is connected to one channel of Oscilloscope
- Sine Samples are sent from the pattern memory when Trigger is high

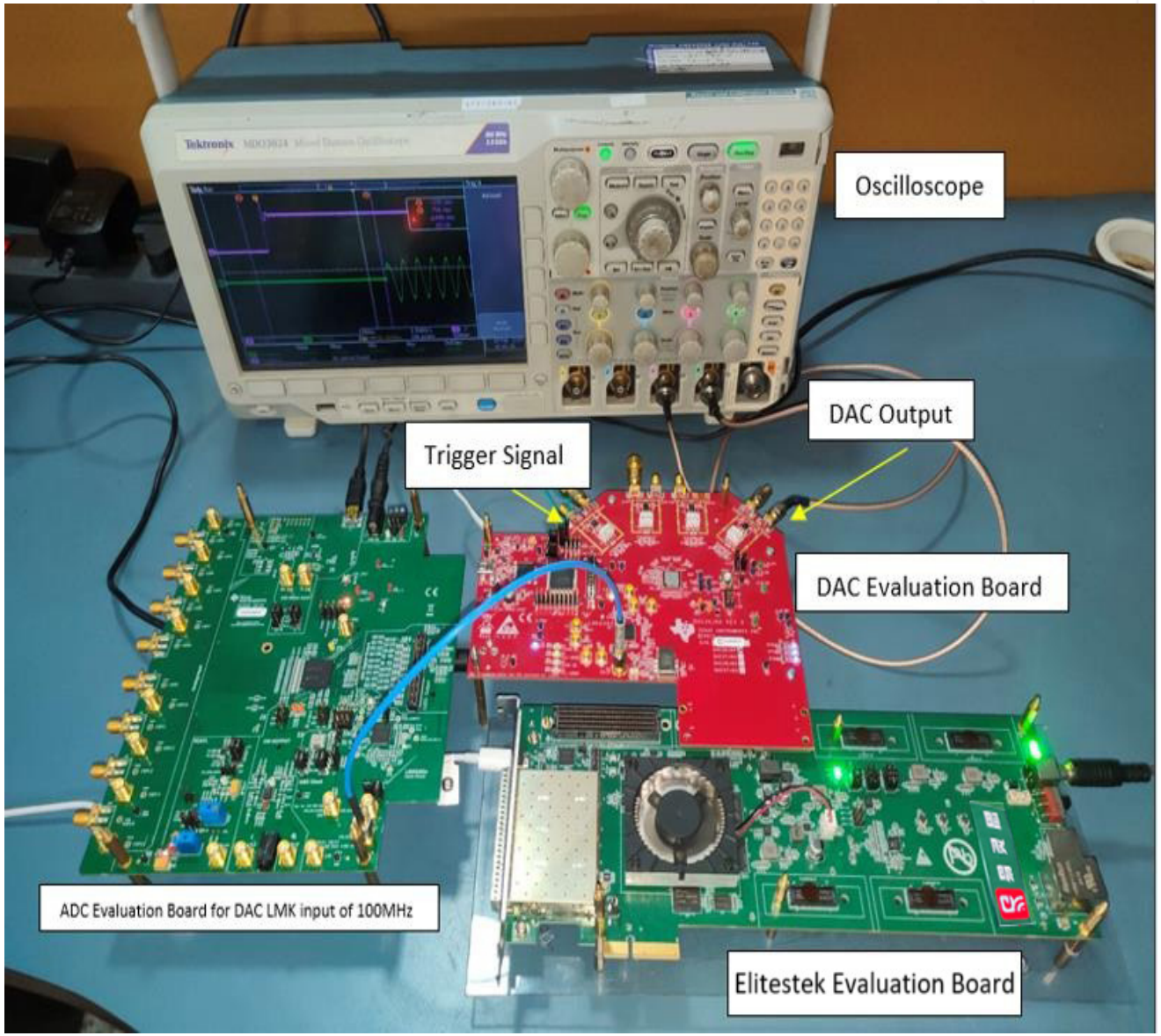
- DAC Analog Output
- Sine Samples are output from the DAC
- DAC Output is connected to the second Channel of the scope



Test Procedure

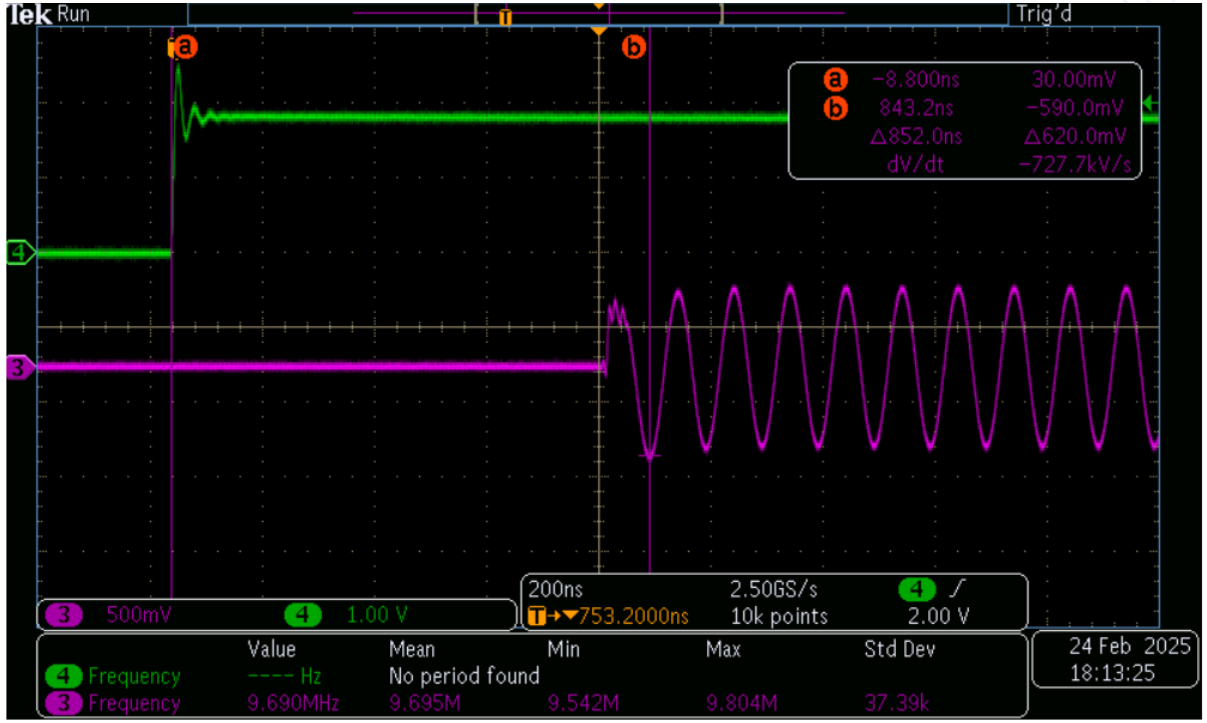
1. The procedure is same as the one explained in slide number 9.
2. For deterministic latency testing select the test case number 9.
3. Set up the trigger condition in the Oscilloscope.

Test Set up



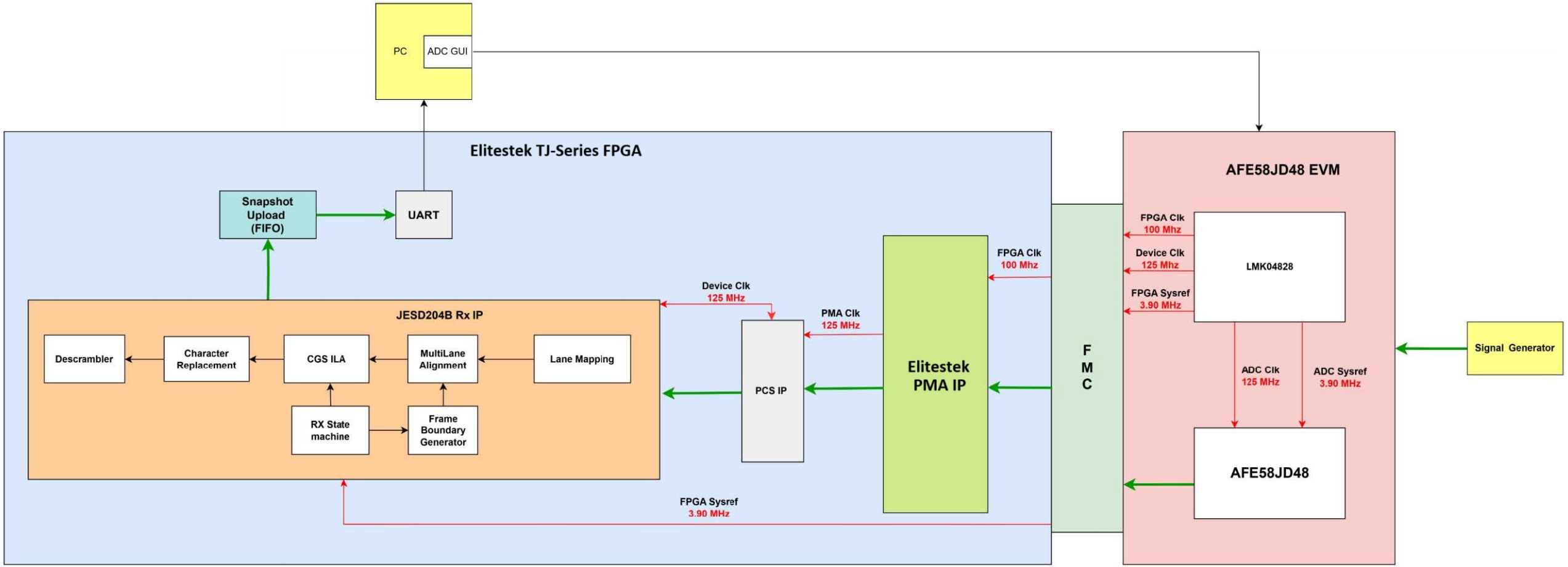
DAC : Deterministic Latency Testing Result

Reset Type	Mode (LMF)	Interpolation	Min Value (ns)	Typical Value (ns)	Max Value (ns)	No. of Iterations	Variation (ps)
Cold	40X	x4	852.00	852.00	852.10	30	150
Warm	40X	x4	852.00	852.00	852.00	30	100



JESD204B Receiver

JESD204B Receiver Block Design



Test Cases

ADC Input sampling rate = SerDes Rate / (ADC Resolution after 8b10b * No of converters in a single lane)

Test Case	Modes (LMF)	No. of converters in single lane	ADC Input Sampling Rate (MSPS)	ADC Output Sampling Rate (MSPS)	LMK Sysref
0	484 (40X)	2	125.00	125.00	Continuous

Test Parameters

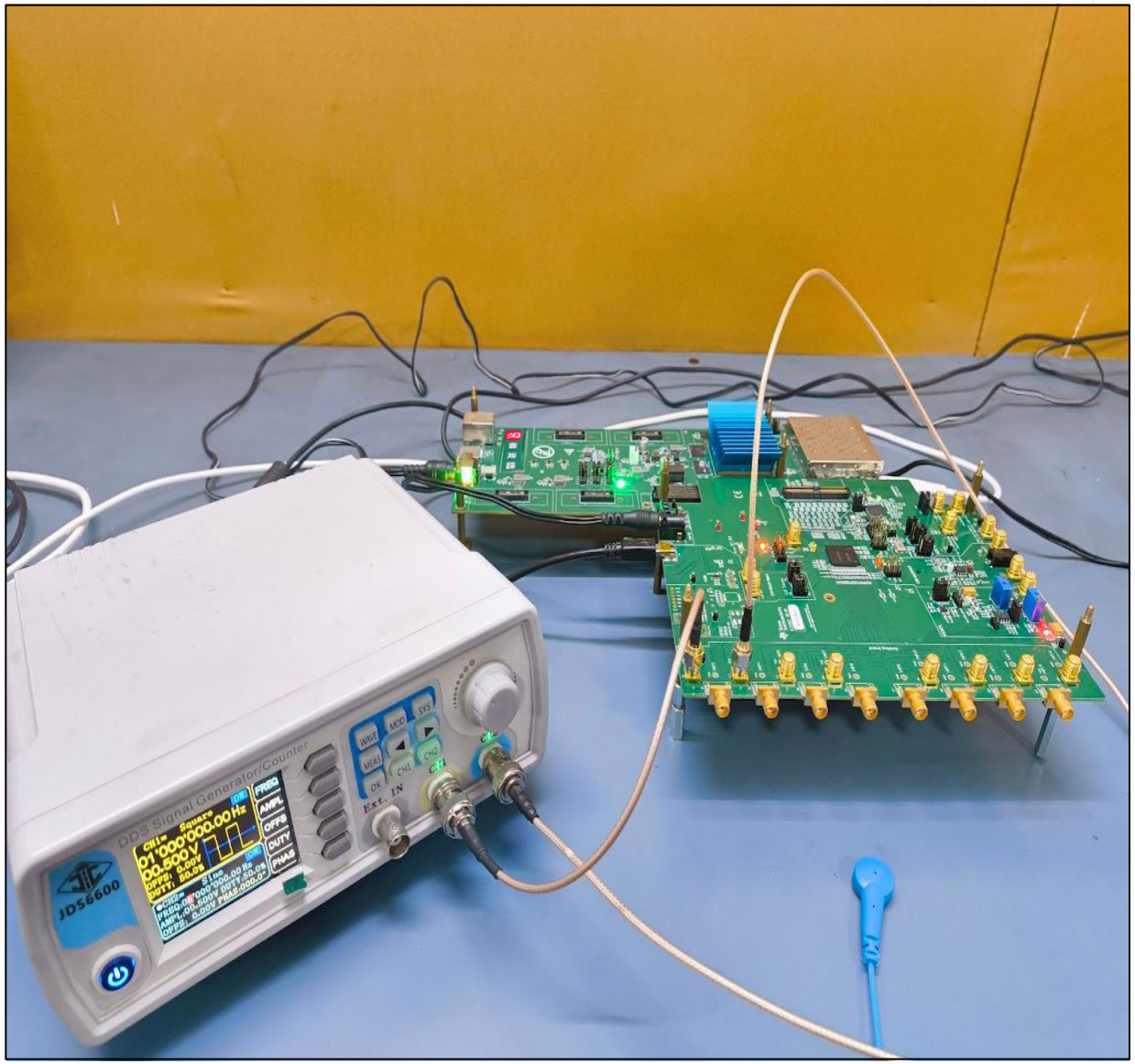
- Serdes Rate = 5 Gbps
- FPGA JESD204B Clock = 125 MHz
- FPGA Reference Clock = 100 MHz
- FPGA Sysref = 3.90 MHz
- ADC Clock = 125 MHz
- ADC Sysref = 3.90625 MHz
- Decimation = x1
- Test Pattern
  - Channel A : 1 Mhz Sine Wave, 500mv Amplitude
  - Channel C : 5 MHz Sine Wave,500mv Amplitude.
  - Channel B,D : Left Open .

Test Procedure

Following are the Hardware connection :

1. Connect TI ADC EVM (TI ADS54J66)with the Elitestek TJ-Series Evaluation (TJ375N1156X) Board on J15 FMC Connector
   (Quad 2).
2. Connect host PC with Elitestek TJ-Series Evaluation Board via USB cable which can be used as UART and JTAG
3. Start Signal Generator and connect it with ADC EVM through SMA cables.

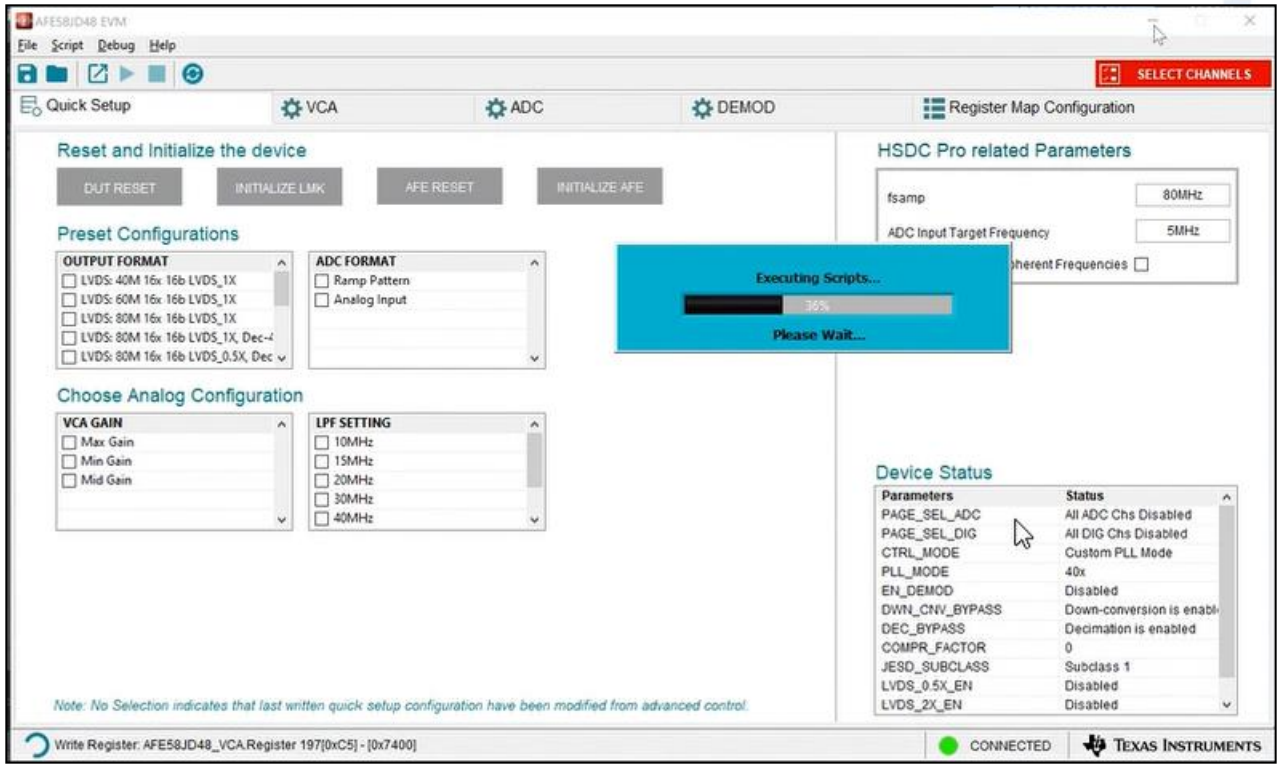
Test Setup



Test Procedure : ADC GUI configuration

1. The ADC is configured through the GUI
2. Open the GUI and load the required configuration (.cfg) file through which we want to operate the ADC eval board GUI (File → Open configuration → file_name.cfg)

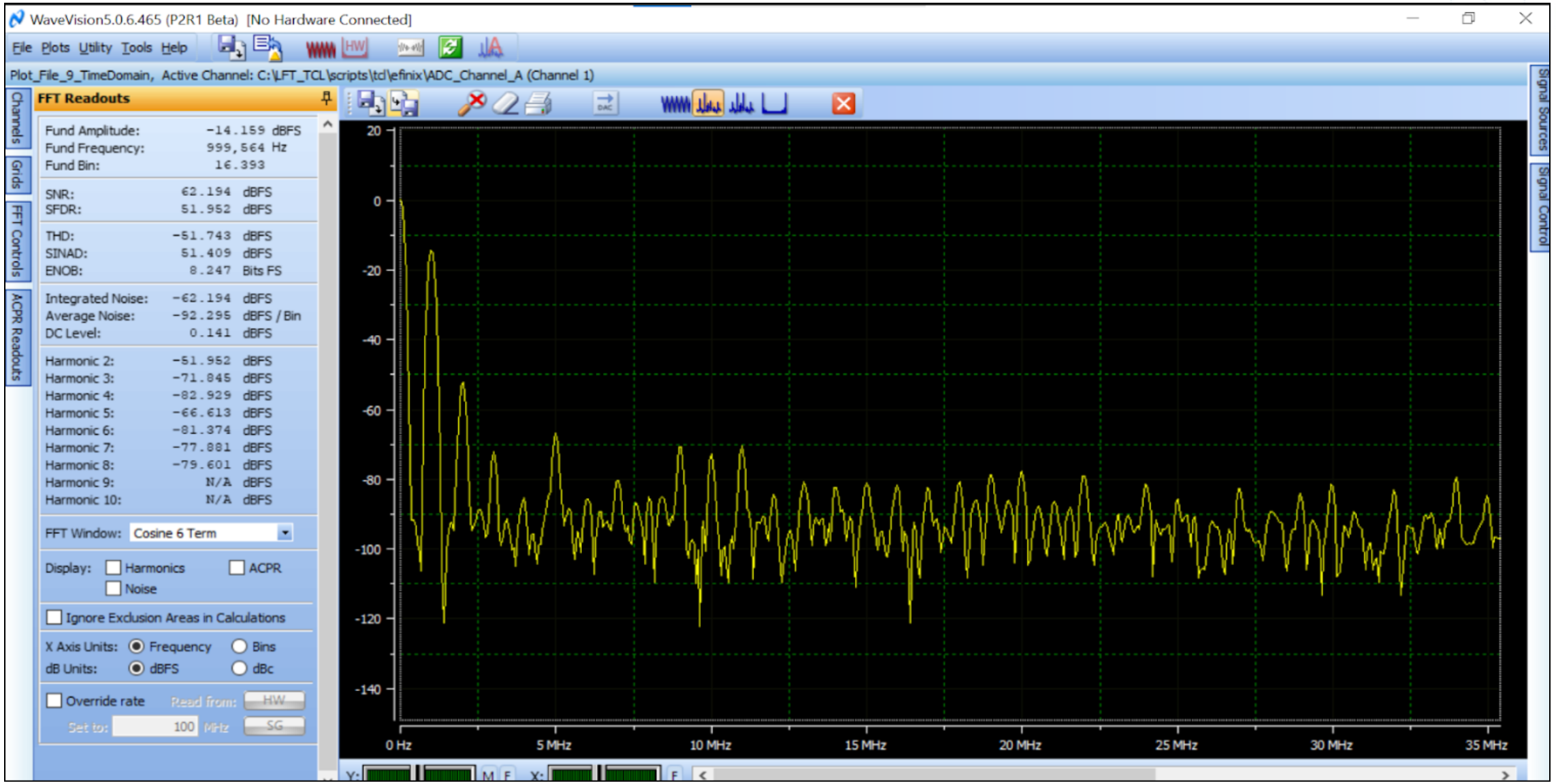
Once ADC is configured , program the bit file to the Elitestek evaluation board.



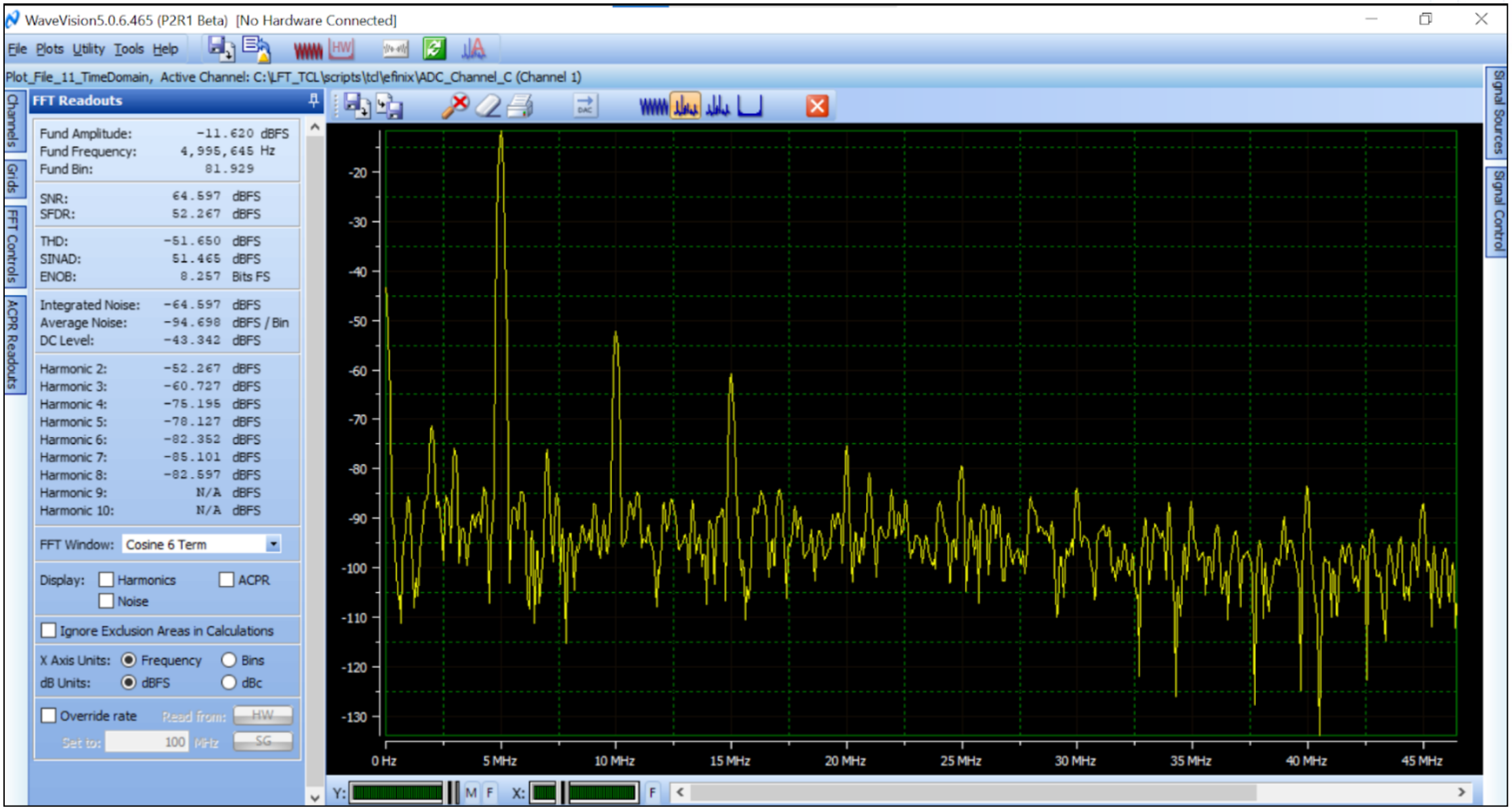
Test Procedure : TCL Script sequence

1. Open the TCL IDE from the start menu, by default the required TCL script is sourced
2. The console will display the option to select the testing for the JESD204B Transmitter with DAC or JESD204B Receiver with ADC. Select option 2 to test the JESD204B Transmitter with DAC.
3. This script includes the complete sequence from the JESD204B configuration to the capturing of the data through snapshot streaming interface and data decryption for each ADC input
4. After selection of ADC testing the sequence of measuring the clock frequency, JESD204B RX IP configuration for 40X mode and status of errors and link up information are displayed
5. Once link up is done without any errors, the captured ADC sample data are uploaded to the host PC with user permission, if user wants to upload the data, select the option 1
6. Once the decryption is done for captured samples, open the TI wave vision software to view the waveform for the captured file.

Test Results - Ch A - Frequency Domain



Test Results - Ch C - Frequency Domain

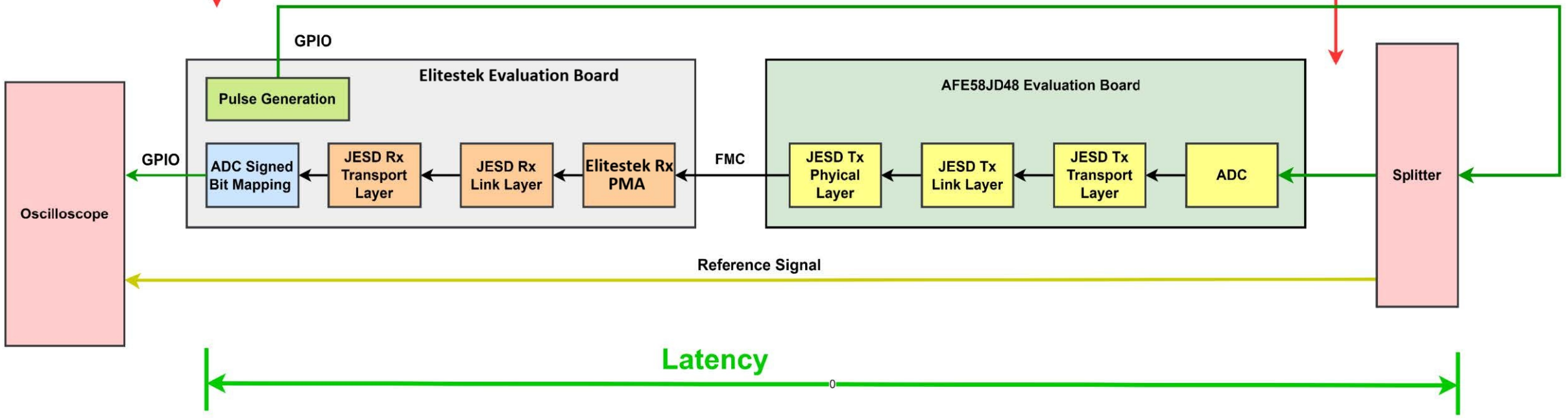


JESD204B Receiver DETERMINISTIC LATENCY TESTING

ADC : Deterministic Latency Testing

- ADC Resolution = 16 bits --> 1 sign bit and 15 data bits
- For Square wave, since the Duty Cycle = 50%, half samples will be +ve and other half will be -ve. So MSB / signed bit of ADC samples will be a square wave
- The MSB bit of received data can be used as a trigger to check the latency

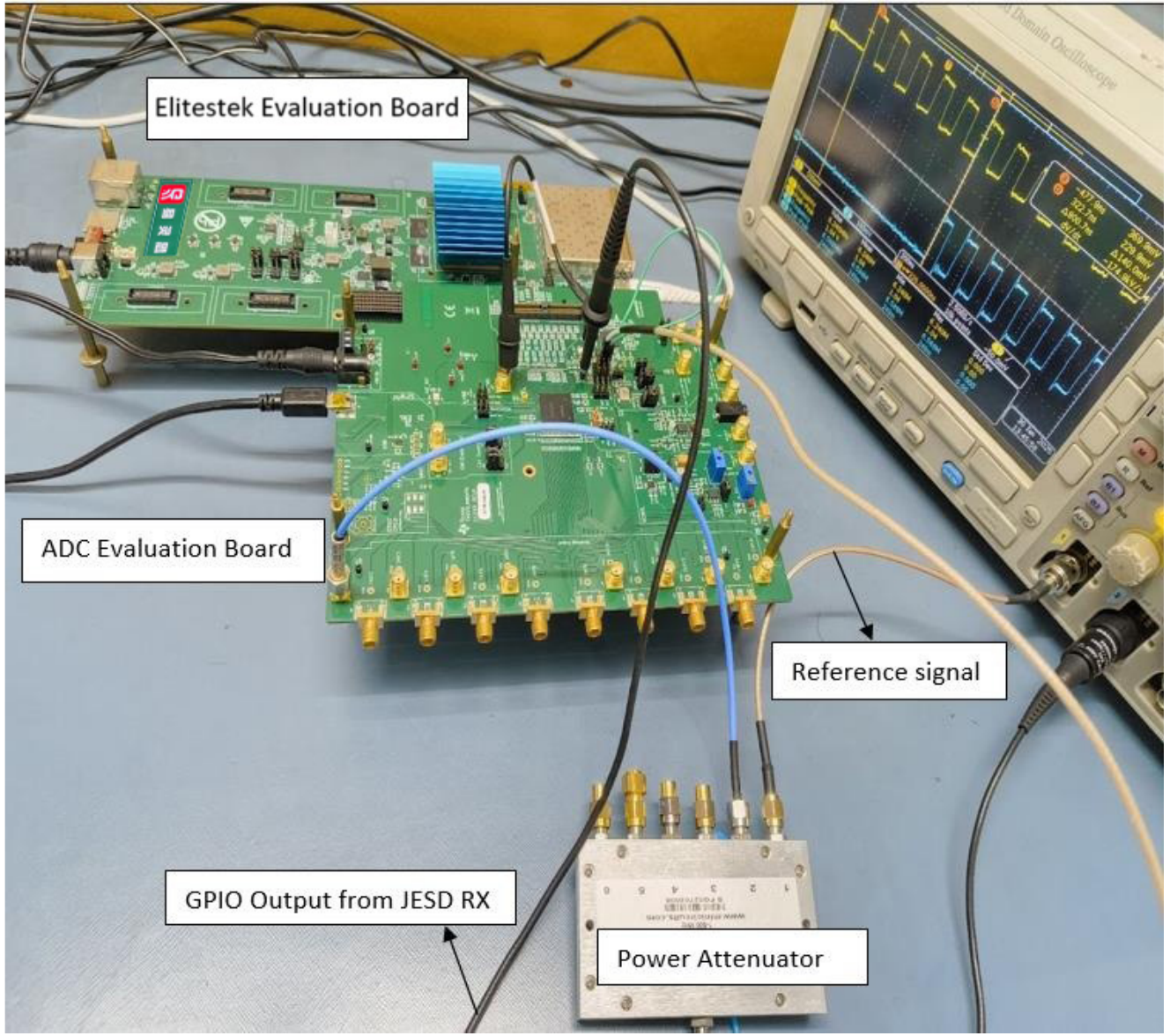
- Square wave with 50% duty cycle is sent from the FPGA
- Port 1 of Splitter is connected to ADC input
- Port 2 of Splitter is connected to Oscilloscope



Test Procedure

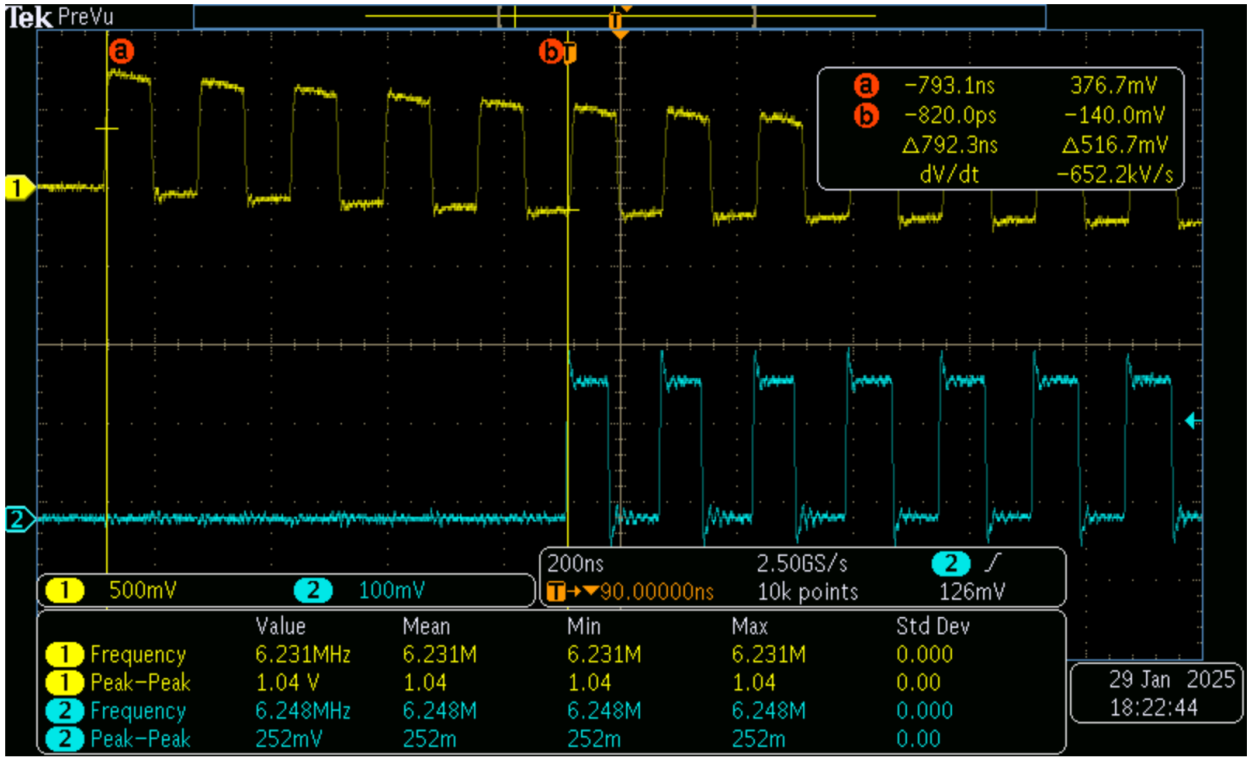
1. The procedure is same as the one explained in slide number 17 .
2. For deterministic latency set up the trigger condition in the Oscilloscope

Test Set up



ADC : Deterministic Latency Testing Result

Reset Type	Mode	Min Value (ns)	Typical Value (ns)	Max Value (ns)	No. of Iterations	Variation (ps)
Cold	40X	789.81	789.95	790.1	30	150
Warm	40X	789.81	789.91	790.03	30	100



Queries ?

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Thank You!

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