logic fruit Technologies

DAC Testing with LFT JESD204B TX IP ported on Elitestek Evaluation Board White Paper

Date: 16th April 2025

Contents

1. DAC38J84 Device

1.1 DAC38J84 Description

The terminal-compatible DAC38J84 family is a 16-bit, quad-channel, 1.6/2.5 GSPS digital-to-analog converter (DAC) with JESD204B interface.

Digital data is input to the device through 1, 2, 4, or 8 configurable serial JESD204B lanes running up to 12.5 Gbps with on-chip termination and programmable equalization. The interface allows Subclass 1 SYSREF-based deterministic and full synchronization of multiple devices.

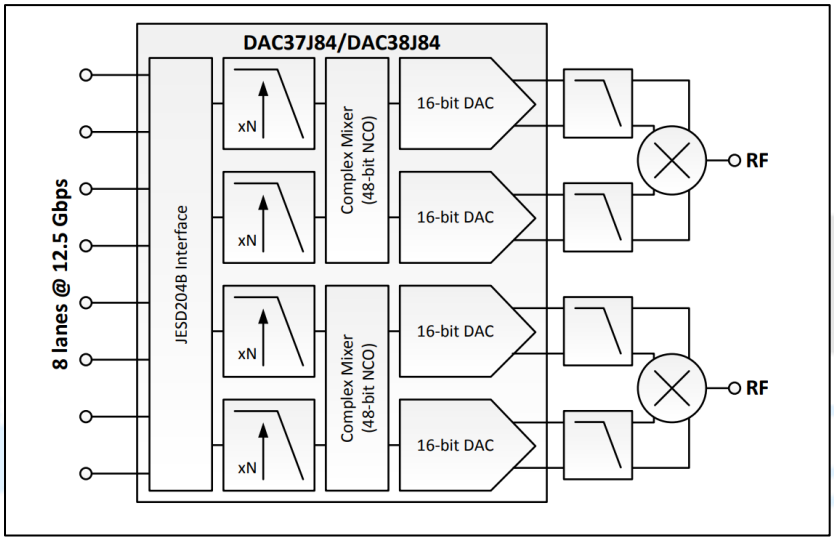

Figure 1: DAC38J84 Block Diagram

1.2 Features of DAC38J84

- 16-bit Sample Resolution
- 1.23 GSPS Maximum Input Data Rate
- 2.5 GSPS Maximum Sample Rate
- JESD204B Serial Interface with features supporting
  - 8 JESD204B Serial Input Lanes
  - 12.5 Gbps Maximum Bit Rate per Lane

- Subclass 1 Multi-DAC Synchronization
- On-Chip Very Low Jitter PLL
- Selectable 1x -16x Interpolation
- 3/4-Wire Serial Control Bus (SPI):1.5 V – 1.8 V
- Integrated Temperature Sensor

2. Logic Fruit JESD204B Transmitter IP

2.1 IP Block Diagram

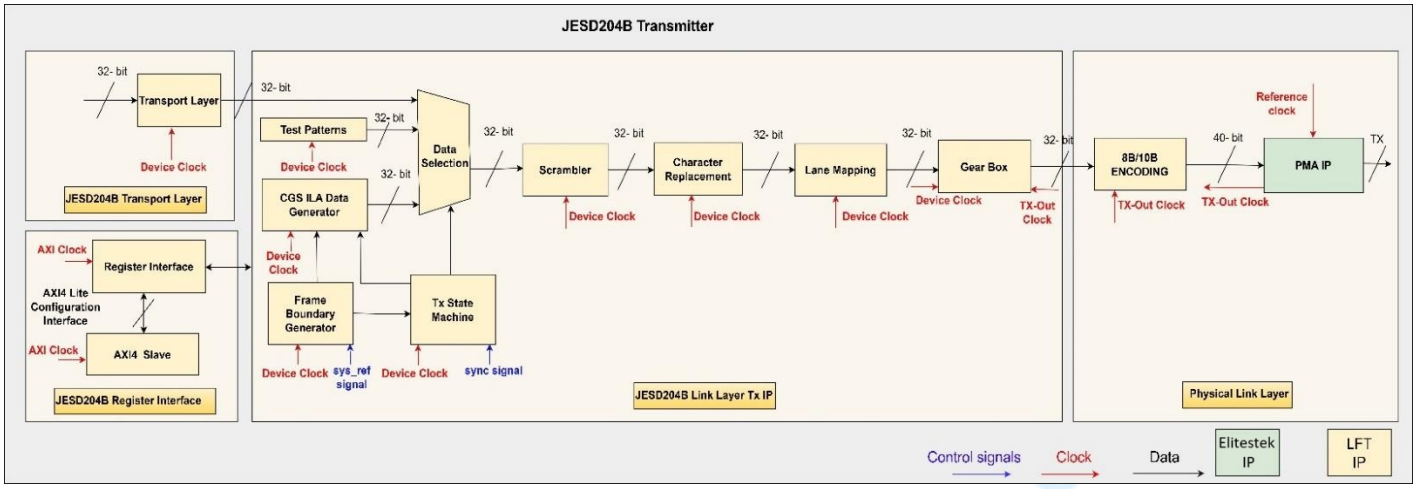

Figure 2 : Logic Fruit JESD204B Transmitter IP Block Diagram

2.2 IP Features

- Design as per JESD204B Standard.
- Supports Data Rate up to 12.5 Gbps
- Supports up to 8 lanes per core (This limitation is due to the Transceivers).
- Supports Link Layers.
- Supports Subclass 0 and 1.
- Does not support Subclass 2.
- Number of Frames per Multiframe (K) = 1 to 32

- Number of Samples per Frame (F) = 1 to 256
- Supports Scrambling.
- Supports Initial Lane Alignment.
- Supports Character Replacement.
- AXI Stream Data interface.
- AXI Lite Configuration interface.

3. DAC38J84 testing using Logic Fruit JESD204B Transmitter IP

3.1 Testing Hardware Setup Block Diagram

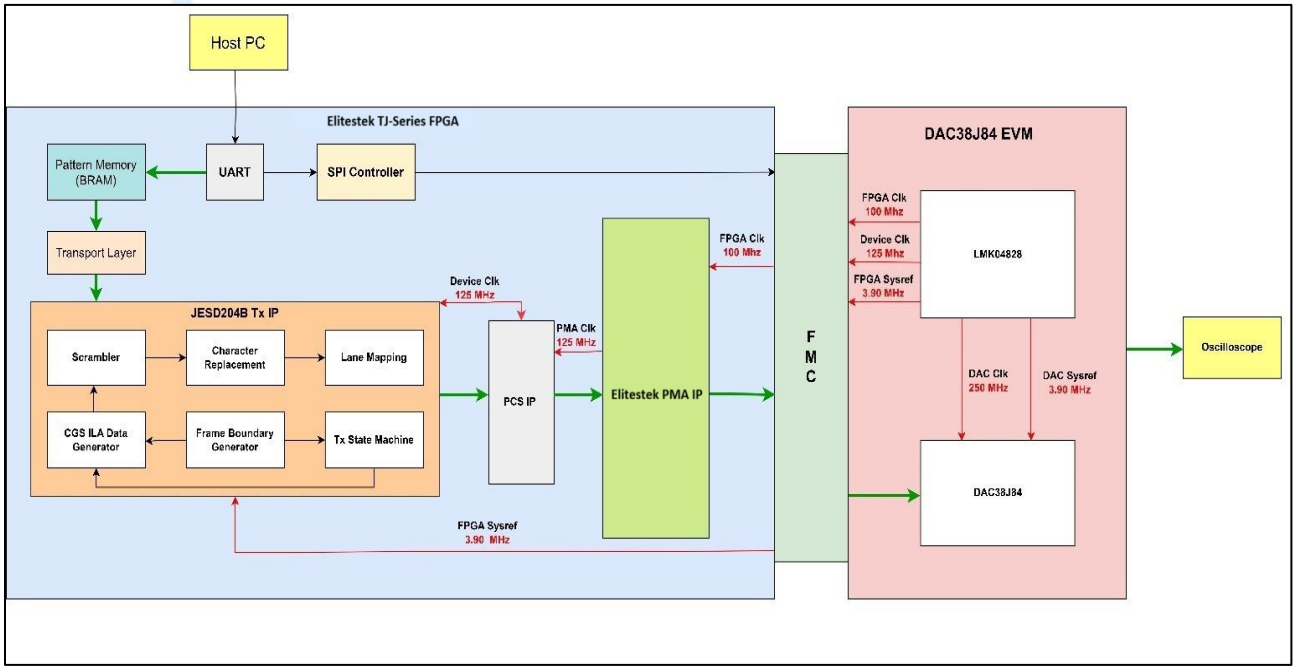

Figure 3: Hardware design for DAC38J84EVM testing using Elitestek TJ375N1156X FPGA Evaluation Board and LFT JESD204B TX IP

The chip LMK04828 on DAC38J84 EVM acts as a low-jitter Clock source for the DAC, FPGA, and Device Clocks. SYSREF is also generated for the same clock source since it must be synchronous with the Device clock and DAC Clock for SubClass1 operation.

Here, for the line rate of 5 Gbps, the JESD204B Tx IP operates on a 40-bit data width, whereas the JESD204B Rx IP on the DAC38J84 EVM operates on a 20-bit data width.

The DAC register is configured through the SPI Controller in the JESD204B TX IP Application layer.

The data samples sent to the DAC are fed into the pattern memory block via the UART. These samples are continuous sinusoidal waves of fixed sample rate generated using MATLAB/Octave software. These samples are stored in a Block RAM in the pattern memory module.

On the JESD link up, the samples in the Block RAM are played continuously on the DAC38J84.

The TX State machine block in the link layer is responsible for the JESD204b Linkup by handling different states: IDLE, CGS, ILA, and Data. Depending upon the type of subclass and programmed values of K and F, the State machine moves to different states before linkup. The user can access the AXI register set on the FPGA using the UART Interface.

3.2 Test Modes of JESD204B TX IP with DAC

Here are the JESD204B parameters :

LMF :

L = Number of JESD204B Lanes in the Link

M = Number of Converters per device

F = Number of octets per frame clock period.

The following are the different modes of testing done for DAC:

- Test Cases for 5 Gbps

SerDes Clock = SerDes Rate / SerDes Data Width

Chipset	SerDes Rate	SerDes Data width (Resolution after 8b10b)	SerDes Clock
LFT JESD204B TX (Elitestek FPGA)	5 Gbps	40 bits	125 MHz
TI DAC38J84	5 Gbps	20 bits	250 MHz

- Serdes Rate = 5 Gbps
- FPGA JESD204B Clock = 125 MHz
- FPGA Reference Clock = 100 MHz
- FPGA Sysref = 3.90625 MHz
- DAC Clock = 250 MHz
- DAC Sysref = 3.90625 MHz
- No. Of Frames per MultiFrame (K) =32

DAC Input sampling rate = SerDes Rate / (DAC Resolution after 8b10b * Number of converters in a single lane)

DAC Output sampling rate = DAC Input sampling rate * Interpolation Factor

Test Case	Modes (LMF)	Interpolation	No. of converters in single-lane	DAC Input Sampling Rate (MSPS)	DAC Output Sampling Rate (MSPS)	LMK Sysref	Line Rate (Gbps)
0	442	x1	1	250.00	250.00	Continuous	5.00
1	442	x2	1	250.00	500.00	Continuous	5.00
2	442	x4	1	250.00	1000.00	Continuous	5.00

3	244	x2	2	125.00	250.00	Continuous	5.00
4	244	x4	2	125.00	500.00	Continuous	5.00
5	244	x8	2	125.00	1000.00	Continuous	5.00

- **Example : Test Case 5 : LMF = 244, x8 interpolation**

  Input frequency = 10MHz

Figure 4: Time domain 10 MHz output waveform for x8 interpolation, LMF = 244 mode

4. Deterministic Latency Testing

The JESD204B Standard's deterministic latency is the latency from the frame-based data input at the TX to the frame-based data output at the RX. Provided timing requirements are met, latency should be programmable and repeatable on power cycles and re-sync events.

The Block RAM programs input samples as the input to JESD204B Transmitter IP, which are sent to JESD204B Receiver and subsequently to DAC38J84. A trigger signal, which is controlled through the AXI register set, is used to ensure deterministic latency behavior. This trigger signal triggers the Block RAM to send data to the input of the Transmitter.

4.1 Deterministic Latency Testing Block Diagram

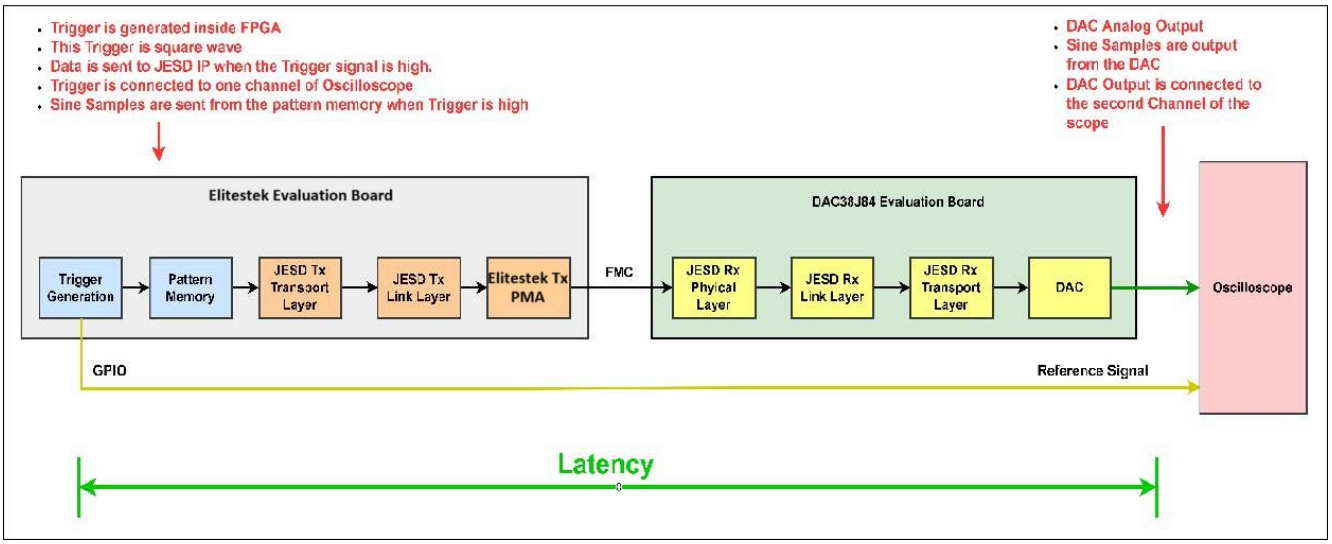

Figure 5 : Deterministic Latency Testing Setup Description

The required trigger signal is generated inside the FPGA as a square wave, which is used as the reference signal for checking the deterministic latency. When the trigger signal is high, the sine samples are transmitted from the FPGA to the DAC. The deterministic latency is the time from the start of the trigger signal to the start of the DAC output sine wave.

4.2 JESD204B TX Modes for Deterministic Latency

- Test Cases for 5 Gbps
  - Serdes Rate = 5 Gbps

- FPGA JESD204B Clock = 125 MHz
- FPGA Reference Clock = 100 MHz
- DAC Clock = 250 MHz
- No. Of Frames per MultiFrame (K) = 32

Below are the test cases for Deterministic Latency Testing

Test Case	Modes (LMF)	Interpolation	Number of converters in a single lane	DAC Input Sampling Rate (MSPS)	DAC Output Sampling Rate (MSPS)	LMK Sysref	Line Rate (Gbps)
10	442	x4	1	250.00	1000.00	Pulsed	5.00
Multiple Reset Testcase							
11	442	x4	1	250.00	1000.00	Pulsed	5.00

Following are the Deterministic Latency Output waveforms for above mentioned test cases:

a) ***Case1*** *: LMF = 442, 4x Interpolation, Line Rate = 5Gbps*

Signal	Frequency (MHz)
DAC Clock	1000
Device Clock (Logic Clock)	125
SYSREF (Pulsed Mode)	3.90625

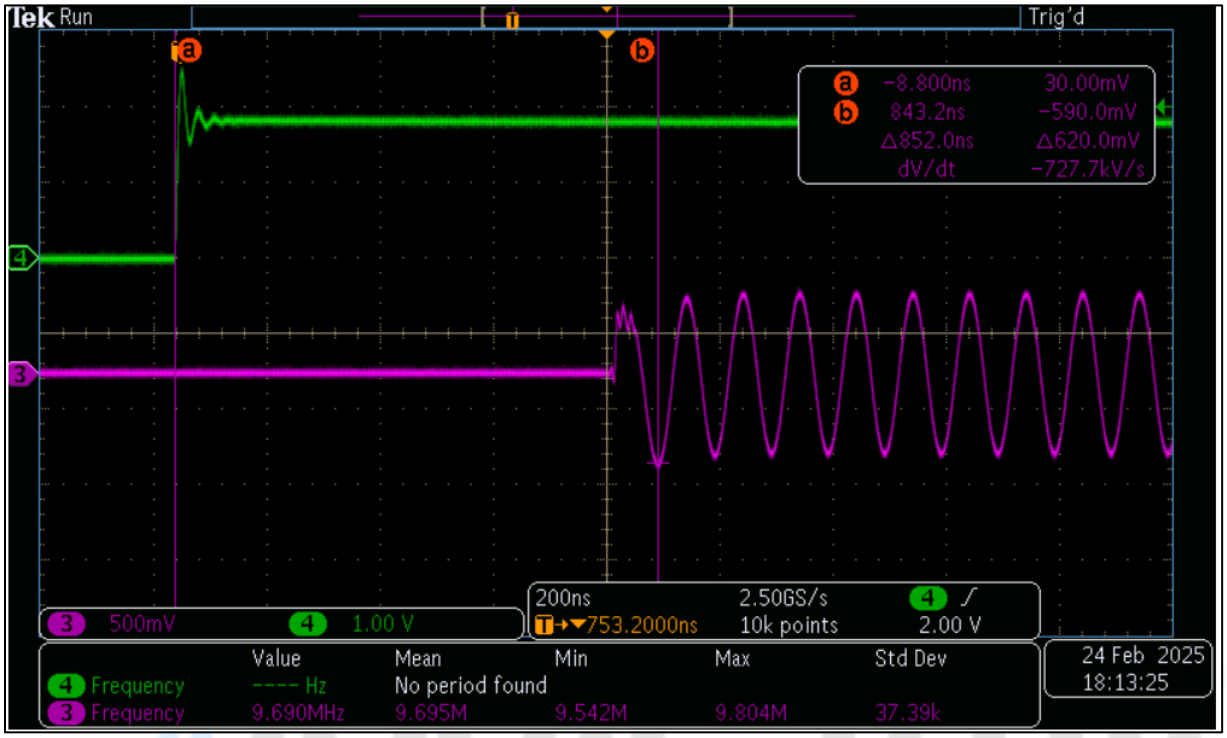

Figure 6.Deterministic Latency capture between trigger signal(green) and DAC output(pink) at input frequency of 10MHz

In the above image, the green waveform represents the trigger pulse given to the Block RAM, after which it starts transmitting data to the Transmitter Input.

The pink waveform represents the 10 MHz DAC Output.

As the scope measures, the delay between the trigger pulse rising edge and DAC waveform is 852.00 ns.

The table below shows the variation of Deterministic Latency values on different types of resets.

Reset Type	Mode (LMF)	Interpolation	Min Value (ns)	Typical Value (ns)	Max Value (ns)	No. of Iterations	Variation (ps)
Cold	442	4x	852.00	852.00	852.15	30	150
Warm	442	4x	852.00	852.00	852.10	30	100