logic fruit Technologies

ADC Testing with LFT JESD204B RX IP ported on Elitestek Evaluation Board White Paper

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1 AFE58JD48 Device

1.1 AFE58JD48 Description

AFE58JD48 is a 16-bit, Sixteen-channel, 125 MSPS analog-to-digital converter (ADC) with a JESD204B interface. It is realized through a multichip module with three dies: one 16-CH Voltage-Controlled Amplifier (VCA) die and two 8-CH analog-to-digital (ADC)Dies.

The ADC die primarily supports a JESD204B interface that runs up to 12.8Gbps and reduces circuit board challenges in high-channel-count systems. Each ADC die supports x4 Serdes output for digital data communication with FPGAs.

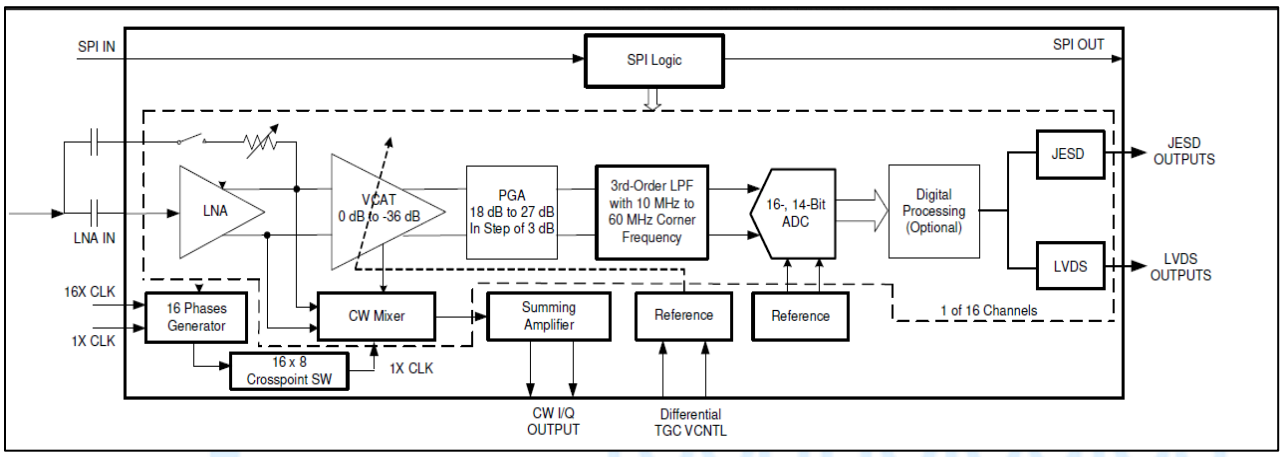

Figure 1 : AFE58JD48 Block Diagram

1.2 Features of AFE58JD48

- 16-bit Sample Resolution
- 125 MSPS Maximum Sample Rate
- Supports both JESD204B and LVDS-based serial data output.
- JESD204B Serial Interface with features supporting
  - 4 JESD204B Serial Output Lanes per ADC Die.
  - 10 Gbps Maximum data Rate per Lane (supports 12.8 Gbps for 10cm or below trace length).

  - Supports Subclass 0, Subclass 1, and Subclass 2 device operation.
  - Subclass 1 and Subclass 2-based synchronization.
- On-Chip Low Jitter PLL.
- 3/4-Wire Serial Control Bus (SPI)

2 Logic Fruit JESD204B Receiver IP

2.1 IP Block Diagram

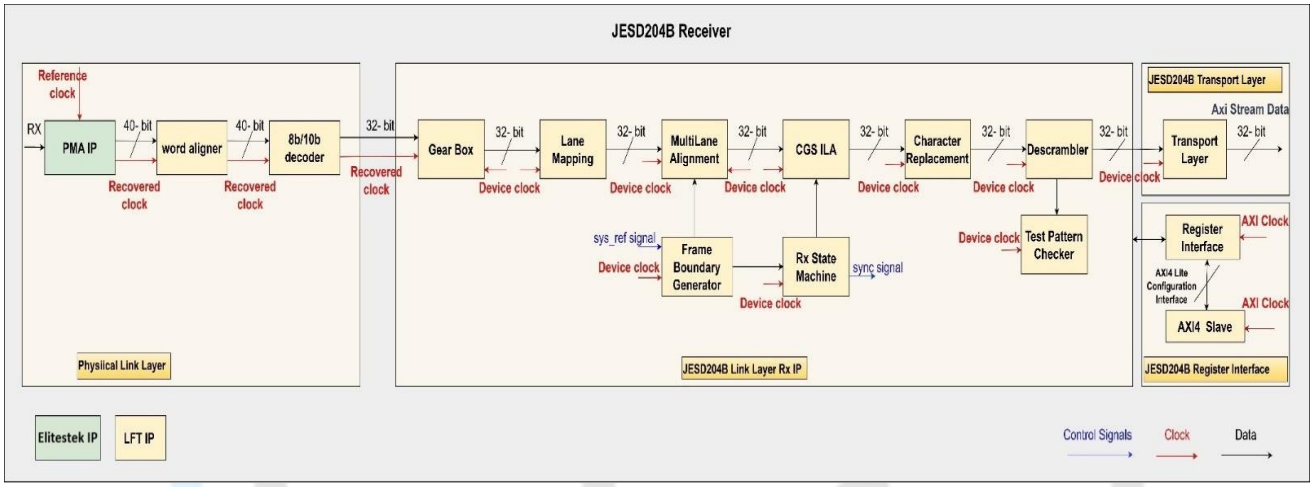

Figure 2: Logic Fruit JESD204B Receiver IP Block Diagram

2.2 IP Features

- Design as per JESD204B Standard.
- Supports Data Rate up to 12.5 Gbps
- Supports up to 8 lanes per core (This limitation is due to the Transceivers).
- Supports Link Layers.
- Supports Subclass 0 and 1.
- Does not support Subclass 2.
- Number of Frames per Multiframe (K) = 1 to 32
- Number of Samples per Frame (F) = 1 to 256
- Supports Scrambling.
- Supports Initial Lane Alignment.
- Supports Character Replacement.
- AXI Stream Data interface.
- AXI Lite Configuration interface.

3 AFE58JD48 testing using Logic Fruit JESD204B Receiver IP

3.1 Testing Hardware Setup Block Diagram

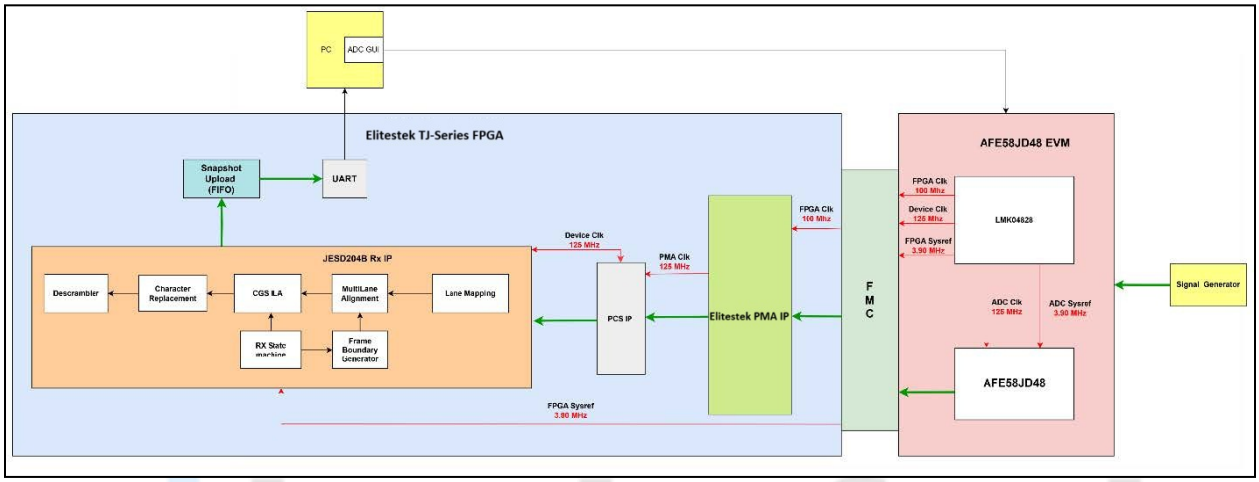

Figure 3 : Hardware design for AFE58JD48 testing using Elitestek TJ375N1156X FPGA Evaluation Board and LFT JESD204B RX IP

The LMK04826 on AFE58JD48EVM acts as a low-jitter Clock source for the ADC, FPGA, and Device Clocks. SYSREF is also generated for the same clock source since it must be synchronous with the Device clock and ADC Clock for SubClass1 operation.

Here, for the line rate of 5 Gbps, the JESD204B Rx IP operates on a 40-bit data width, and the JESD204B Rx IP present on AFE58JD48 EVM operates on a 40-bit data width. The reference PMA Clock is 100 MHz

The AFE58JD48EVM configuration is done through the USB interface provided on board. The AFE58JD48EVM provides a GUI for configuration and debugging. FPGA JESD204B RX IP configuration is done through UART from the host PC. The user can access the AXI register set on the FPGA using the UART Interface.

The data received from the ADC is decoded and mapped into each lane. The multilane alignment module receives the mapped input data and transmits the data on all the lanes in an aligned

manner. The RX state machine is responsible for the JESD204B link up by handling different states: IDLE, CGS, ILA, and Data. Depending upon the type of subclass and programmed values of K and F, the State machine moves to different states before linkup. In the data phase, the character alignment block monitors the characters that are aligned in the received data stream. In the data transmission phase, corresponding characters are replaced based on frame and multi-frame boundaries. Depending on the ADC modes, the received data is mapped and sampled at the output in the transport layer.

3.2 Test Modes of JESD204B RX IP with ADC

Here are the JESD204B parameters:

LMF :

L = Number of JESD204B Lanes in the Link

M = Number of Converters per device

F = Number of octets per frame clock period.

- Test Cases for 5 Gbps

SerDes Clock = SerDes Rate / SerDes Data Width

Chipset	**SerDes Rate**	**SerDes Data width (Resolution after 8b10b)**	**SerDes Clock**
LFT JESD204B RX (Elitestek FPGA)	5 Gbps	40 bits	125 MHz
TI ADC AFE58JD48	5 Gbps	40 bits	125 MHz

The following is the mode of testing done for ADC:

ADC Input sampling rate = SerDes Rate / (ADC Resolution after 8b10b * No of converters in a single lane)

Test Case	Modes (LMF)	No. of converters in single lane	ADC Input Sampling Rate (MSPS)	ADC Output Sampling Rate (MSPS)	LMK Sysref	Line Rate (Gbps)
0	484 (40X)	2	125.00	125.00	Continuous	5.00

Example:- TC0: Mode 484 at 5 Gbps

Parameter	Value
Number of lanes	1
ADC SerDes Rate	5 Gbps
ADC Resolution after 8b/10b	20 bits
No. of converters in single lane	2
ADC Input sampling rate	5/ (20*2) = 125MSPS

Input Frequency = 62.5 MHz

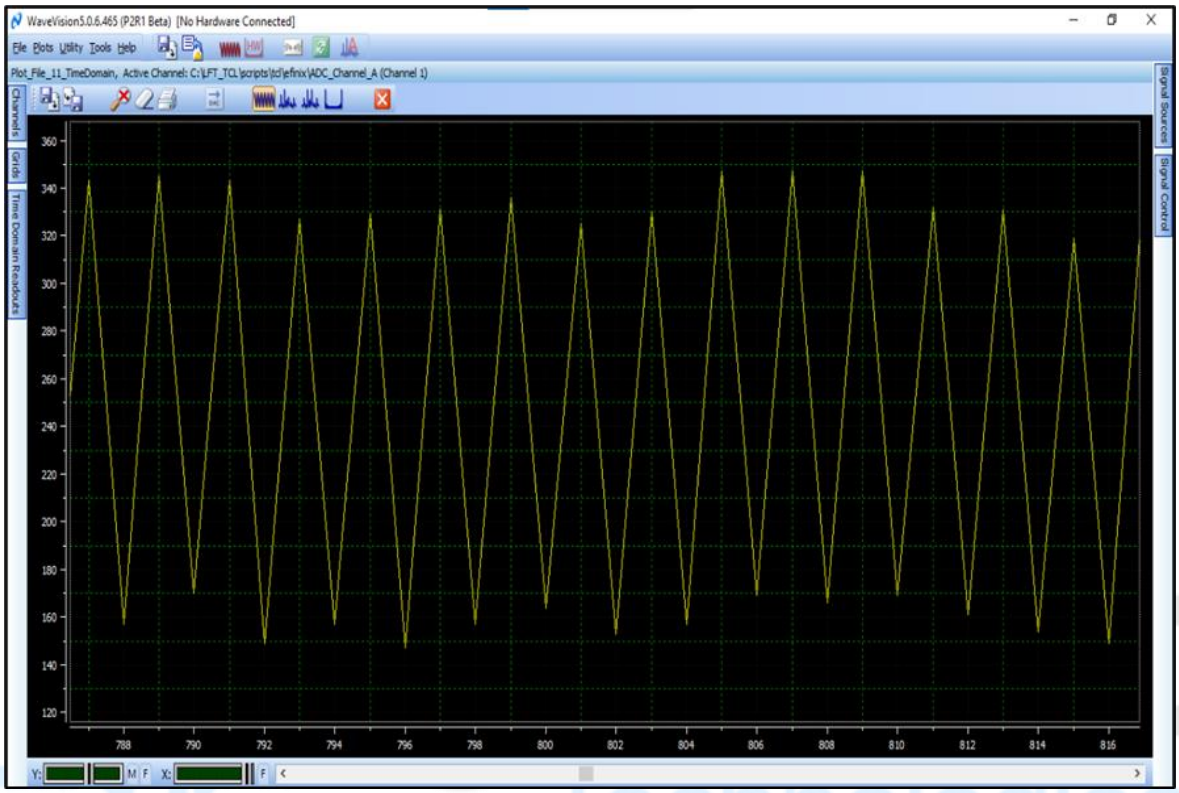

Figure 4: Time domain plot for captured waveform for input frequency of 62.5 MHz

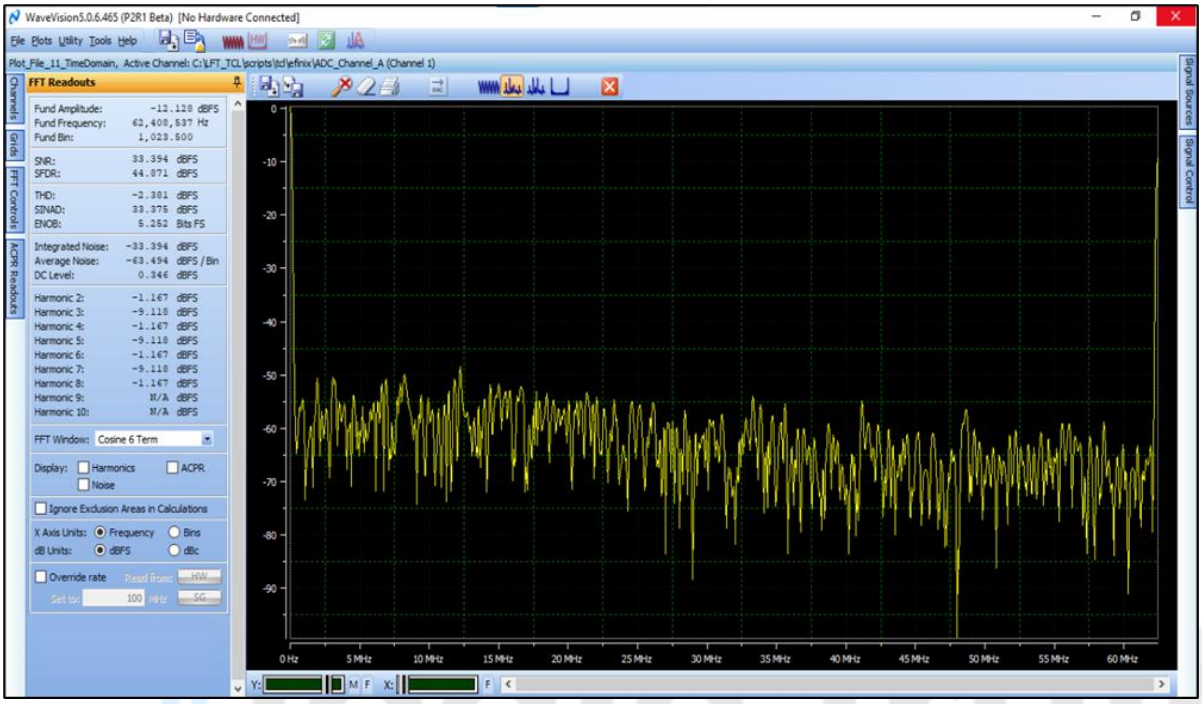

Figure 5: frequency domain plot for captured waveform for input frequency of 62.5 MHz

4 Deterministic Latency Testing

The JESD204B Standard's deterministic latency is the latency from the frame-based data input at the TX to the frame-based data output at the RX. Provided timing requirements are met, latency should be programmable and repeatable over power cycles and re-sync events.

A square wave is generated from an FPGA of 6.25 MHz, which is sent on the output through one of the AFE58JD48EVM GPIO via FMC. This square wave is the reference signal for measuring deterministic latency and ADC sampling input. The sampled input is sent to the FPGA JESD204B RX IP via the JESD204B interface, where in the transport layer the MSB bit of each sample is extracted and sent to the AFE58JD48 GPIO for capturing at the Oscilloscope for measurement. The sampled MSB bit is compared with respect to the reference square wave to calculate the total delay in the path.

4.1 Deterministic Latency Testing Block Diagram

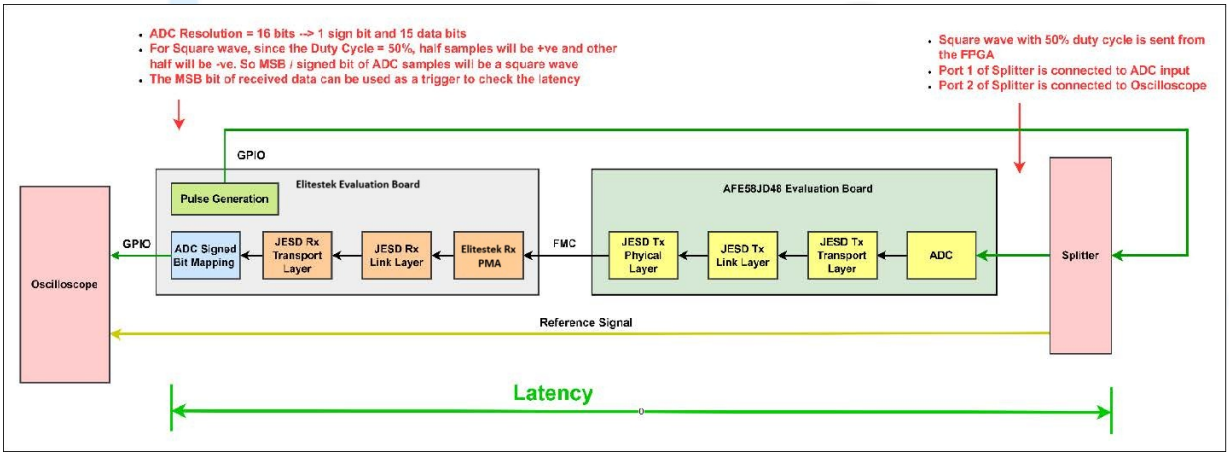

Figure 6: Deterministic Latency Testing Setup Description

The pulse generation block in the Elitestek FPGA will generate a square wave, which is fed to the splitter. The Port 1 of the splitter port will be connected to the Oscilloscope as a reference signal and the Port 2 is given as an input to the ADC. The MSB bit of the received data from the JESD204B RX Transport layer present in Elitestek FPGA is used as a trigger to check the latency. The deterministic latency is determined from the start of the reference signal to the start of the signed bit of the ADC sample.

4.2 JESD204B RX Modes for Deterministic Latency

Below are the test cases for Deterministic Latency Testing

Test Case	Modes (LMF)	No. of converters in single lane	ADC Input Sampling Rate (MSPS)	ADC Output Sampling Rate (MSPS)	LMK Sysref
1	484 (40X)	2	125.00	125.00	Continuous

Below are some snapshots of oscilloscope showing the latency measurement example.

a) **Case1** : LMF = 484, Line Rate = 5Gbps

Signal	Frequency (MHz)
ADC Clock	125
Device Clock (Logic Clock)	125
SYSREF (Pulsed Mode)	3.90625

Figure 7: Deterministic Latency capture between reference square pulse(green) and ADC samples MSB output(pink).

In the above image, the green waveform represents the reference square pulse generated by FPGA. Pink waveform represents the ADC samples MSB bit output. As the scope measures, the delay between the reference square pulse rising edge and ADC samples MSB bit rising edge, delay comes to be 789.9 ns. Below table shows the variation of Deterministic Latency values on different types of resets.

Multiple Reset testcase is one in which the linkup sequence is run again without Power cycle, basically Warm reset. In the cold reset testcase complete board is power cycled.

Reset Type	Mode	Min Value (ns)	Typical Value (ns)	Max Value (ns)	No. of Iterations	Variation (ps)
Cold	40X	789.81	789.95	789.96	30	150
Warm	40X	789.81	789.91	789.91	30	100