logic fruit Technologies

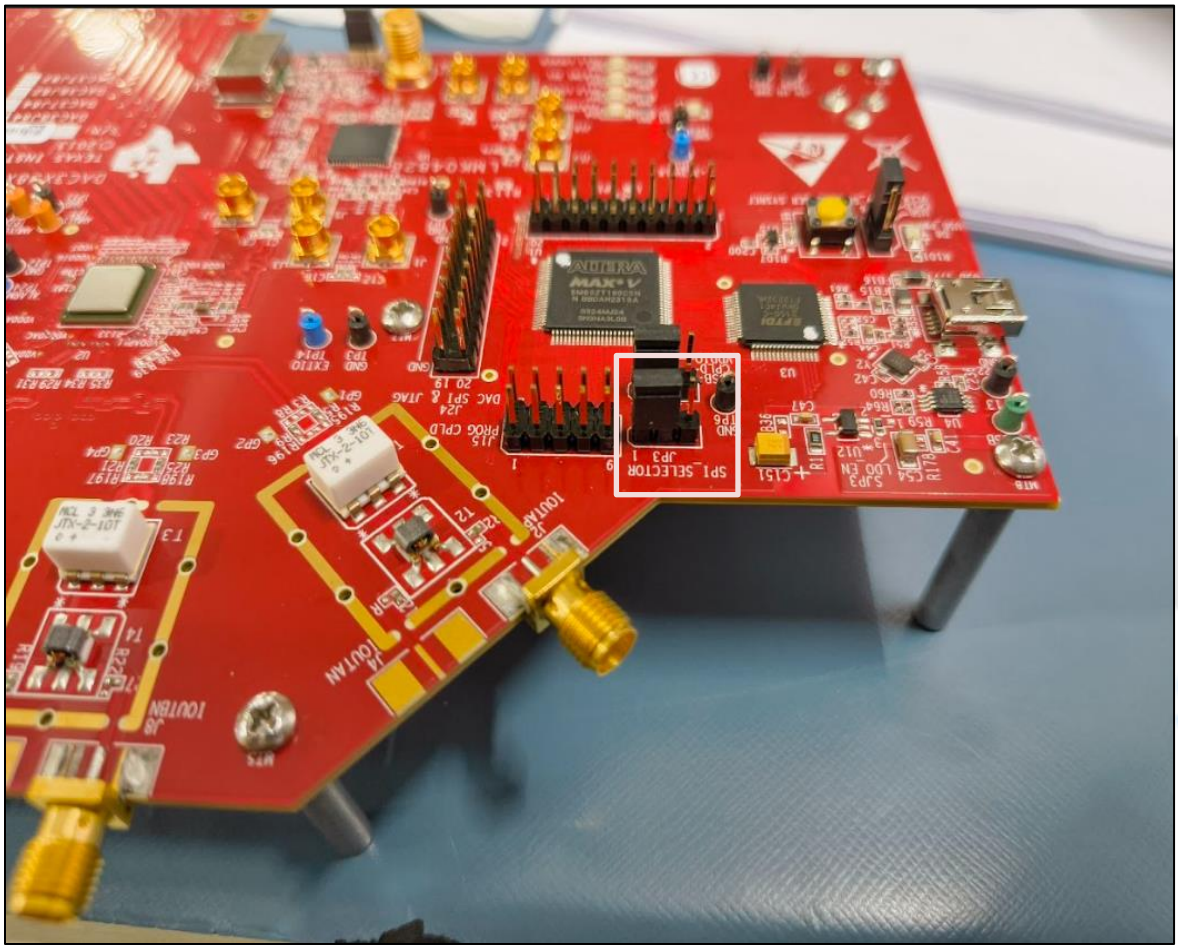
Hardware changes on ADC and DAC for JESD204B Tx and RX Porting on Elitestek FPGA

Date: 25th February 2025

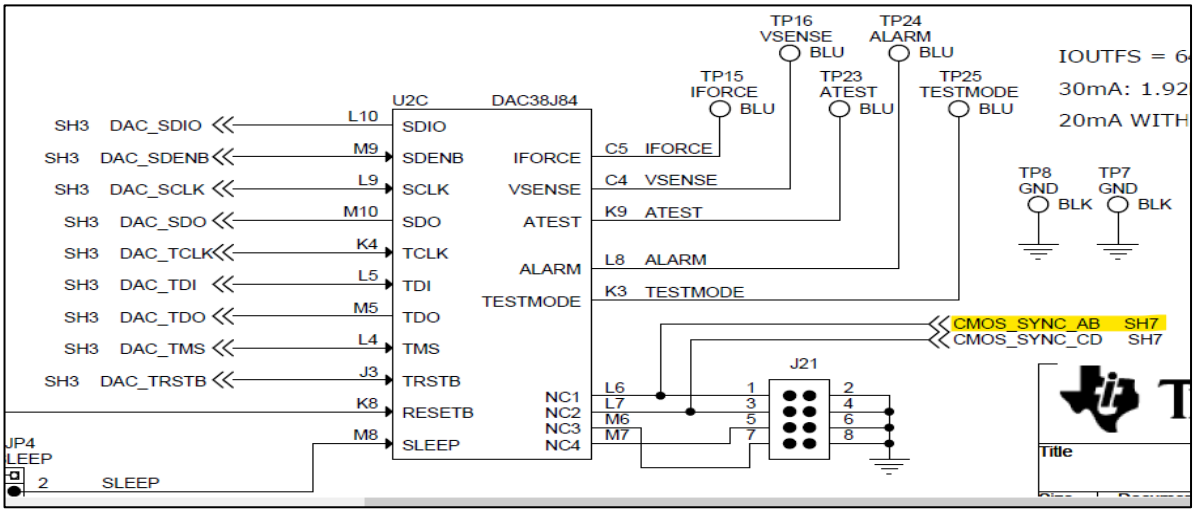
Contents

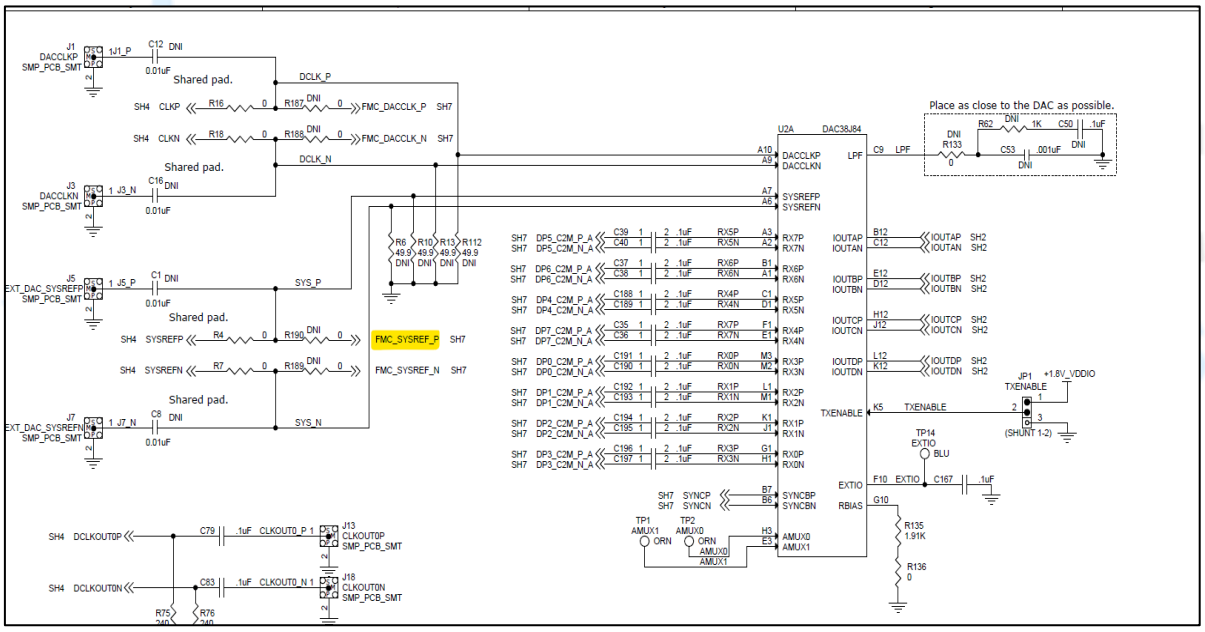
1 DAC Hardware changes

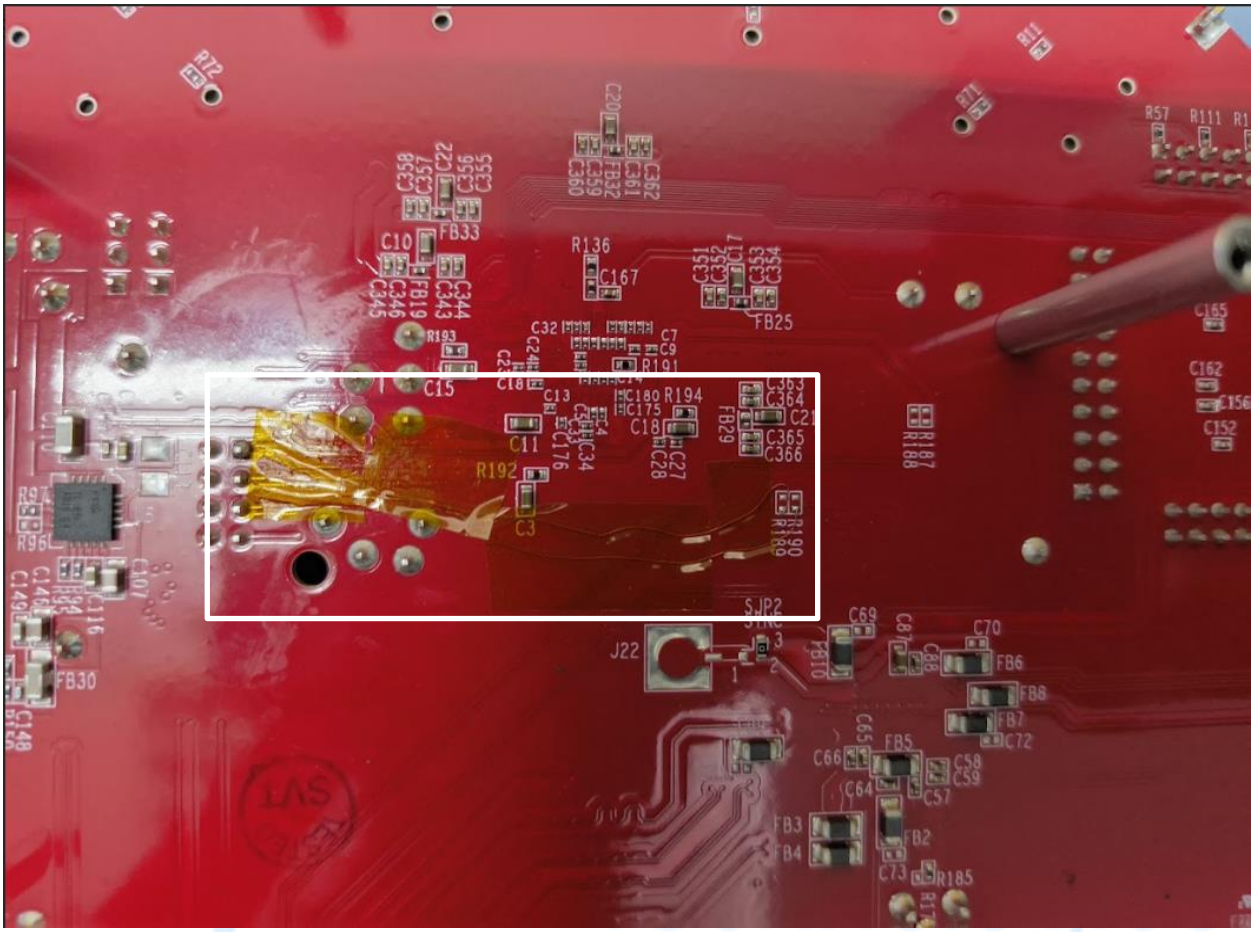
1. For SPI header position changed to 1-2 for configuration through FPGA



2. SYNC from header J21 mapped to FMC_SYSREF, which is mapped on the FMC connector


U2C
DAC38J84
SH3 DAC_SDIO
SH3 DAC_SDENB
SH3 DAC_SCLK
SH3 DAC_SDO
SH3 DAC_TCLK
SH3 DAC_TDI
SH3 DAC_TDO
SH3 DAC_TMS
SH3 DAC_TRSTB
L10 SDIO
M9 SDENB
L9 SCLK
M10 SDO
K4 TCLK
L5 TDI
M5 TDO
L4 TMS
J3 TRSTB
K8 RESETB
M8 SLEEP
IFORCE
VSENSE
ATEST
ALARM
TESTMODE
NC1
NC2
NC3
NC4
C5 IFORCE
C4 VSENSE
K9 ATEST
L8 ALARM
K3 TESTMODE
TP16 VSENSE BLU
TP24 ALARM BLU
TP15 IFORCE BLU
TP23 ATEST BLU
TP25 TESTMODE BLU
TP8 GND BLK
TP7 GND BLK
IOUTFS = 6
30mA: 1.92
20mA WITH
CMOS_SYNC_AB SH7
CMOS_SYNC_CD SH7
J21
L6
L7
M6
M7
JP4
LEEP
2 SLEEP
Title

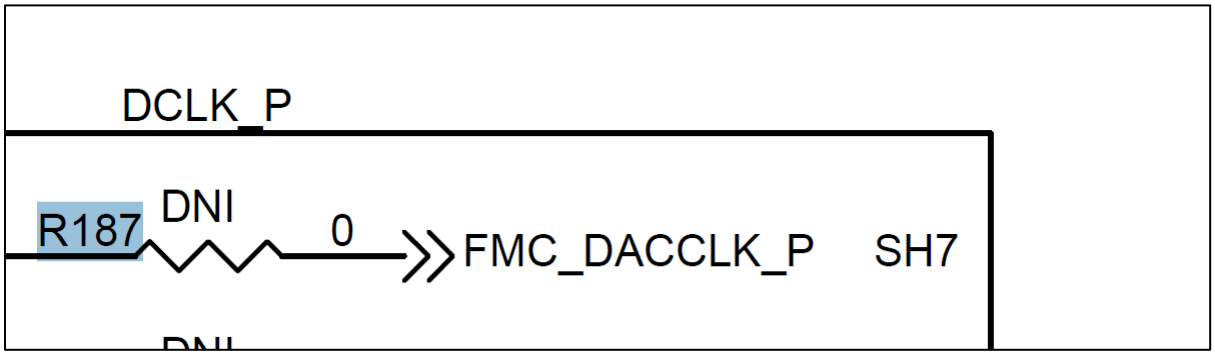

Shared pad.
DCLK_P
DCLK_N
SYS_P
SYS_N
FMC_SYSREF_P
FMC_SYSREF_N
FMC_DACCLK_P
FMC_DACCLK_N
U2A DAC38J84
Place as close to the DAC as possible.
DACCLKP
DACCLKN
SYSREFP
SYSREFN
IOUTAP
IOUTAN
IOUTBP
IOUTBN
IOUTCP
IOUTCN
IOUTDP
IOUTDN
TXENABLE
EXTIO
RBIAS
SYNCP
SYNCN
SYNCBP
SYNCBN
AMUX0
AMUX1
CLKOUT0P
CLKOUT0N

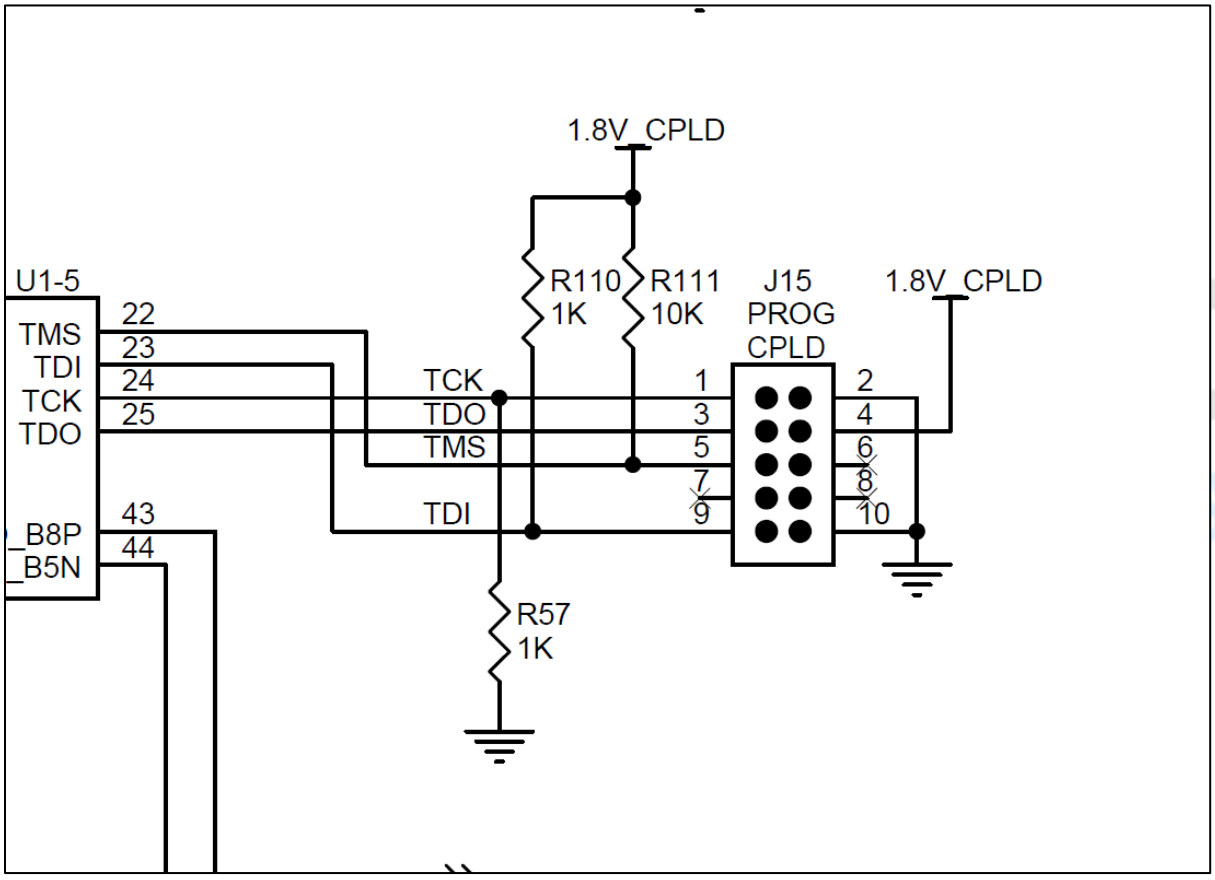


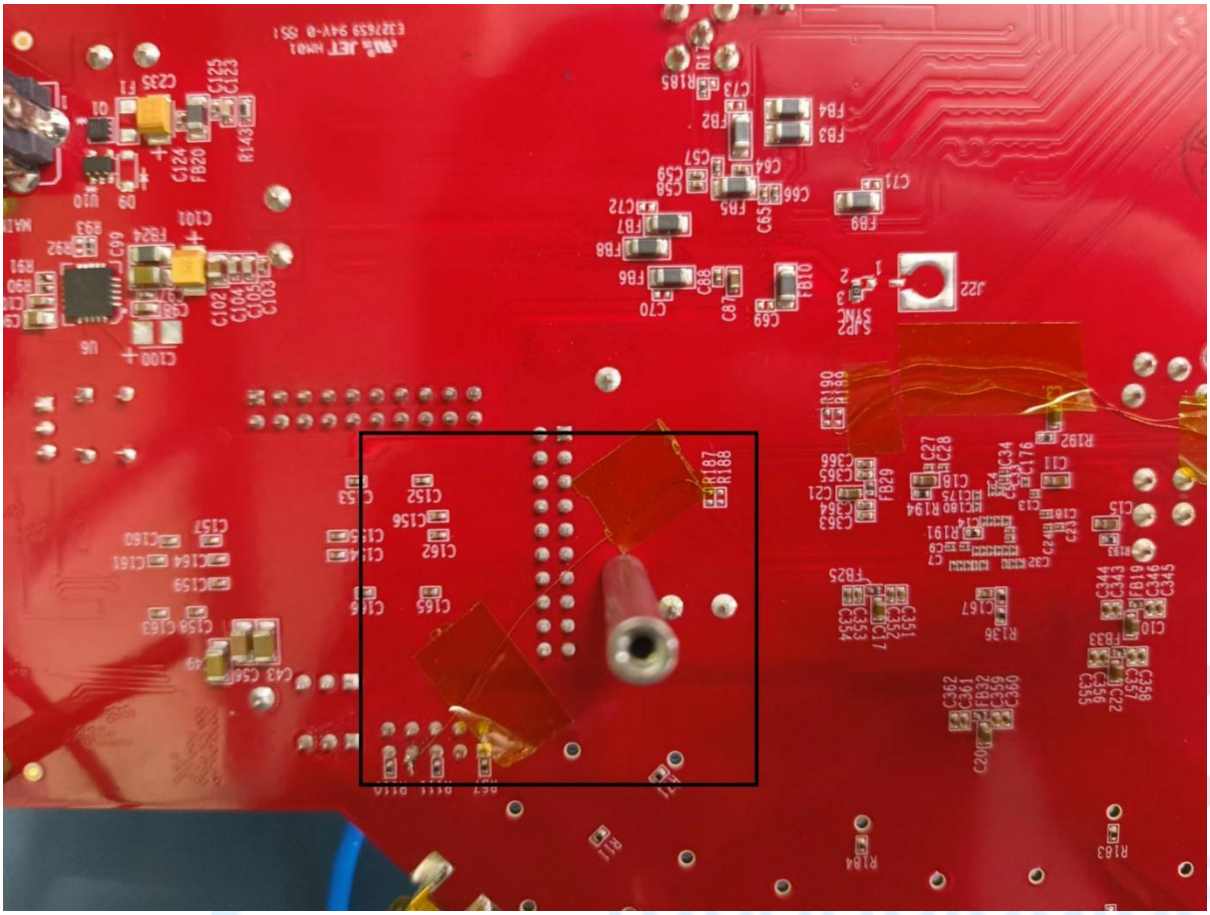
3. The following changes are made to test deterministic latency

To prove the deterministic latency, the sample trigger needs to be mapped to the GPIO header, but the Elitestek Evaluation board doesn't have any GPIO's, also the DAC card doesn't have any GPIO's mapped to any of the header. So, the following changes are made to map the trigger signal:

- The FMC_DACCLK_P signal from the FPGA is not used in the current design.
- The signal R187 on the DAC EVM has a DNP resistor. Connect a wire from one pad of the resistor on the FMC side to the J15 header PIN 7.


DCLK_P
R187
DNI
0
FMC_DACCLK_P
SH7

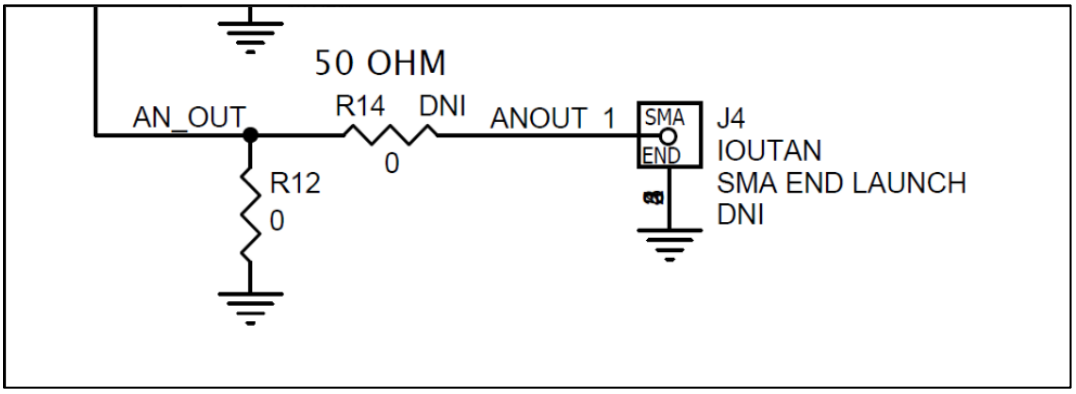

1.8V_CPLD
U1-5
TMS
TDI
TCK
TDO
22
23
24
25
43
44
_B8P
_B5N
TCK
TDO
TMS
TDI
R110
1K
R111
10K
J15
PROG
CPLD
1.8V_CPLD
1
2
3
4
5
6
7
8
9
10
R57
1K



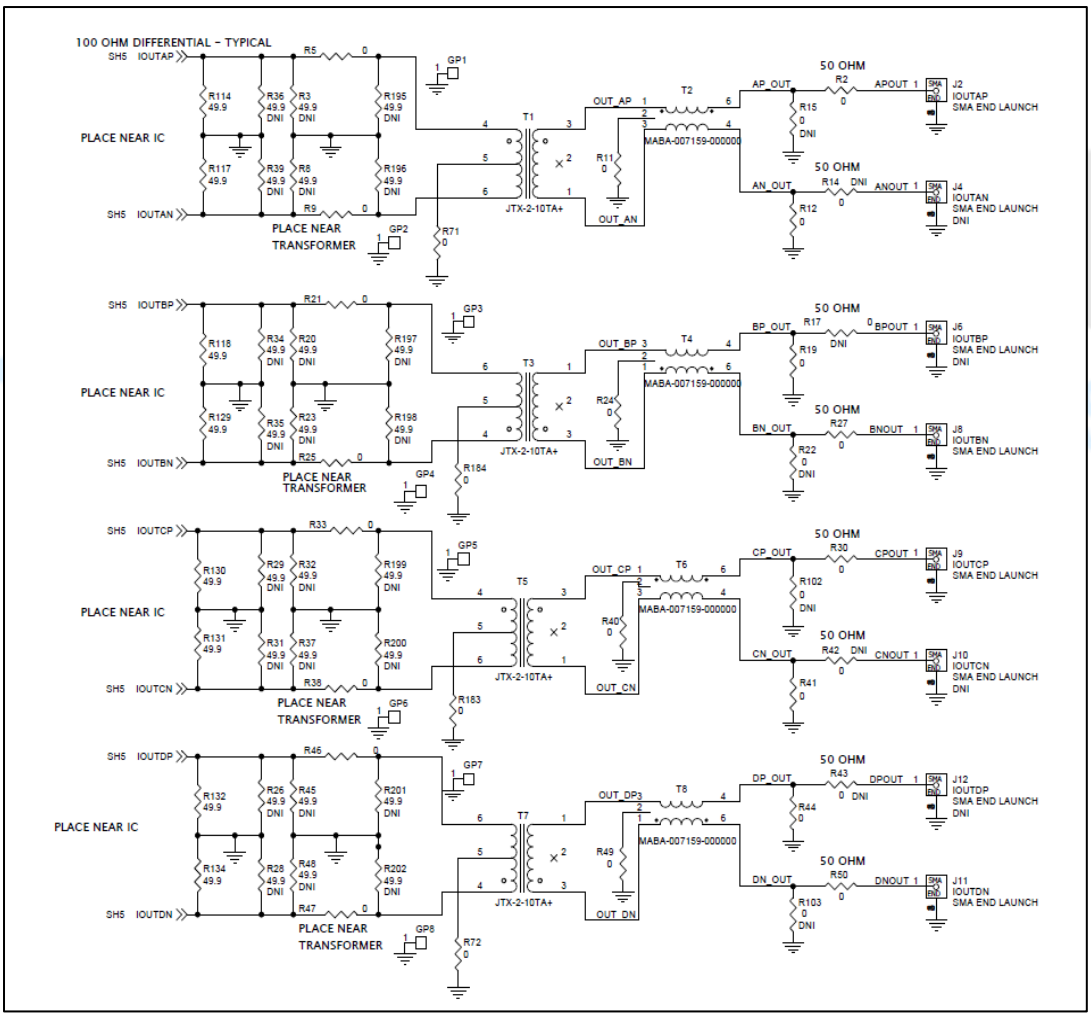
4. The following changes are made to get the same output on all DAC outputs.

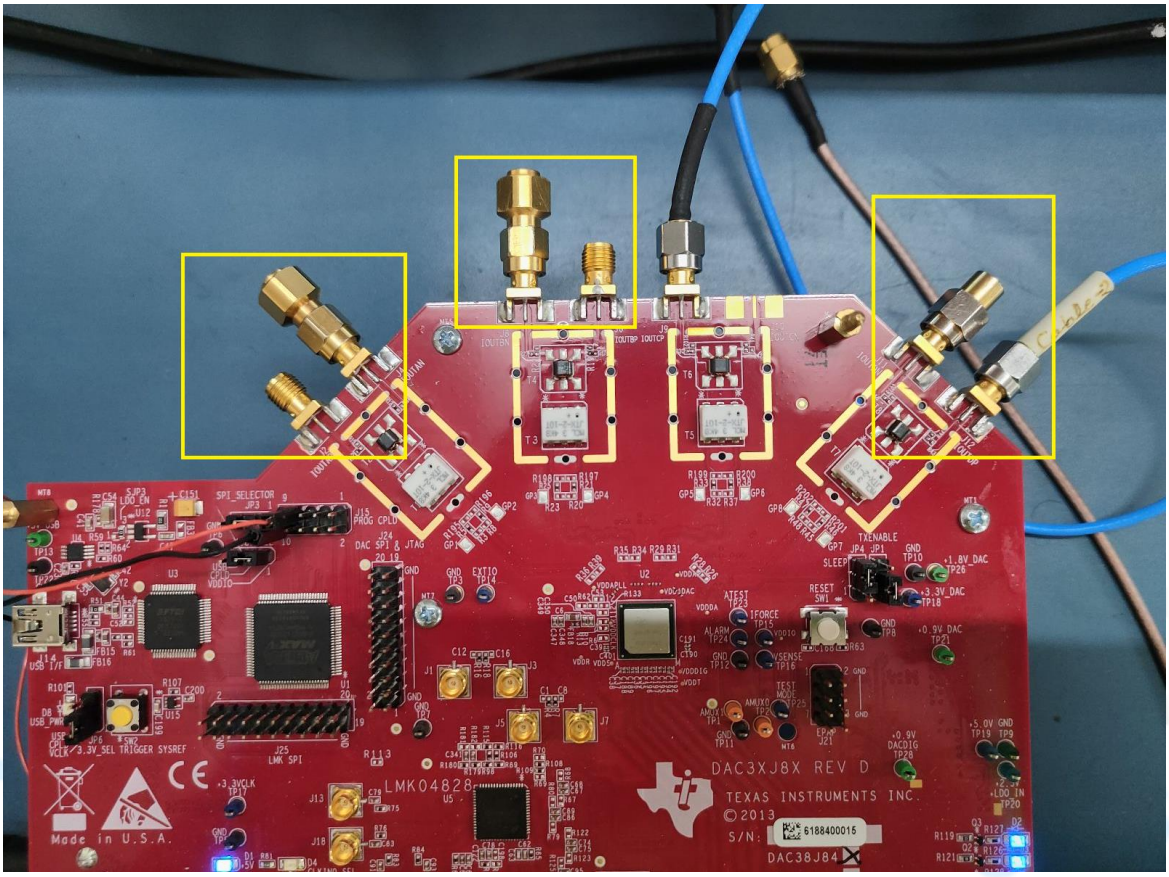
There were SMA connectors mapped on alternate polarities on channel AB and CD. To get same output on all the channels **add the SMA female connectors on other polarities wherever they are not present.**

- The R14 is mounted with 0 ohm and R12 0 ohm resistor is removed from the board.
- The J4 is mounted with SMA female header (similar changes are done for other paths).
- To make sure there is no impedance mismatch in the transmission lines, 50-ohm termination was used on SMA connectors.



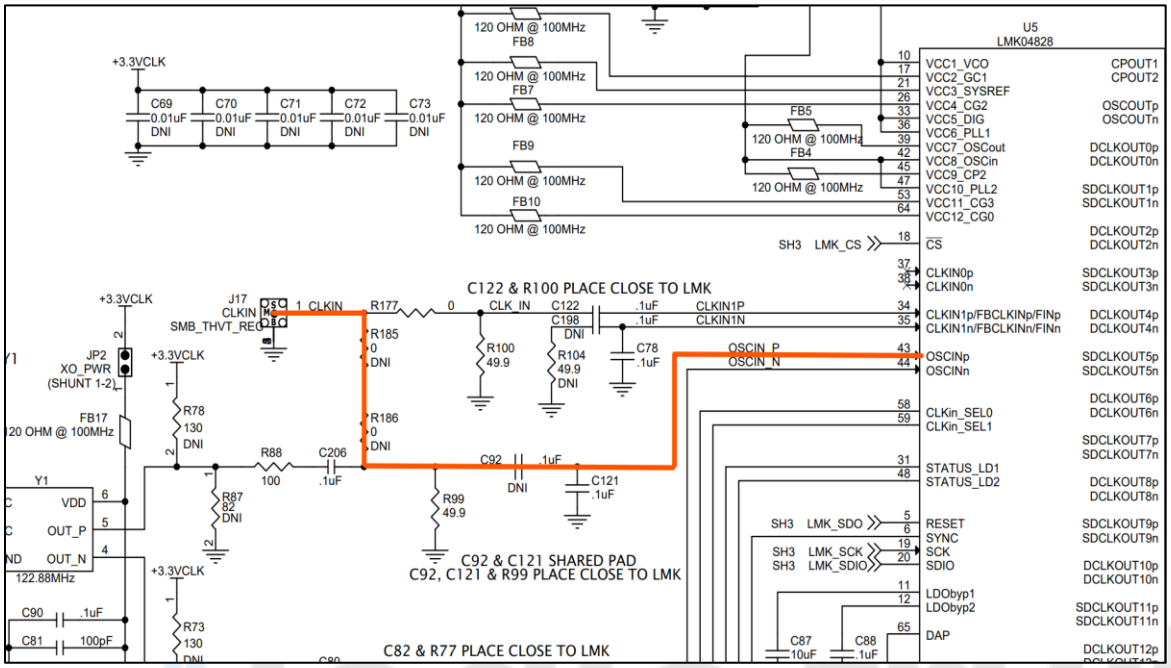
- Similar changes need to be made for other channels, where the P side is not mounted





5. External VCXO input :

   - Due to the less PDF2 value for PLL2, there was jitter on output clock which is the cause of 1.6ns variation in the output.
   - So to reduce this jitter on the output clock we need to change the VCXO clock input to the LMK chip, since there is only 122.88 MHz VCXO on board, we cannot change that.
   - Hence, we need to give a clock directly from some external source.
   - On board there is no SMA on the OSCIN pin on LMK, so we will be using CLKIN1 SMA for this external input and through some register changes we will enable the path from CLKIN1 to OSCIN input of LMK.



To enable the highlighted path, we need to do following modifications

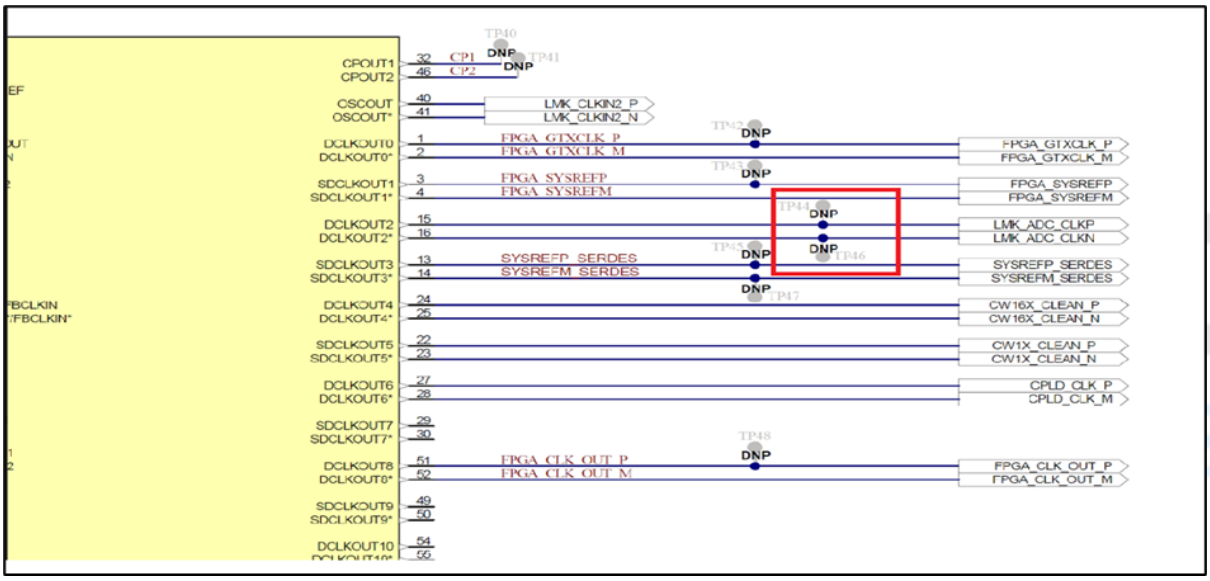
Reference	current state	Requirement	Remarks
R177	0 ohm	DNP	Required
R185	DNP	0 ohm	Required
R186	DNP	0 ohm	Required
C92	DNP	0.1uF	Required
C121	0.1uF	DNP	Required
R77	49.9 ohm	0 ohm	Not Required
C80	0.1uF	DNP	Required
C206	0.1uF	DNP	Required

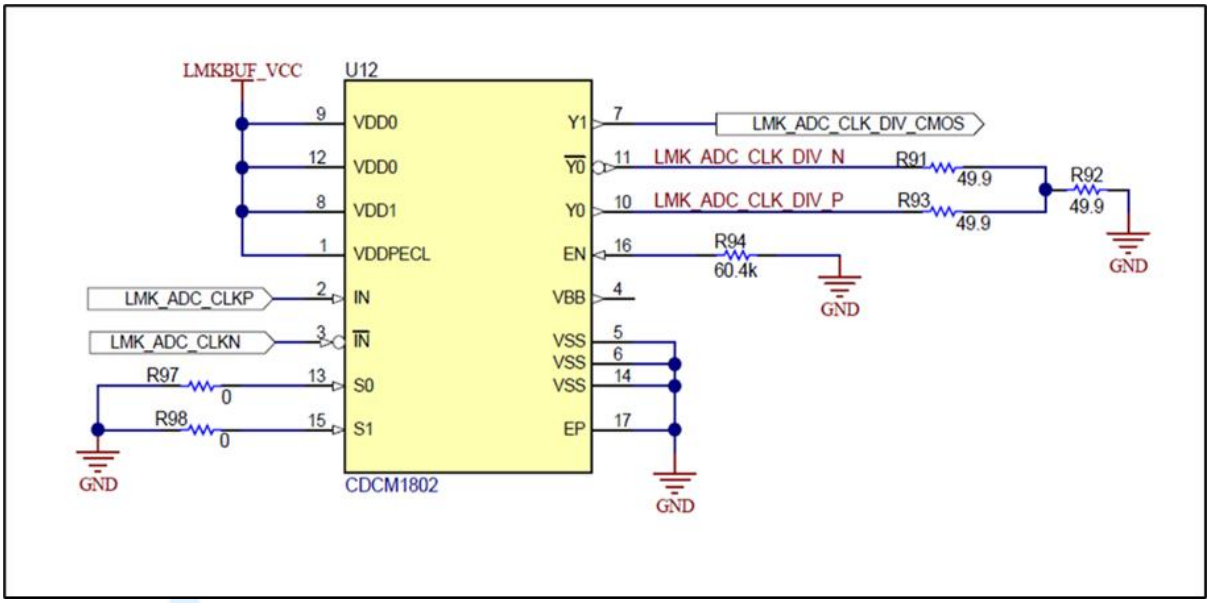
2 ADC Hardware changes

1. While testing the 40X PLL mode, the PLL was locked, but the output of the clock buffer used on the LMK to ADC path was noisy and the clock frequency was unexpected (some randomly changing frequency was observed on the scope).

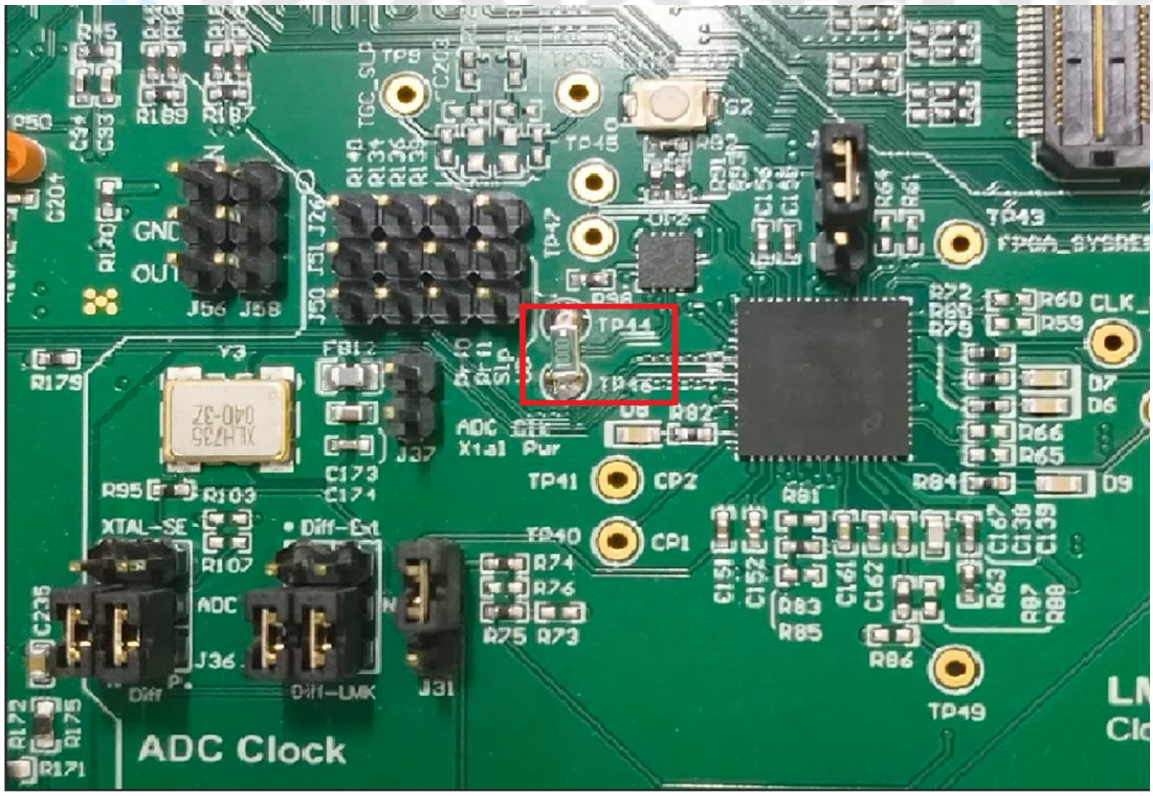
2. The clock buffer datasheet recommends adding a 100ohm termination at the input for LVDS clock input because the clock buffer input is high impedance. But on the eval board there was no termination on the input.

3. To overcome this issue, we added a 100ohm termination between the test points (TP44 and TP46) provided on board on the differential clock output



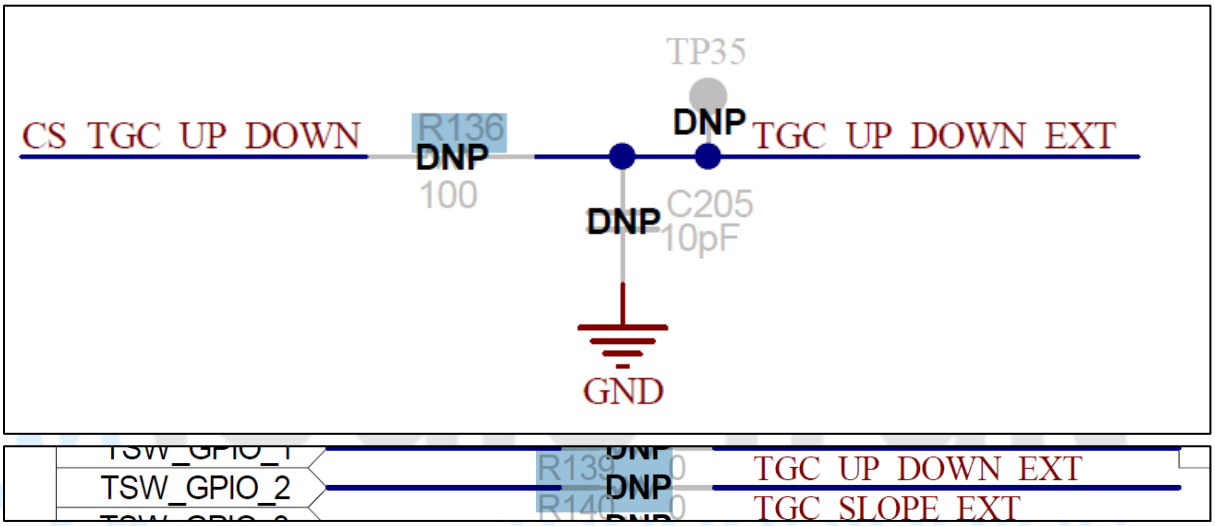


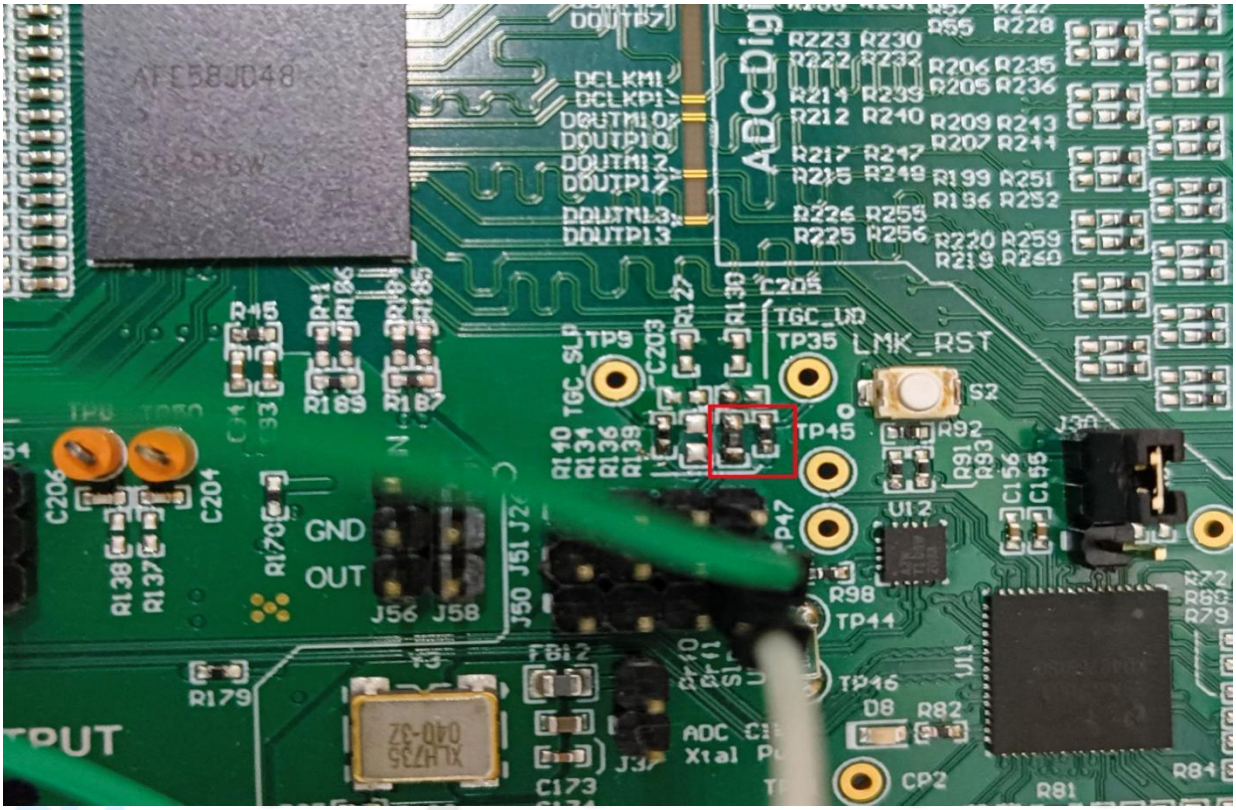
The below image is the 100ohm termination done on ADC Evaluation Board



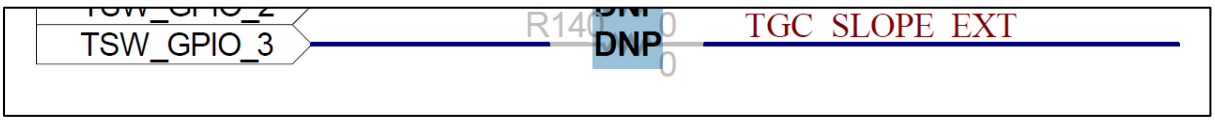
6. The following changes are made to prove deterministic latency

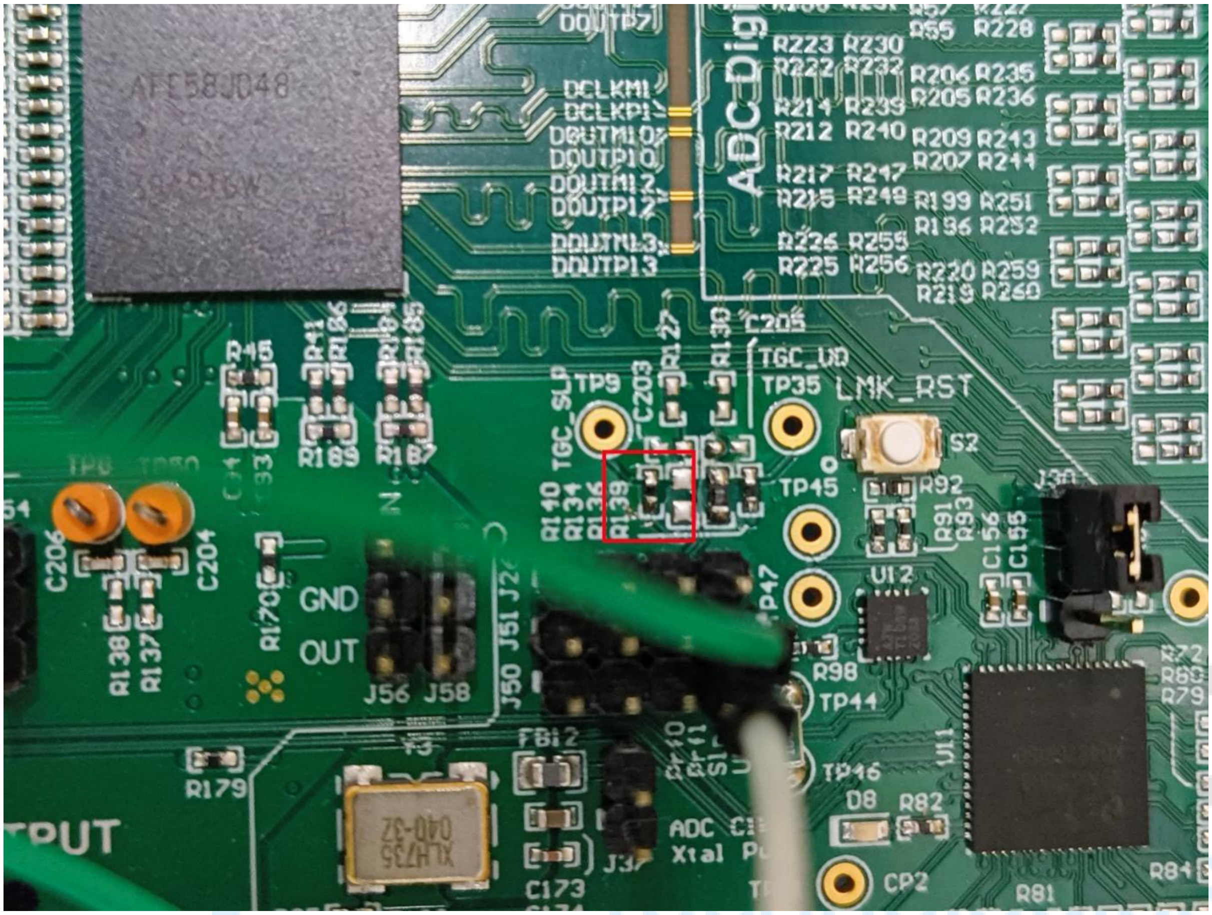
   - To prove deterministic latency, a square wave needs to be sent from FPGA to the scope and ADC input, for which there is a need for a GPIO header
   - Since ELITESTEK EVM has no GPIO connected to the header, the ADC eval board spare header will be used.
   - The **TSW_GPIO_2** will be used for this purpose, but there are two DNP resistors between the path, which need to mound.
   - The resistor references are R139 and R136, and zero-ohm resistors are mounted on them.



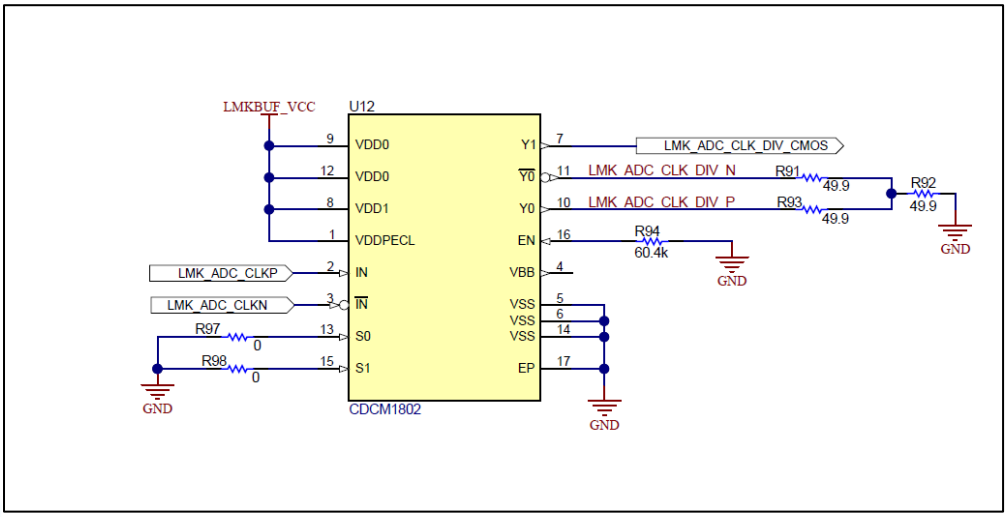


- Another GPIO is needed to prove deterministic latency, here an ADC_MSB signal from FPGA must be checked in the scope. For this purpose, one test point or header is required
- Connect the **TSW_GPIO_3** for this purpose, but there is one DNP resistor in between the path, which needs to be mounted. The resistor references are R140, so mount zero-ohm resistors on this.




DCLKM1
DCLKP1
DOUTM10
DOUTP10
DOUTM12
DOUTP12
DOUTM13
DOUTP13
TGC_VD
TP35
LMK_RST
S2
TP9
TP45
GND
OUT
J56
J58
U12
TP44
TP16
D8
R82
CP2
FB12
C173
R179
ADC
Xtal

- Changed the divider value of buffer in the path of LMK to ADC sampling clock



- S0 and S1 pins on CDCM1802 are for divider value setting for the device, currently it is set on four that means the buffer will generate a output clock which is /4 of the input clock.
- **We need to change this divider to one.**
- As per TI this divider in the path can lead to length mismatching and since there is a factor of four between input and output so this can lead to phase variation between SYSREF and Device clock output from this divider. So, it's better to keep this divider to one to remove this ambiguity.

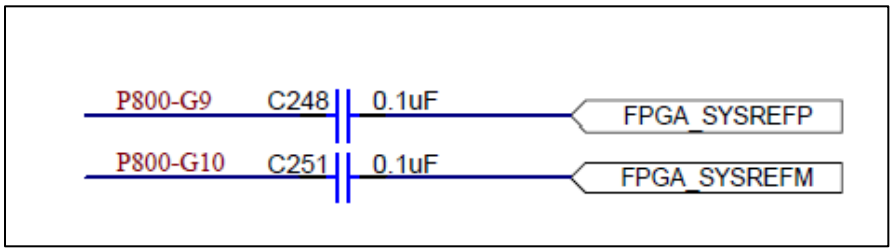
- As per the datasheet to make this divider one we need to change the R97 resistor value from 0ohm to 60k ohm.

Table 1. Selection Mode Table

MODE	EN	S1	S0	LVPECL(1)	LVCMOS
				Y0	Y1
0	0	X	X	Off (high-z)	Off (high-z)
1	$V_{DD}/2$	0	$V_{DD}/2$	/1	/1
2	$V_{DD}/2$	$V_{DD}/2$	1	/1	/2
3	1	0	0	/1	/4
4	$V_{DD}/2$	0	1	/2	/2
5	1	0	1	/2	/4
6	$V_{DD}/2$	0	0	/4	/4
7	$V_{DD}/2$	1	0	/4	/8
8	$V_{DD}/2$	$V_{DD}/2$	$V_{DD}/2$	/8	/1
9	1	1	0	/8	/4
10	1	1	1	Off (high-z)	/4

(1) The LVPECL outputs are open emitter stages. Thus, if you leave the unused LVPECL output Y0 unconnected, then the current consumption is minimized and noise impact to remaining outputs is neglectable. Also, each output can be individually disabled by connecting the corresponding VDD input to GND.

- Removal of AC caps on the sysref path to FPGA.
  - Remove the 0.1uf capacitor on the path and replace it with 0 ohm resistor to improve the slew rate on the sysref path.
  - Change C248 and C251 on the path to 0ohm resistor.



- Increase of DVDD_1V15 swing to improve the amplitude on the FPGA RX side.
  - Change the feedback resistor R1 value to 5.9k or 5.7k whatever available.