Design Document for Porting JESD204B Transmitter and Receiver IP on Elitestek TJ-Series FPGA

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1.3	16th May 2025	• Addition of 12.5Gbps testing results for ADC and DAC	Arpitha

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1 Introduction

1.1 Purpose

The purpose of this document is to specify the FPGA Architecture for

- JESD204B Transmitter and Receiver IP.
- Interfacing JESD204b Link Layer IP with Elitestek PMA.

1.2 Scope

The scope of this document is to explain the High-Level Design Description Details for JESD204B IP and interface details between JESD204b Link Layer IP and Elitestek PMA IP. All the top-level modules of JESD204B IP are explained in this Document.

1.3 Acronyms and Abbreviations

Abbreviations	Definition
ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
PHY	Physical Layer
TX	Transmitter
RX	Receiver
PMA	Physical Medium Attachment
PCS	Physical Coding Sublayer
IP	Intellectual Property
ILA	Initial Lane Alignment
CGS	Code Group Synchronization
LMFC	Local Multi frame Clock

IN	Input
OUT	Output
FIFO	First In First Out

Table 1: Abbreviations

1.4 Applicable Documents

1. JESD204B Specification: Serial Interface for Data Converters
2. Proposal Document for JESD204B porting on Elitestek TJ-Series FPGA

2 JESD204B Protocol Overview

2.1 Protocol Architecture

JESD204B is the standard serial interface between the data converters and the logic devices. It describes the multi-gigabit serial data link between the Analog to Digital Converter (ADCs) and Digital to Analog Converter (DACs) to the FPGAs or ASIC. JESD204B standard supports a maximum lane rate of up to 12.5 Gbps with Multiple Lane feature support. It supports Multi-Lane and Multi-Device synchronization. It is necessary for high-density systems as it provides reduced PCB area and package size.

JESD204B protocol uses 8b/10b encoding and decoding in the Physical layer for DC balancing.

Figure 1 illustrates data flow through different layers in the JESD204B protocol.

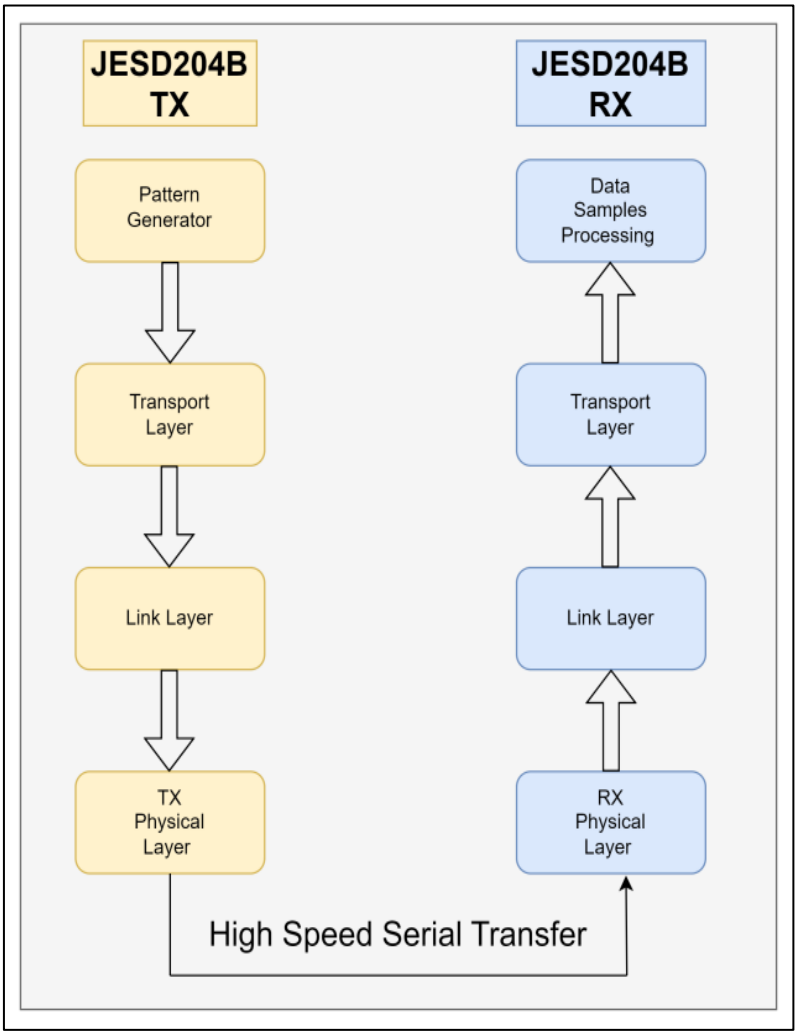


Figure 1. JESD204B Data Layer Flow

2.2 Features of LFT JESD204b Link Layer IP

Following are the LFT JESD204B Transmitter and Receiver features:

- Design as per JESD204B Standard.
- Supports up to 8 lanes per core (This limitation is due to the Transceivers).
- Supports Transport and Link Layers.
- Supports Subclass 0 and 1.
- Does not support Subclass 2.
- No of Frames per Multi-frame (K) = 1 to 32
- No of Samples per Frame (F) = 1 to 256
- Supports Scrambling.
- Supports Initial Lane Alignment.
- Supports Character Replacement.
- AXI Stream Data interface.
- AXI Lite Configuration interface.
- Supports Error Detection and Link Retraining.
- Supports Multi Device Synchronization: Proved Synchronization up to 32 Channels

2.3 Applications

Figure 2 and Figure 3 illustrate the application of the JESD204B protocol. It provides an overview of the interface between the ADC and DAC with the FPGA logic devices through JESD204B protocol over the SERDES lanes.

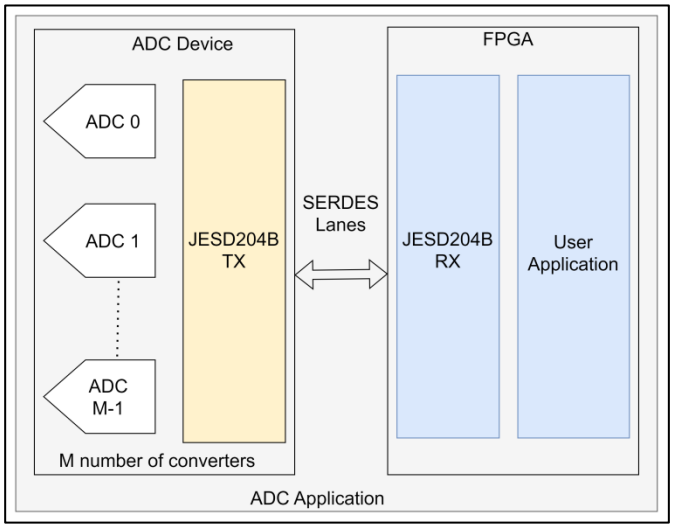


Figure 2. ADC Application Block Diagram

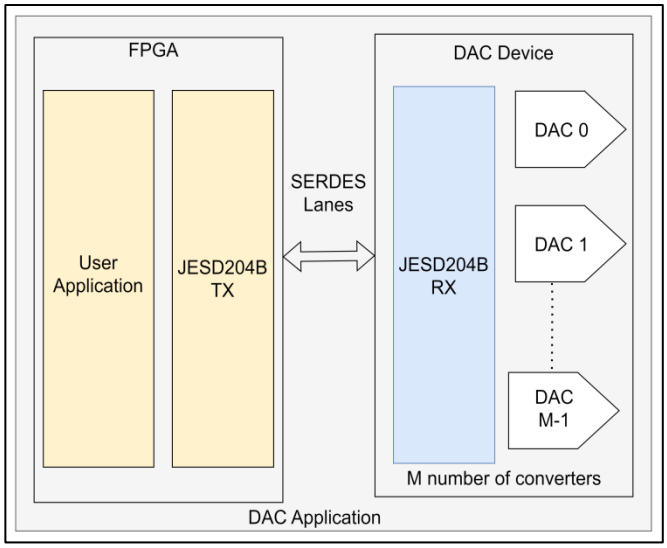


Figure 3. DAC Application Block Diagram

3 JESD204B Transmitter Core

3.1 Transmitter IP Block Diagram

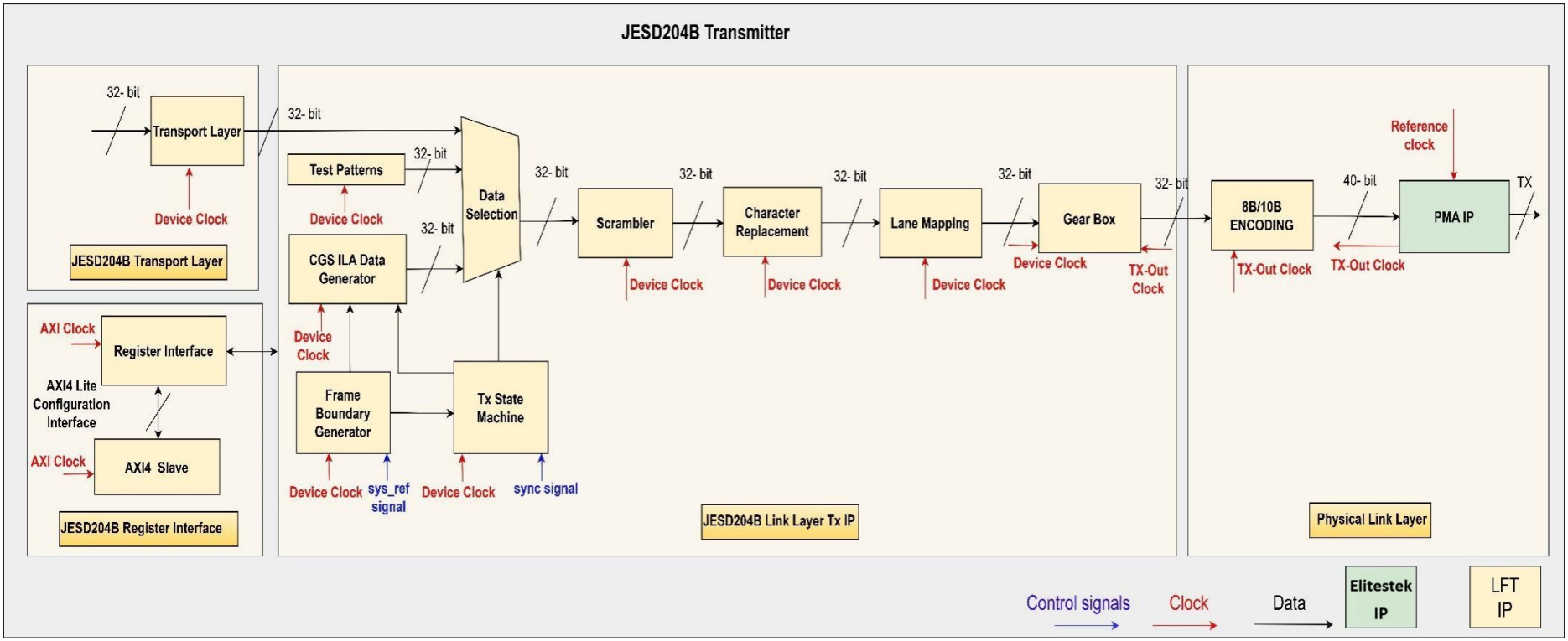


Figure 4. JESD204B Transmitter Block Diagram

3.2 Transmitter IP I/O Signals Description

Signal Name	Direction	Width	Description
Clocks and Resets			
refclk_p	IN	1	Positive differential reference clock
refclk_n	IN	1	Negative differential reference clock
sys_reset_i	IN	1	On board system reset
Transceiver signals			
txp_out	IN	1	Transceiver positive transmitter signal
txn_out	IN	1	Transceiver negative transmitter signal
JESD204B control signals			
tx_sysref_i	IN	1	Sysref control signal to the Tx IP, used when Subclass 1 is selected
tx_sync_i	OUT	1	Sync signal to the TX IP
AXI Stream Input signals			
tx_aresetn_o	OUT	1	Active low reset signal to the transport layer module
tx_tdata_i	IN	32*L	Input data from the transport layer
tx_tready_o	OUT	1	Ready signal to the transport layer
AXI-Lite Control Signals			
tx_s_axi_aclk_i	IN	1	AXI Lite register interface clock
tx_s_axi_aresetn_i	IN	1	AXI Lite register reset signal
tx_s_axi_awaddr_i	IN	32	Write address. Specifies the address of the first transfer in the write burst transaction. Associated

			control signals determine the addresses of remaining transfers in a burst
tx_s_axi_awprot_i	IN	3	Write protection type. This signal indicates the privilege and security level of the transaction, and whether the transaction is data access or instruction access. [0] – Privileged or Unprivileged [1] – Secure or Non-secure [2] – Instruction or data access This feature is not supported and must be driven to 3'h0.
tx_s_axi_awvalid_i	IN	1	Write address valid. This signal indicates that the channel is signaling valid write address and control information. Address and control information remains stable until awready signal is high. 0: Address and control information not valid. 1: Address and control information valid.
tx_s_axi_awready_o	OUT	1	Write address ready. It indicates that the slave is ready to accept the address and associated control signals. 0: Slave not ready 1: Slave ready
tx_s_axi_wdata_i	IN	32	Write Data.
tx_s_axi_wstrb_i	IN	4	Write strobes. This signal indicates which byte lanes hold valid data. There is one write strobe bit for every eight bits of the write data bus.
tx_s_axi_wvalid_i	IN	1	Write valid. This signal indicates that valid write data and strobes are available. 0: Write data and strobes not available. 1: Write data and strobes available.
tx_s_axi_wready_o	OUT	1	Write ready. It indicates that the slave can accept write data. 0: Slave not ready 1: Slave ready
tx_s_axi_bresp_o	OUT	2	Write response. Indicates status of write transaction This signal indicates an error if the data phase ID does not match the address phase ID. For example, if AWID = 0 and WID! = 0, the controller responds with bresp error.

tx_s_axi_bvalid_o	OUT	1	Write response valid. Indicates that valid written response is available. 0: Write response not valid. 1: Write response valid.
tx_s_axi_bready_i	IN	1	Response ready. This signal indicates that the master can accept a written response. 0: Master not ready 1: Master ready
tx_s_axi_araddr_i	IN	32	Read address. Gives the initial address of the read burst transaction, and control signals issued alongside the address show how the address is calculated for the remaining transfers in the burst.
tx_s_axi_arprot_i	IN	3	Read protection type. This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or instruction access. [0] – Privileged or Unprivileged [1] – Secure or Non-secure [2] – Instruction or data access This feature is not supported and must be driven to 3'h0.
tx_s_axi_arvalid_i	IN	1	Read address valid. This signal indicates that the channel is signaling valid read address and control information. Address and control information remains stable until arready signal is high. 0: Address and control information not valid. 1: Address and control information valid.
tx_s_axi_arready_o	OUT	1	Read address ready. It indicates that slave is ready to accept read address and associated control signals. 0: Slave not ready 1: Slave ready
tx_s_axi_rdata_o	OUT	32	Read Data.
tx_s_axi_rresp_o	OUT	2	Read response. It indicates the status of the read transaction. Currently, the controller always responds with rx_s_axi_rresp_o = 0.
tx_s_axi_rvalid_o	OUT	1	Read valid. Indicates that required read data is available and read transfer can complete. 0: Read data not available. 1: Read data available.

tx_s_axi_rready_i	IN	1	Read ready. This signal indicates that the master can accept a read data and response. 0: Master not ready 1: Master ready

Table 2. JESD204B Transmitter IP I/O signal Description

3.3 Transmitter IP Attribute Description

Attribute	Description
NUMBER_OF_LANES(L)	Indication of the total number of transceiver lanes used
JESD204B_IP_REV_NO	JESD204B Revision number
Tx Parameters	
OCTETS_PER_FRAME	Number of Octets in a frame
FRAMES_PER_MULTIFRAME	Number of frames in a Multi frame
OCTETS_PER_MULTIFRAME	Number of octets in a Multi frame
SUB_CLASS	Type of Subclass
MULTI_FRAMES_IN_ILA	Number of Multi Frames in an ILA
SCRAMBLING	Scrambler enable and disable selection
SYSREF_ALWAYS	Periodic or one-shot reference signal
ILA Settings Parameters	
ILA_DID	Device Identification number
ILA_ADJCNT	Number of adjustment resolution steps to adjust DAC LMFC.
ILA_BID	Bank ID – extension to DID
ILA_ADJDIR	Direction to adjust DAC LMFC
ILA_PHADJ	Phase Adjustment request to DAC

ILA_SCR	Scrambling Enabled
ILA_L1	Number of lanes per converter device
ILA_M1	Number of converters per device
ILA_CS	Number of control bits per sample
ILA_N	Converter Resolution
ILA_Nt	Total number of bits per sample
ILA_SUBCLASSV	Device Subclass Version 000 – Subclass 0 001 – Subclass 1 010 – Subclass 2
ILA_JESDV	JESD204 version 000 – JESD204A 001 – JESD204B
ILA_S	Number of samples per converter per frame cycle
ILA_HD	High Density format
ILA_CF	Number of control words per frame clock period per link
ILA_RES1	Reserved field 1
ILA_RES2	Reserved field 2
ILA_LID	Lane Identification number
Test Data Generator Parameters	
RPAT_EN	Enabling Modified Random Pattern
JSPAT_EN	Enabling Scrambled Jitter Pattern
PRBS_EN	Enabling PRBS generator

Table 3. JESD204B Transmitter IP Attribute description

3.4 Transmitter IP Functional Block Description

3.4.1 Transport Layer

- The transport layer maps the sample data to required data format accepted by the DAC chip.
- It will convert the sample data to octets and frames by adding additional control and tail bits if necessary and transmit data on different lanes.
- When the link layer is ready to accept data, it asserts the ready signal, and the formatted data is sent from the transport layer to the link layer.
- The channel mode and the number of lanes activated are sent from the register interface.
- The IQ mapper module will send the data only on the activated number of lanes

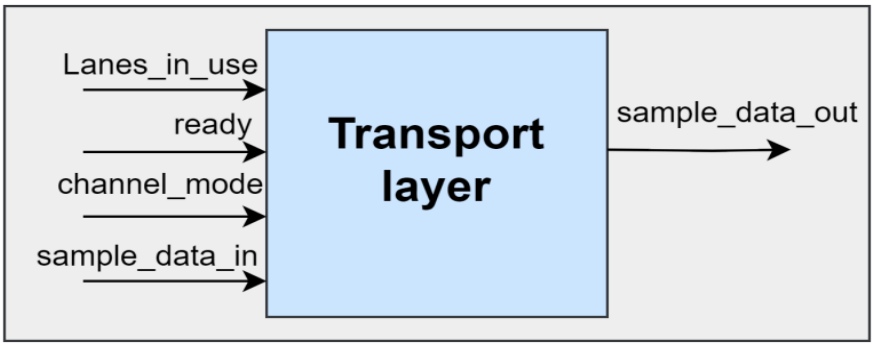


Figure 5. Transport layer Block design I/O signals

Signal Name	Direction	Width	Description
lanes_in_use	In	4	Number of transceiver Lanes in use.
ready	In	1	Ready signal to send data from IQ mapper.
channel_mode	In	1	0 - Quad Channel Mode (Real Data) 1 - Dual Channel Mode (IQ Data)

sample_data_in	In	128	Input data
sample_data_out	Out	255	Output data

Table 4. Transport layer I/O signals description

3.4.2 Link Layer

The Link Layer of JESD204B Tx IP includes the following modules:

- TX state machine
- CGS_ILA Data Generator module
- Frame Boundary Generator
- Scrambler
- Character Replacement
- Lane Mapping

3.4.2.1 TX State machine

- The TX state machine module defines the different states of JESD204B protocol as CGS, ILA and data phase.
- The TX device detects the low SYNC signal for at least four consecutive local frame clock periods and interprets the SYNC pulse as a synchronization request.
- Initially the State Machine is in IDLE State, when the Sync signal is high and Sysref is captured, then state machine proceeds to CGS State. K28.5 characters are sent continuously in IDLE and CGS states.
- When SOMF is 1, then State Machine proceeds to ILA State. In ILA State, ILA information is sent on the parallel data and state Machine proceeds to Data State.
- The transition of the states is shown in the FSM diagram below

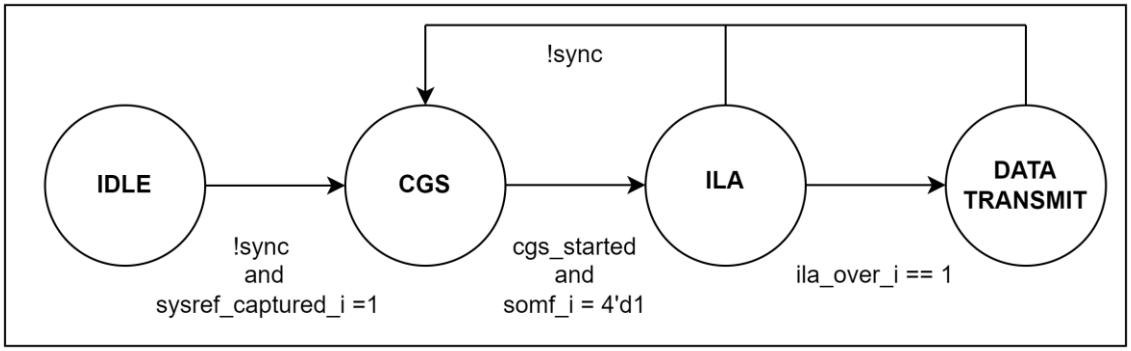


Figure 6.TX Data phase state machine

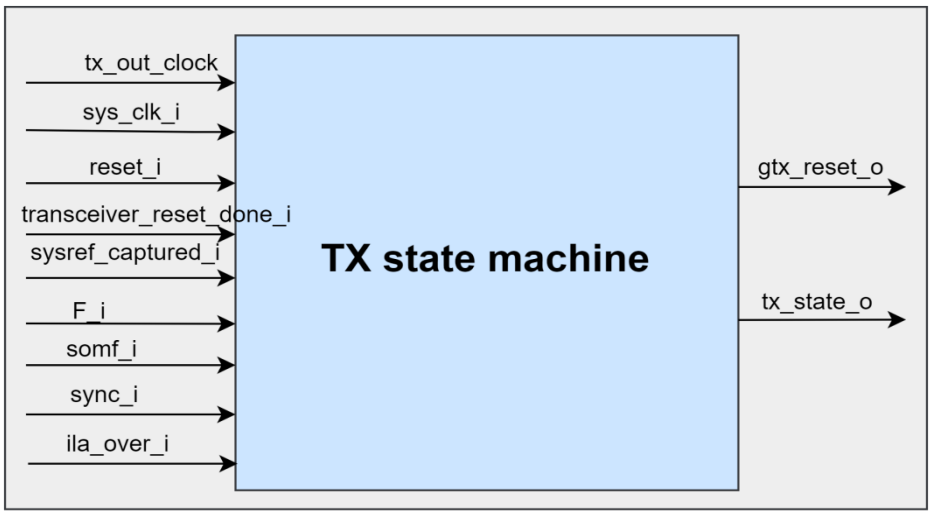


Figure 7.TX State machine Block design I/O signals

Signal Name	Direction	Bus Width	Description
Tx_out_clk	In	1	Output clock from the PHY block
sys_clk_i	In	1	System Clock
Reset_i	In	1	Active high reset
transceiver_reset_done_i	In	1	Tx_reset done from the PHY block
Sync_i	In	1	Sync signal from the receiver
Sysref_captured_i	In	1	Input signal which provides the reference phase for the clock signals

Tx_state_o [1:0]	OUT	2	00 - IDLE 01 - START_CGS 10 - ILA 11 -DATA_TRANSMIT
ila_over_i	n	1	Indicates the end of ILA Phase

Table 5.TX State machine I/O signals description

3.4.2.2 CGS_ILA Data Generator module

The CGS_ILA Data Generator module generates the CGS, ILA Data for the transmission based on the sync signal received from the receiver.

3.4.2.2.1 Code Group Synchronization (CGS)

In the CGS phase, the receiver aligns with the 10-bit symbol boundary of the transmitted symbols.

CGS is achieved by the following process:

- The receiver generates the synchronization request by asserting the ~SYNC signal low.
- The transmitter on issue of the synchronization request, transmits the stream of /K/=/K28.5/ (BC) symbols
- The receiver synchronizes when it receives at least 4 consecutive /K28.5/ Symbols without any error. It then deactivates the ~SYNC signal by asserting it high and moves to the next non-K28.5 symbol, which is the ILA phase, in case of any error the synchronization fails and the link stays in CGS phase.
- The Subclass type of the transmitter device determines the start of next phase, as follows:
  - Subclass 0: The transmitter on receiving the deactivated ~SYNC signal from the receiver, continue transmitting the /K/ symbols until the start of next frame and from next frame it transmits the ILA sequence.

- Subclass 1: The transmitter on receiving the deactivated ~SYNC signal from the receiver continues transmitting the /K/ symbols until the next LMFC boundary. The transmitter transmits the ILA sequence on the chosen LMFC boundary.

The following two figures represent flow of the synchronization process:

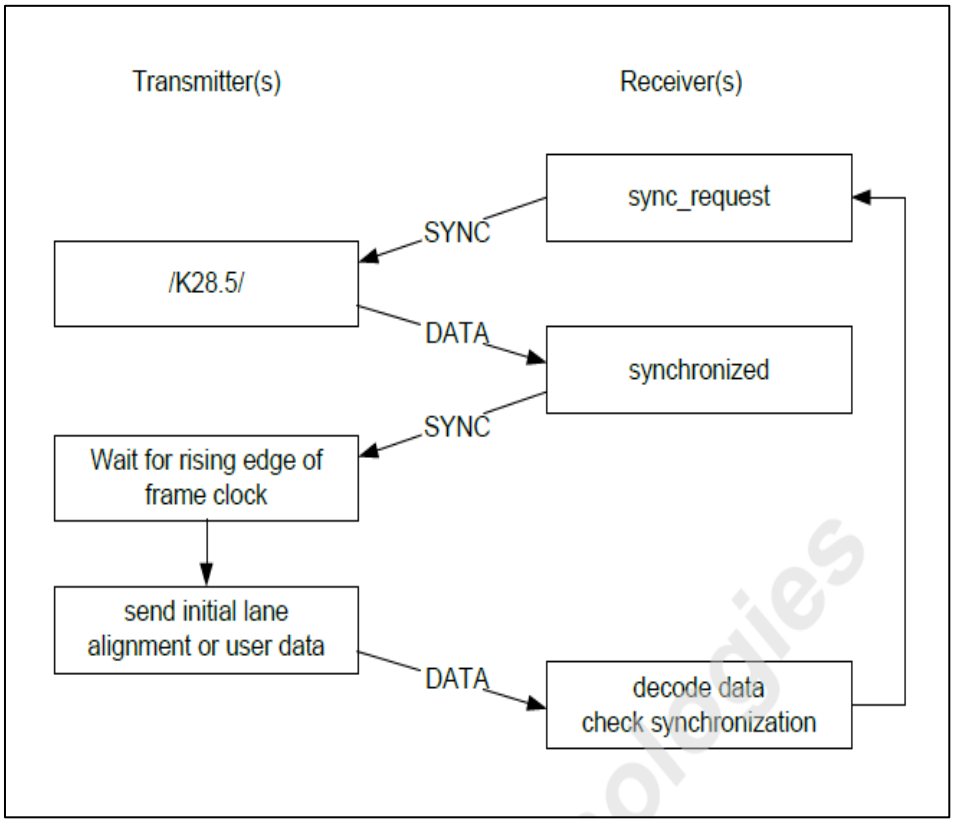


Figure 8. Synchronization process for Subclass 0

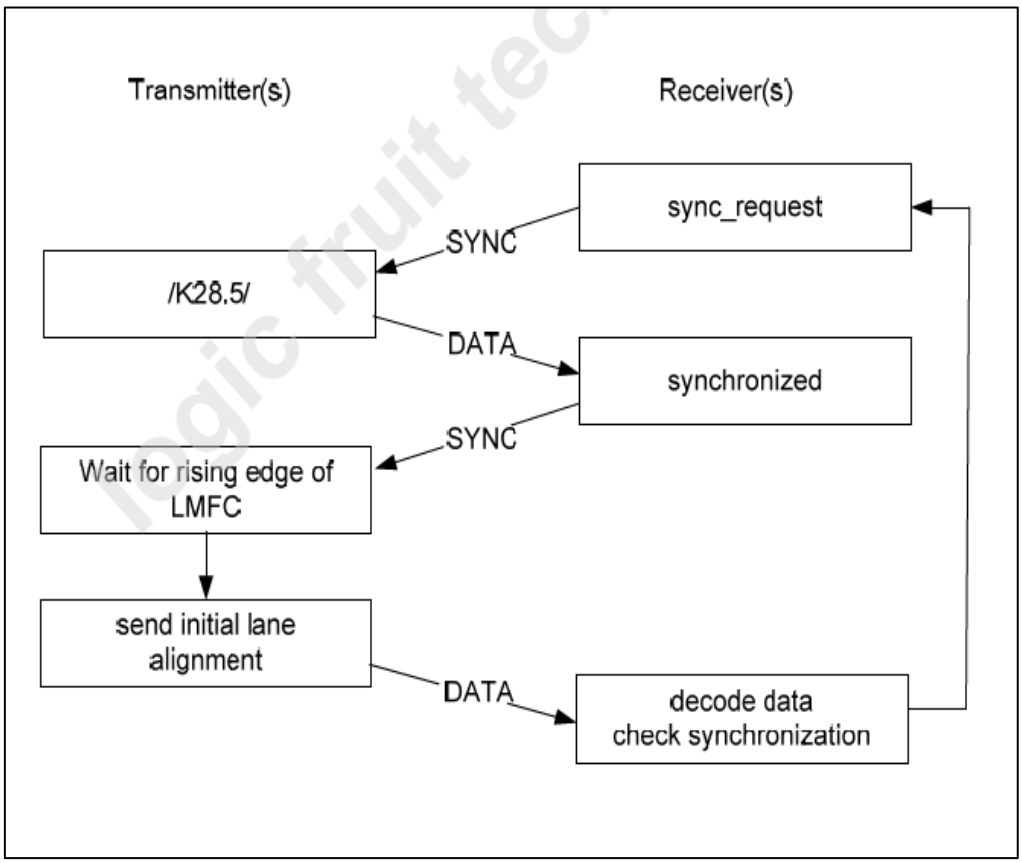


Figure 9.Synchronization process for Subclass 1

3.4.2.2.2 Initial Lane Alignment (ILA)

The Lane synchronization is done using Initial Lane Alignment (ILA) sequence

- The ILA phase begins after SYNC signal is asserted high.
- In the ILA phase there are a minimum of 4 multi-frames and up-to 256 multi-frames containing the alignment symbols and other character symbols.
- A multi-frame is defined as a group of K successive frames
- ILA symbols are always transmitted without scrambling, even if the scrambling is enabled.
- After the CGS phase the first non-/K28.5/ symbol marks the start of frame, if the transmitter emits an ILA sequence the first non-/K28.5/ symbol is /K28.0/ know as /R/ character.
- The first four multi frames consist of the following:

- Multi frame 1: The MF 1 starts with an /R/ character [K28.0] which represents the start of sub-sequence and ends with an /A/ character [K28.3] which represents the lane alignment character.
- Multi frame 2: The MF 2 starts with an /R/ character followed by /Q/ character [K28.4] which represents the start of the link configuration data, followed by link configuration data parameters over 14 configuration octets and ends with an /A/ character.
- Multi frame 3: same as multi frame 1.
- Multi frame 4: same as multi frame 1.

The below figure represents in detail transmission of the ILA sequence frames.

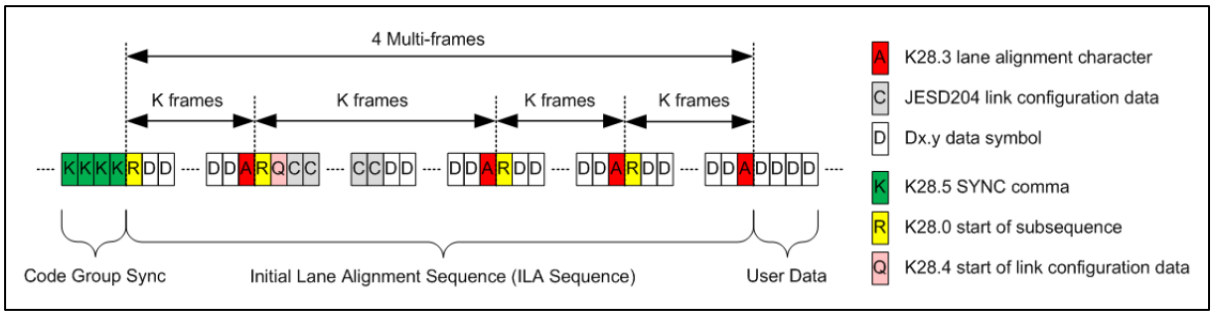


Figure 10.Initial Lane Alignment Sequence

Signal Name	Direction	Bus Width	Description
tx_out_clk	IN	1	Output clock from the PHY block
reset_i	IN	1	Active high reset
sync_n	IN	1	Sync pulse from the receiver (Active LOW)
tx_state_i	IN	2	Represents the state value for different phases
multi_frames_in_ila_i	IN	8	Total Number of Multi Frames in ILA
lanes_in_use_i	IN	8	Number of lanes being used
transceiver_reset_done	IN	1	Tx_reset done from the PHY block
ila_over	OUT	1	Indicates the end of ILA Phase

cgs_ila_data_out	OUT	L*32	CGS_ILA Data out from each lane
cgs_ila_charisk_out	OUT	L*4	CGS_ILA Char out from each lane
somf_i	IN	4	Start Of Multi frame Indicator
eomf_i	IN	4	End Of Multi frame Indicator
Configuration Octets parameters			
F_i	IN	8	Number of Octets per Frame
K_i	IN	5	Number of Frames per Multi frame
DID_i	IN	8	Device/Link identification Number
ADJCNT_i	IN	4	Used only in Subclass2
BID_i	IN	4	Bank ID, this is the extension of the DID
ADJDIR_i	IN	1	Used only in Subclass2
PHADJ_i	IN	1	Used only in Subclass2
SCR_i	IN	1	Indicates whether scrambling is enabled or disabled
L1_i	IN	6	Number of lanes per converter device
LID_i	IN	5	Number of lanes per converter device
M1_i	IN	9	Number of converters per device
CS_i	IN	2	Number of control bits per sample
N_i	IN	6	Converter Resolution
Nt_i	IN	6	Total Number of bits pert sample
SUBCLASSV_i	IN	3	Subclass version of device ● 000 - Subclass ● 001 - Subclass1 ● 010 - Subclass2
JESDV_i	IN	3	Version of JESD ● 000 - JESD204A ● 001 - JESD204B
S_i	IN	6	Number of samples per converter per frame cyle

HD_i	IN	1	High Density Format
CF_i	IN	5	Number of control words per frame clock period per link
RES1_i	OUT	8	Reserved Field 1
RES2_i	OUT	8	Reserved Field 2

Table 6. CGS ILA module I/O signals description

3.4.2.3 Frame Boundary Generator

- The frame boundary indicator module generates the frame boundaries named as sof, eof, sofm and eofm and detects the sysref signal for subclass 1
- It is responsible for Multichip synchronization using subclass 1
- Detection of Sysref signal
  - For Subclass 1 the sysref signal is distributed to all the devices in the system, this can be a periodic signal or a pulse signal
  - Sysref signal is synchronized with respect to the PHY TX clock and rising edge detection is done to know whether it is periodic or a pulse signal
  - On the rising edge of every sysref the number of octets per multiframe should be four or zero so that the sysref is aligned to the LMFC clock, in case there is any mismatch then the sysref alaram is raised high.
- Generation of frame boundary signals:
  - The frame boundary signals are dependent on the number of octets in a frame (F) and number of multiframes (K).
  - The Sysref, Octets per Frame, Frames per Multiframe are programmed through Register Interface.
  - This module is responsible to generate all the timing signals required for the IP

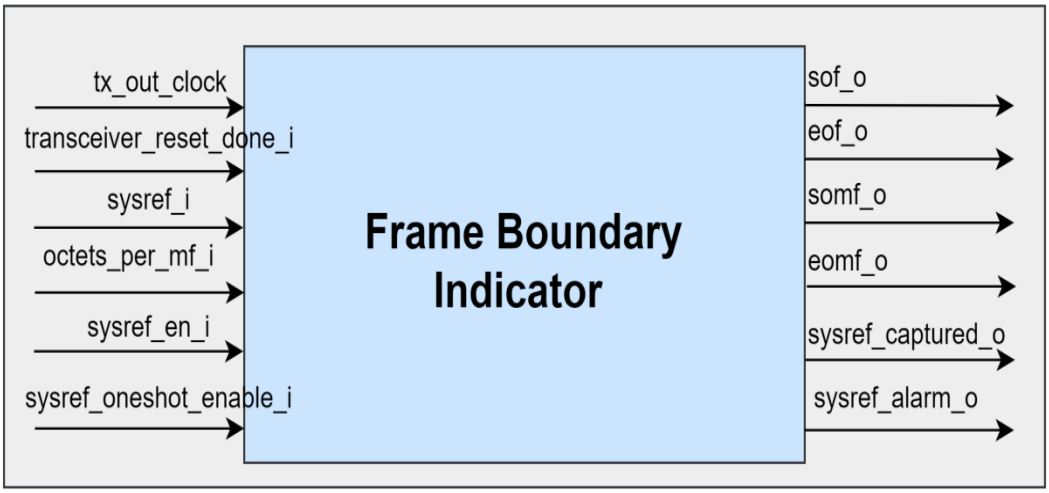


Figure 11. Frame Boundary Block

Signal	Direction	Bus Width	Description
tx_out_clk	IN	1	Output clock from the PHY block
reset_i	IN	1	Active high reset
F_i	IN	8	Number of Octets per Frame
K_i	IN	5	Number of Frames per Multi frame
octets_per_mf_i	IN	13	Number of Octets per Multi frame
transceiver_reset_done	IN	1	Tx_reset done from the PHY block
eof_o	OUT	4	End Of Frame Indicator
sof_o	OUT	4	Start Of Frame Indicator
somf_o	OUT	4	Start Of Multi Frame Indicator
eomf_o	OUT	4	End Of Multi Frame Indicator
sysref_i	IN	1	Syref from JESD interface
sysref_en_i	IN	1	1 = Subclass 1 0 = Subclass0
sysref_oneshot_enable_i	IN	1	1 = Sysref one shot mode enabled 0 = Sysref periodic mode enabled
sysref_alarm_o	OUT	1	Indicates any mismatch between Sysref and Local Multiframe clock

			(LMFC)
sysref_captured_o	OUT	1	Sysref Status Signal

Table 7. Frame Boundary Indicator I/O signals description

3.4.2.4 Scrambler

- The scrambler module, based on the scramble enable signal, transmits the scrambled data or else the original data
- The scramble enable signal is disabled for the CGS and ILA phase.
- The polynomial used for scrambling the data is $1 + x^{14} + x^{15}$

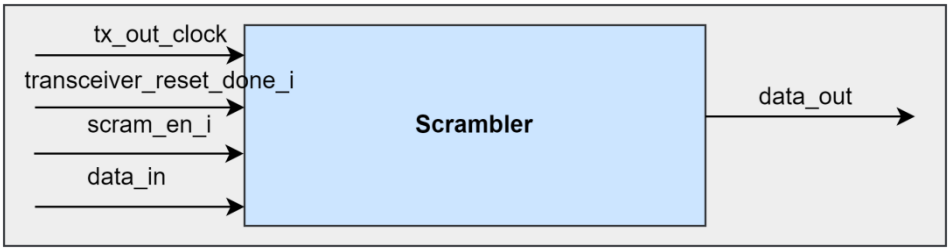


Figure 12. Scrambler module I/O signals

Signal Name	Direction	Bus Width	Description
tx_out_clk	IN	1	Output clock from the PHY block
reset_i	IN	1	Active high reset
scram_en_i	IN	1	Enable signal for scrambler
data_in	IN	32	Input for the scrambler
data_out	OUT	32	Scrambled data out on lane

Table 8. Scrambler module I/O signal descriptions

3.4.2.5 Character Replacement

The character replacement module monitors the alignment characters in the transmitted data stream and do corresponding character replacement based on frame and multi frame boundaries in data transmission phase and can be by-passed in CGS and ILA phases.

- In the data phase, frame alignment is monitored with control characters.
- Character replacement is used at the end of frames since there is no additional overhead to accommodate data or frame alignment during the data phase.
- Character replacement allows an alignment character to be issued at a frame boundary “if and only if” the last character of the current frame may be replaced with the last character of the last frame, facilitating confirmation that the alignment has not changed since the ILAS sequence.
- Character replacement depends on whether scrambling has been enabled or disabled.
- When scrambling is disabled, the character replacement occurs as follows:
  - If the last octet of the current frame, which is not coinciding with the end of a multi-frame, is equal to the last octet of the previous frame, then the transmitter shall replace the current last octet and encode it as the control character /F/ = /K28.7/.
  - If the last octet of the current frame, which coincides with the end of the multi-frame, equals the last octet in the previous frame, then the transmitter shall replace the current last octet and encode it as the control character /A/ = /K28.3/.
  - On receiving the /F/ or /A/ symbol, the receiver replaces it with the value of the octet used at the same position in the previous frame.
- When scrambling is enabled, the character replacement occurs as follows:
  - If the last scrambled octet of the current frame, which is not coinciding with the end of a multi-frame, is equal to 0xFC, the transmitter shall encode it as a control character /F/.
  - If the last scrambled octet in a multi-frame equals 0x7C, the transmitter shall encode it as a control character /A/.

- Upon receiving an /F/ or /A/ symbol, the receiver shall input the corresponding data octet 0xFC or 0x7C to the descrambler.

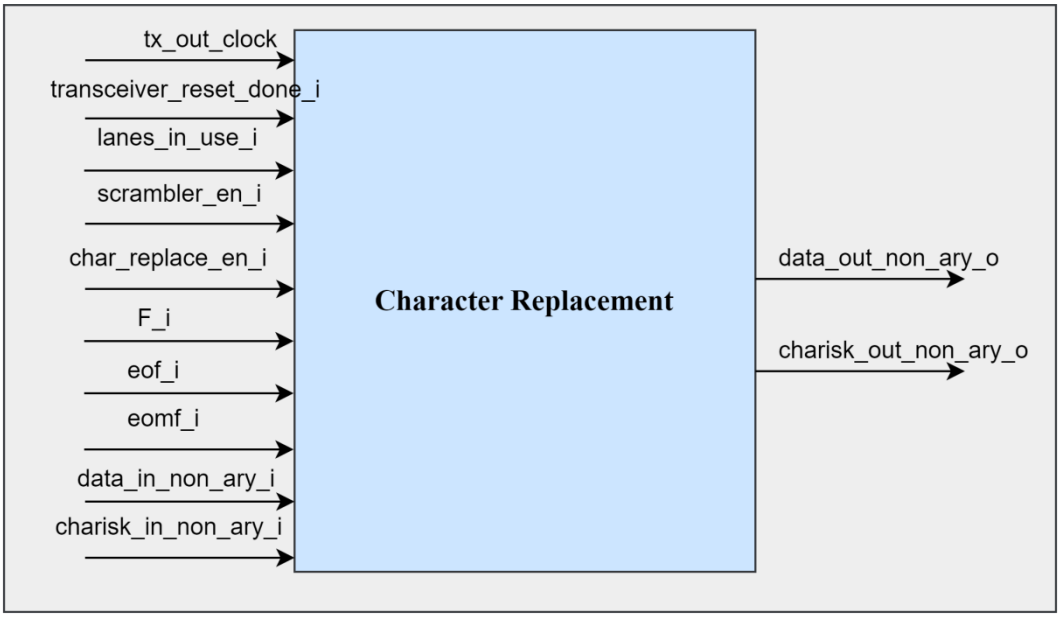


Figure 13. Character Replacement I/O signals

Signal	Direction	Bus Width	Description
tx_out_clk	IN	1	Output clock from the PHY block
reset_i	IN	1	Active high reset
lanes_in_use	IN	4	Number of Transceiver lanes in use
scrambler_en	IN	1	Enable signal for Scrambling
data_txd	IN	L*32	Enable signal for character replacement
charisk_in	IN	L*4	Data out after character replacement
F	IN	8	Number of Octets per Frame
K	IN	5	Number of Frames per multi-frame
char_replace_en	IN	1	Enable signal for character replacement
eof	IN	4	End Of Frame Indicator

eomf	IN	4	End Of Multi frame Indicator
char_replace_data_out	OUT	N*32	Data out after character replacement
char_replace_char_out	OUT	N*4	Indicator out for k character on the lane

Table 9. Character Replacement I/O signal descriptions

3.4.2.6 Lane Mapping

- The Lane mapping module maps the data in each lane.
- It receives the input from character replacement block and transmits the output to the 8b/10b encoder module

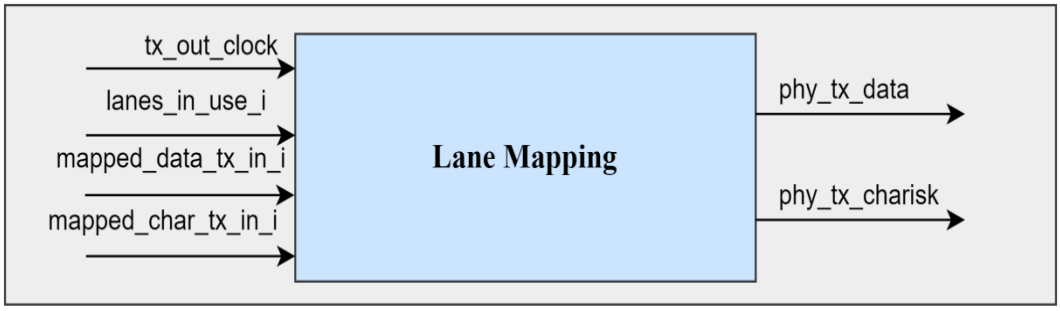


Figure 14. Lane Mapping I/O signals

Table 10. Lane Mapping I/O signal description

Signal	Direction	Bus Width	Description
tx_out_clk	IN	1	Output clock from the PHY block
lanes_in_use_i	IN	8	Number of lanes connected to the receiver
mapped_data_tx [31:0]	IN	L*32	data in from the character replacement
mapped_char_tx [3:0]	IN	L*4	char in from the character replacement
phy_tx_data [31:0]	OUT	L*32	Data transmitted on lane after mapping
phy_tx_charisk [3:0]	OUT	L*4	Indicator for K character in transmitted data after mapping on lane

3.4.2.7 TX Gear Box

- This module is used to handle the CDC between the data received from the Transceiver and the data processed inside the JESD204B TX IP.
- The FIFO module is used to take care of the clock domain crossing, where the write clock is the device clock from the LMK and read clock is the transceiver clock for each lane.

3.4.3 Physical Layer

- JESD204b Physical layer includes Elitestek PMA and PCS Blocks.
- The PMA IP supports 20-bit data width. Maximum serial data rates support up to 5Gbps.
- Elitestek PMA example design contains 8b10b Encoding and PMA initialization blocks. The same example design will be used for the JESD204b Physical layer.
- Following block diagram gives an overview of the example design of Elitestek TX PMA IP

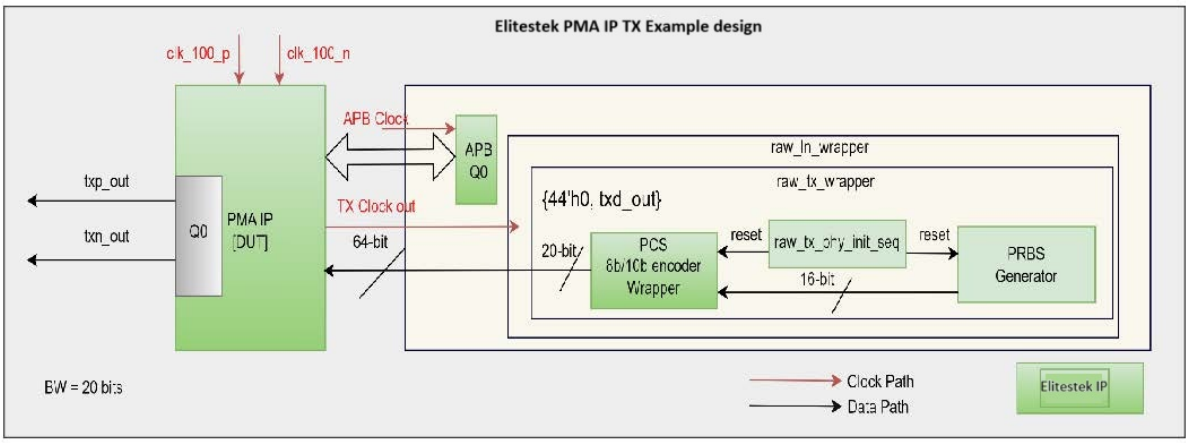


Figure 15. Elitestek PMA IP TX example design

3.4.3.1 Physical coding sublayer (PCS)

- The PCS module includes the 8b/10b encoder block.
- The 8b/10b encoding module encodes the 8-bit octets into 10-bit symbols depending on the running disparity value (RD+/-)
- The encoding enables many bit transitions which are needed for the clock data recovery at the receiver end.

3.4.3.2 Elitestek TX PMA IP

- The Elitestek TX PMA block consists of timing FIFO, timing flipflop, and byte serializer.
- It supports only the FIFO mode
- The TX PHY initialization depends on the transceiver power state of request and acknowledgment
- The following FSM state diagrams describe the different states of Elitestek TX PHY initialization

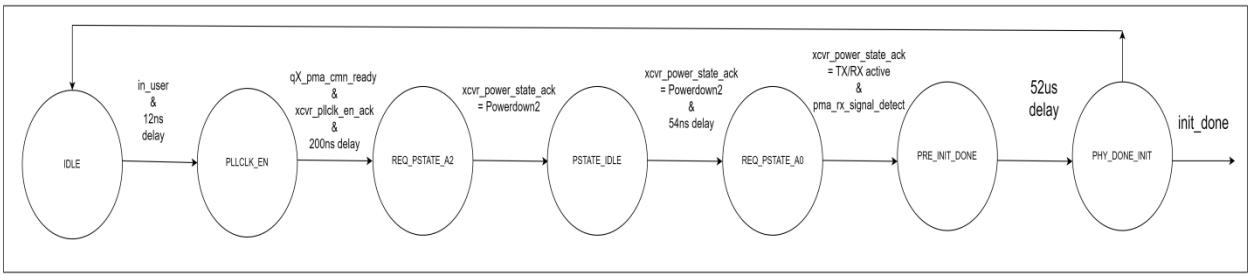


Figure 16.FSM state diagram of Elitestek TX PMA IP initialization

Signal	Direction	Bus Width	Description
Reference clock	IN	`1	On board reference clock to the PHY block
sys_reset_i	IN	1	System reset
tx_out_clk	OUT	1	Output clock from the PHY block
reset_done_o	OUT	L*32	Reset done signal from the PHY block
txp	OUT	L	Serial Differential signal out
txn	OUT	L	Serial Differential signal out
txdata_in	IN	L*32	Data transmitted to the PHY block
txcharisk_in	IN	L*4	Indicator for K character in transmitted data

Table 11. PHY Block I/O Signals

3.4.4 Transmitter Register Interface

The JESD204B TX core is configured using an AXI4-Lite Register Interface. The register map is shown in below table.

Offset	Bits	Mode	Default	Description
0x2	31:13	**R**	19'h0	**Reserved**
	12:0	**RW**	13'h20	**octets_per_mf_o** Number of octets per multi frame.
0x3	31:24	**RW**	8'h1c	**control_chars_R_o** ILA_CONTROL_CHARS_R
	23:16	**RW**	8'h7c	**control_chars_A_o** ILA_CONTROL_CHARS_A
	15:8	**RW**	8'9c	**control_chars_Q_o** ILA_CONTROL_CHARS_Q
	7:0	**RW**	8'hbc	**control_chars_K_o** ILA_CONTROL_CHARS_K
0x4	31:24	**RW**	8'hfc	**control_chars_F_o** ILA_CONTROL_CHARS_F
	23:16	**RW**	8'h55	**DID_o** ILA_DID
	15:12	**RW**	4'h0	**ADJCNT_o** ILA_ADJCNT
	11:8	**RW**	4'h0	**BID_o** ILA_BID
	7	**RW**	1'b0	**ADJDIR_o** ILA_ADJDIR
	6	**RW**	1'b0	**PHADJ_o** ILA_PHADJ
	5	**RW**	1'b0	**SCR_o** ILA_SCR
	4:0	**RW**	4'h8	**L1_o** ILA_L1
0x5	31:24	**RW**	8'h1	**M1_o** ILA_M1
	23:22	**RW**	2'b10	**CS_o** ILA_CS
	21:17	**RW**	5'b01101	**N_o** ILA_N
	16:12	**RW**	5'b01111	**Nt_o** ILA_Nt

	11:9	**RW**	3'b001	**SUBCLASSV_o** ILA_SUBCLASSV
	8:6	**RW**	3'b001	**JESDV_o** ILA_JESDV
	5:1	**RW**	5'h0	**S_o** ILA_S
	0	**RW**	1'b0	**HD_o** ILA_HD
0x6	31:30	**RW**	2'b01	**CF_o** ILA_CF
	29:22	**RW**	8'h5a	**RES1_o** ILA_RES1
	21:14	**RW**	8'ha5	**RES2_o** ILA_RES2
	13:0	**R**	14'h0	**Reserved**
0x8	31:1	**R**	31'h0	**Reserved**
	0	**RW**	1'b0	**reg_ip_reset_o** Reset the JESD204b IP.
0xD	31:1	**R**	31'h0	**Reserved**
	0	**RW**	1'b1	**sub_class_o** 0: backward compatible with JESD204a. 1: uses external reference signal SYSREF.
0xF	31:24	**RW**	8'h3	**multi_frames_in_ila_o** Error counter for disparity errors received in transceiver lines.
	16	**RW**	1'b0	**scrambling_o** 0: Scrambler is disabled. 1: Scrambler is enabled.
	13	**RW**	1'b0	**prbs_en_o** 0: Incremental data. 1: PRBS data.
	12:8	**RW**	5'h1f	**frames_per_multiframe_o** Number of frames per multi frame.
	7:0	**RW**	8'h1	**octets_per_frame_o** Number of octets per frame.
0x10	31:8	**R**	24'h0	**Reserved**

	7:0	**RW**	8'hff	**lanes_in_use_o** Number of transceiver lanes in use.
0x14	31:1	**R**	31'h0	**Reserved**
	0	**RW**	1'b0	**sysref_always_o** 0 - LMFC counter aligns for every SYSREF event. 1 - LMFC counter aligns only on the first SYSREF event after transceiver_reset_done and ignores all the subsequent SYSREF events.
0x18	31:1	**R**	31'h0	**Reserved**
	0	**R**	0	**sysref_alarm_i** Indicates the misalignment between LMFC and SYSREF.

Table 12. Transmitter Register Address Map

3.5 JESD204B Transmitter Hardware Testing Overview

3.5.1 Hardware Testing Block Diagram

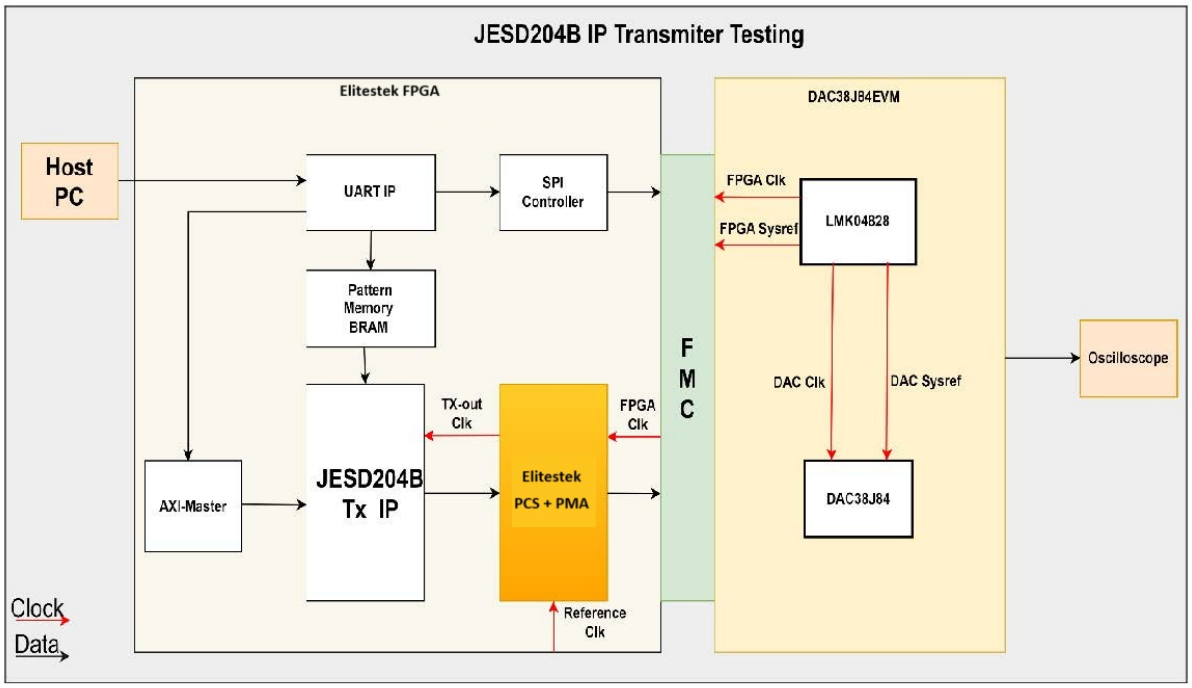


Figure 17. JESD204B IP Transmitter Testing Block diagram

3.5.2 I/O signal Description

Signal Name	Direction	Bus Width	Description
clk_100_p	IN	1	Positive differential reference clock
clk_100_n	IN	1	Negative differential reference clock
clk_25	IN	1	On-board system clock
sys_reset	IN	1	On-Board reset
uart_tx	OUT	1	UART TX signal
uart_rx	IN	1	UART RX signal
txp	OUT	L	Transceiver positive transmitter signal
txn	OUT	L	Transceiver negative transmitter signal
tx_sysref	IN	1	LMK sysref clock to FPGA p/n
tx_sync	IN	1	Sync signal from the DAC
dac_sck	OUT	1	SPI clock
dac_sdo	OUT	1	SPI data output
dac_sdi	IN	1	SPI data input
dac_cs	OUT	1	SPI chip select for DAC
lmk_cs	OUT	1	SPI chip select for LMK

Table 13. JESD204B RX application I/O signal description

3.5.3 Block Description

3.5.3.1 SPI controller

- The SPI controller module is used for programming the registers in the DAC evaluation board, which includes the DAC and clock generator (LMK) registers,
- The chip selects signal lmk_cs and dac_cs are used to select between the DAC or clock generator block registers.
- For the JESD link up, the DAC and clock generator must be programmed.

3.5.3.2 Pattern Memory

- The data samples which are sent to the DAC are fed to the pattern memory block using UART.
- These samples are continuous sinusoidal waves of fixed sample generated using Matlab/Octave software.
- These samples are stored in a Block RAM in the pattern memory module.
- On JESD link up, the samples in the Block RAM are played continuously on the DAC.

3.5.3.3 UART IP

- The UART module is used for the user control interface
- The dynamic programming of the JESD204B IP Registers is done through the UART interface
- The configuration of the DAC registers sent through SPI is done through the UART interface
- The samples are fed to the pattern memory block through UART interface

3.5.3.4 AXI Master

- The AXI-Lite master module will be used for the configuration of the register interface required for programming the register set of JESD204B RX IP
- This register set configuration is must for the link up of JESD204B IP.

3.6 TX Resource Utilization

- The following resource utilization is done for the JESD204B TX Link layer, Transport layer, Physical layer, and Application layer

Modules	Resources					
	LUTs	**FFs**	**SRLs**	**ADDs**	**RAMs**	**DSP/MULTs**
JESD204B TX link layer	3956	5793	17	229	0	0
Transport layer	123	128	0	0	0	0
Physical Layer	1191	1208	0	164	32	0
Application layer	2598	2084	75	366	32	0
TX_top_module	7868	9213	92	759	64	0
Available	362880	362880	67200	362880	2688	1344
Utilization %	2.168209877	2.53885582	0.136904762	0.209160053	2.380952381	0

Table 14. TX Resource Utilization

4 JESD204B Receiver Core

4.1 Receiver IP Block Diagram

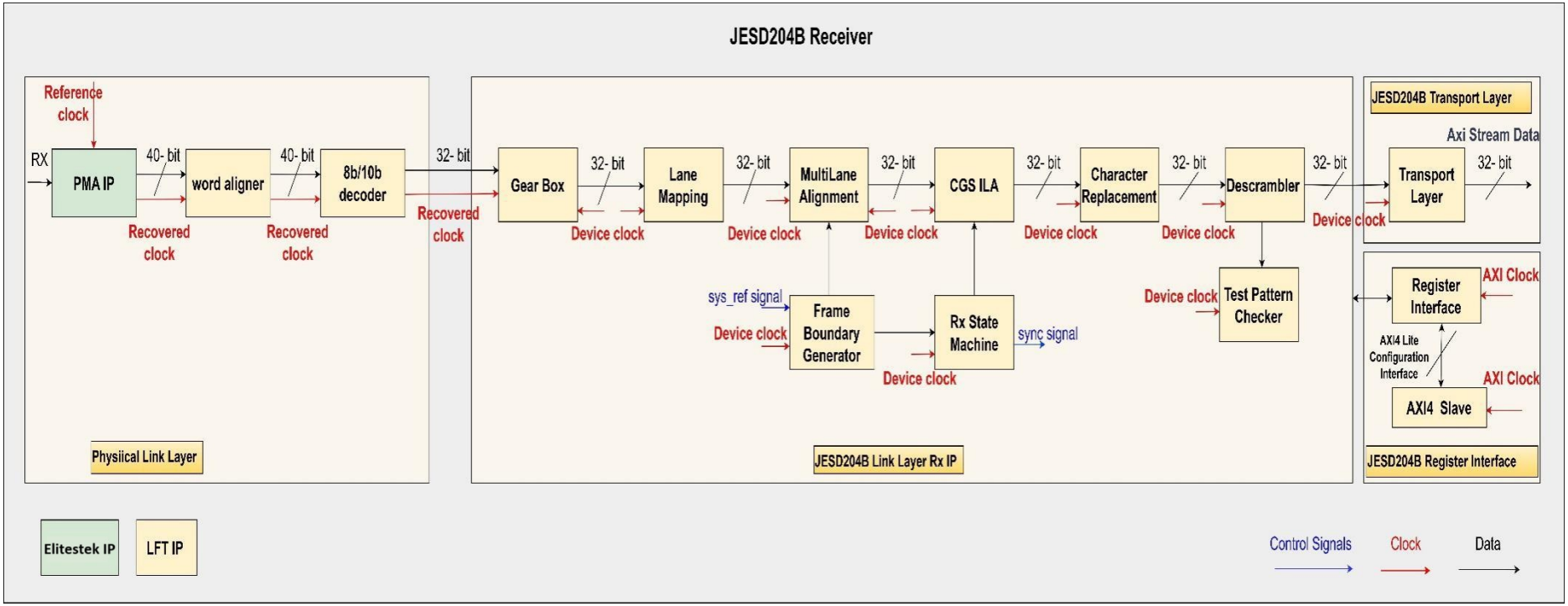


Figure 18. JESD204B Receiver Block Diagram

4.2 Receiver IP I/O signal Description

Signal Name	Direction	Width	Description
Clocks and Resets			
refclk_p	IN	1	Positive differential reference clock
refclk_n	IN	1	Negative differential reference clock
sys_reset_i	IN	1	On board system reset
Transceiver signals			
rxp_in	IN	1	Transceiver positive receiver signal
rxn_in	IN	1	Transceiver negative receiver signal
JESD204B control signal			
rx_sysref_i	IN	1	LMK Sysref control signal to the RX IP
rx_sync_o	OUT	1	Sync signal from the RX IP
Transport layer input signals			
rx_aresetn_o	OUT	1	Active low reset signal to the snapshot module
rx_tdata_o	OUT	32*L	Output data from the RX transport layer
rx_tvalid_o	OUT	1	Valid signal from the transport layer
rx_sof_o	OUT	1	Start of frame signal from the frame boundary generator module
rx_somf_o	OUT	1	Start of multi frame signal from the frame boundary generator module
rx_eof_o	OUT	1	End of frame signal from the frame boundary generator module

rx_eomf_o	OUT	1	End of multi frame signal from the frame boundary generator module
AXI-Lite Interface Signals			
rx_s_axi_aclk_i	IN	1	AXI Lite register interface clock
rx_s_axi_aresetn_i	IN	1	AXI Lite register reset signal
rx_s_axi_awaddr_i	IN	32	Write address. Specifies the address of the first transfer in the write burst transaction. Associated control signals determine the addresses of remaining transfers in a burst
rx_s_axi_awprot_i	IN	3	Write protection type. This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or instruction access. [0] – Privileged or Unprivileged [1] – Secure or Non-secure [2] – Instruction or data access This feature is not supported and must be driven to 3'h0.
rx_s_axi_awvalid_i	IN	1	Write address valid. This signal indicates that the channel is signaling valid write address and control information. Address and control information remains stable until awready signal is high. 0: Address and control information not valid. 1: Address and control information valid.
rx_s_axi_awready_o	OUT	1	Write address ready. Indicates that the slave is ready to accept the address and associated control signals. 0: Slave not ready 1: Slave ready
rx_s_axi_wdata_i	IN	32	Write Data.
rx_s_axi_wstrb_i	IN	4	Write strobes. This signal indicates which byte lanes hold valid data. There is one write strobe bit for every eight bits of the write data bus.

rx_s_axi_wvalid_i	IN	1	Write valid. This signal indicates that valid write data and strobes are available. 0: Write data and strobes not available. 1: Write data and strobes available.
rx_s_axi_wready_o	OUT	1	Write ready. Indicates that the slave can accept write data. 0: Slave not ready 1: Slave ready
rx_s_axi_bresp_o	OUT	2	Write response. Indicates status of write transaction This signal indicates an error if the data phase ID does not match the address phase ID. For example, if AWID = 0 and WID! = 0, the controller responds with bresp error.
rx_s_axi_bvalid_o	OUT	1	Write response valid. Indicates that valid write response is available. 0: Write response not valid. 1: Write response valid.
rx_s_axi_bready_i	IN	1	Response ready. This signal indicates that the master can accept a write response. 0: Master not ready 1: Master ready
rx_s_axi_araddr_i	IN	32	Read address. Gives the initial address of the read burst transaction, and control signals issued alongside the address show how the address is calculated for the remaining transfers in the burst.
rx_s_axi_arprot_i	IN	3	Read protection type. This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or instruction access. [0] – Privileged or Unprivileged [1] – Secure or Non-secure [2] – Instruction or data access This feature is not supported and must be driven to 3'h0.
rx_s_axi_arvalid_i	IN	1	Read address valid. This signal indicates that the channel is signaling valid read address and control information. Address and control information remains stable until aready signal is high. 0: Address and control information not valid. 1: Address and control information valid.

rx_s_axi_aready_o	OUT	1	Read address ready. Indicates that slave is ready to accept read address and associated control signals. 0: Slave not ready 1: Slave ready
rx_s_axi_rdata_o	OUT	32	Read Data.
rx_s_axi_rresp_o	OUT	2	Read response. Indicates the status of the read transaction. Currently, the controller always responds with rx_s_axi_rresp_o = 0.
rx_s_axi_rvalid_o	OUT	1	Read valid. Indicates that required read data is available and read transfer can complete. 0: Read data not available. 1: Read data available.
rx_s_axi_rready_i	IN	1	Read ready. This signal indicates that the master can accept a read data and response. 0: Master not ready 1: Master ready

Table 15. JESD204B Receiver IP I/O signal Description

4.3 Receiver IP Attribute Description

Table 16. JESD204B Receiver IP Attribute description

Attribute	Description
NUMBER_OF_LANES(L)	Indication of the total number of transceiver lanes used
JESD204B_IP_REV_NO	JESD204B Revision number
Register Interface Parameters	
OCTETS_PER_FRAME	Number of Octets in a frame
FRAMES_PER_MULTIFRAME	Number of frames in a multi-frame
OCTETS_PER_MULTIFRAME	Number of octets in a multi frame
SUB_CLASS	Type of Subclass

MULTI_FRAMES_IN_ILA	Number of multi frames in an ILA
SCRAMBLING	Scrambler enable and disable selection.
SYSREF_ALWAYS	Periodic or one-shot reference signal

4.4 Receiver IP Functional Block Description

4.4.1 Transport Layer

- This block will map the decoded sample data to the required data format and recover octets from data based on whatever mechanism is used before sending data from the transmitter.
- This is not a part of the JESD204B standard because different ADCs will follow a different methods for sample mapping, so it varies from device to device.
- Depending on the ADC modes, the received data is mapped and sampled at the output

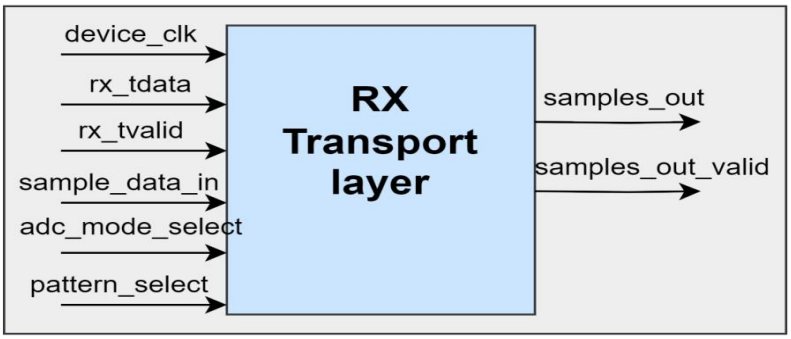


Figure 19. RX Transport layer I/O signals

Signal	Direction	Bus Width	Description
device_clk	IN	1	Receiver Clock
rx_tdata	IN	128	Received Data
rx_tvalid	IN	1	Received data valid
samples_out	OUT	128	Mapped output data

sample_out_valid	OUT	1	Mapped Output valid
adc_mode_select	OUT	3	ADC mode selection bits

Table 17. RX Transport layer I/O signal description

4.4.2 Link Layer

The Link Layer of JESD204B Receiver IP includes the following modules:

- Lane Mapping
- Multi lane alignment
- CGS ILA
- Frame boundary indicator
- Character Replacement
- RX state machine
- Descrambler

4.4.2.1 Lane Mapping

- The lane mapping maps the data received from the transceiver
- The data assignment is done as per the number of lanes

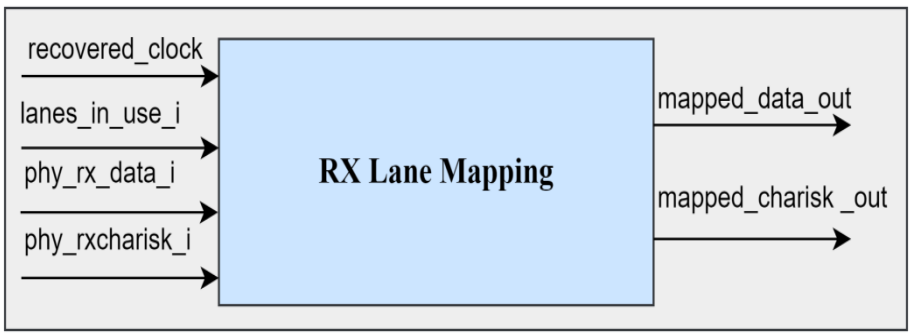


Figure 20. RX Lane Mapping I/O signals

Signal	Direction	Bus Width	Description
recovered_clock	IN	1	Recovered clock from the PHY block
lanes_in_use_i	IN	8	Number of lanes connected to the receiver
phy_rx_data_i	IN	L*32	Received data from the transceiver
hy_rxcharisk_i	IN	L*4	Indicator for K character in received data
mapped_data_out	OUT	L*32	Mapped data out
mapped_char_out	OUT	L*4	Mapped char out

Table 18. RX Lane Mapping I/O signal descriptions

4.4.2.2 Multi-lane alignment module

- The multilane alignment module receives the mapped input data and transmits the data on all the lanes in an aligned manner.
- On the completion of the CGS phase, this module stores the data on all the lanes and releases the data on the detection of the next LMFC rising edge.
- The ILA first sample data will be flushed out of this block from all the lanes at the same time.
- This module implements the LMFC Buffer Required for synchronization.

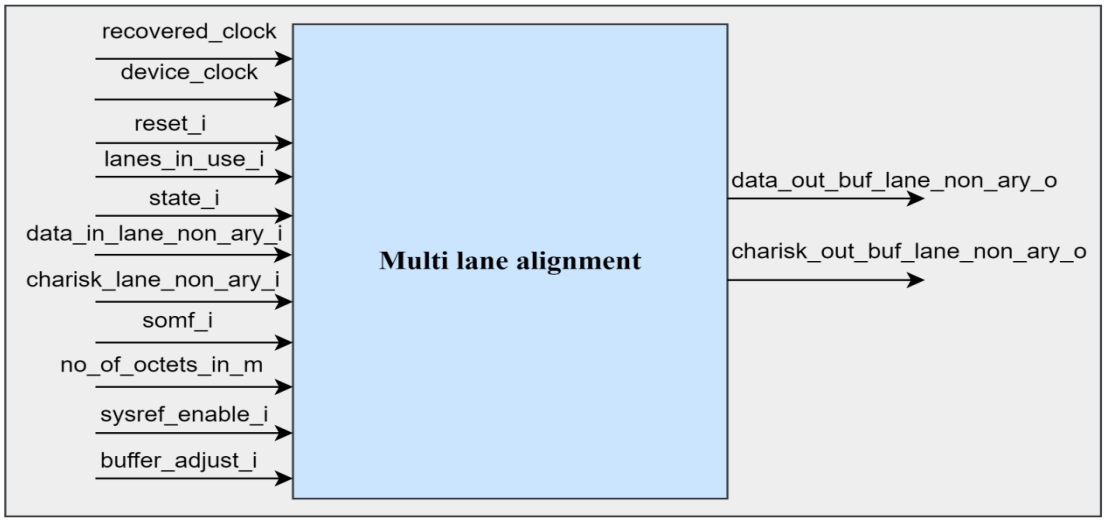


Figure 21.Multi lane alignment I/O signals

Signal	Direction	Bus Width	Description
recovered_clk	IN	1	Recovered clock from the PHY block
device_clk	IN	1	Device clock derived from the recovered clock
data_in_lane_non_ary_i	IN	L*32	Unaligned input data
charisk_lane_non_ary_i	IN	L*4	K Character indication for unaligned data
data_out_buf_lane_non_ary_o	OUT	L*32	Aligned Output data
charisk_out_buf_lane_non_ary_o	OUT	L*4	K Character indication for aligned data
state_i	IN	2	State information from the state machine
lanes_in_use_i	IN	8	Number of lanes used
somf_i	IN	4	Start of multiframe
no_of_octets_in_mf_i	IN	11	Number of octets in a multiframe
sysref_enable_i	IN	1	It indicates the sub-class information
buffer_adjust_i	IN	13	Buffer adjust information

Table 19. Multi-lane alignment I/O signal description

4.4.2.3 CGS ILA data detection module

- The CGS and ILA characters are detected in this module
- It generates the flag cgs_over and ila_over
- The cgs_over flag is generated after detection of four octets of /K28.5/ character

- The ila_over flag is generated after the detection of four ILA multi-frames

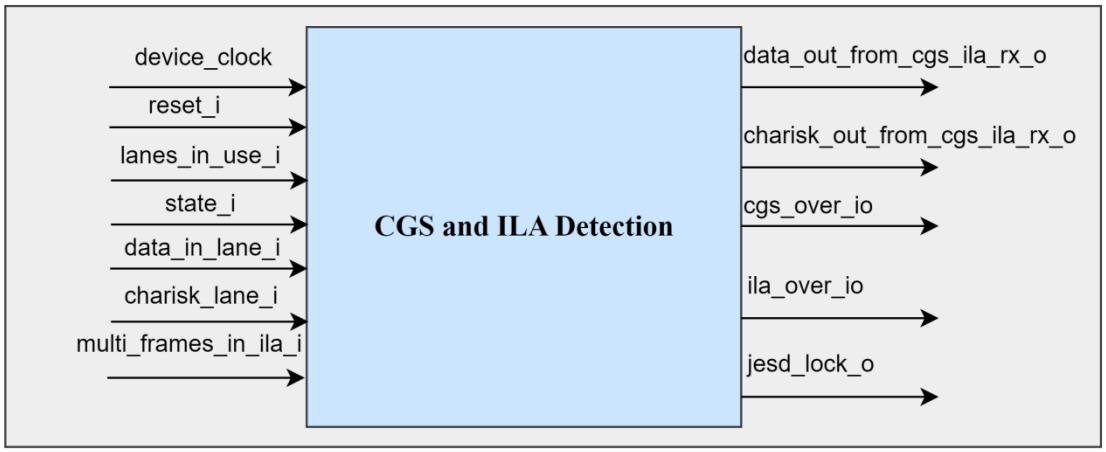


Figure 22. CGS and ILA Detection I/O Signals

Signal	Direction	Bus Width	Description
device_clock	IN	1	Device clock derived from the recovered clock
reset_i	IN	1	Active high reset signal
lanes_in_use_i	IN	8	Number of lanes used
state_i	IN	2	RX states for different data phase
data_in_lane_i	IN	L*32	Input data to the CGS_ILA module
charisk_lane_i	IN	L*4	Input K Character indication
multi_frames_in_ila_i	IN	8	Number of multi-frames
data_out_from_cgs_ila_rx_o	OUT	L*32	Output data from the CGS_ILA module
charisk_out_from_cgs_ila_rx_o	OUT	L*4	Output K Character indication
cgs_over_io	OUT	1	Status flag for indication of CGS data phase is done

ila_over_io	OUT	1	Status flag for indication of ILA data phase is done
jesd_lock_o	OUT	1	Status flag for indication of data phase to start

Table 20. CGS and ILA Detection I/O Signal description

4.4.2.4 RX State Machine

- The RX state machine defines the state of the JESD204B RX IP according to the received status flag inputs.
- The states defined are IDLE state, Start CGS state, ILA state, and Data state
- The reset to the transceiver IP is generated from the RX state machine module
- The RX comma alignment enable signal is asserted in the CGS state
- At the ILA state, the sync signal from RX is asserted as high

The transition of the states is shown in the FSM diagram below:

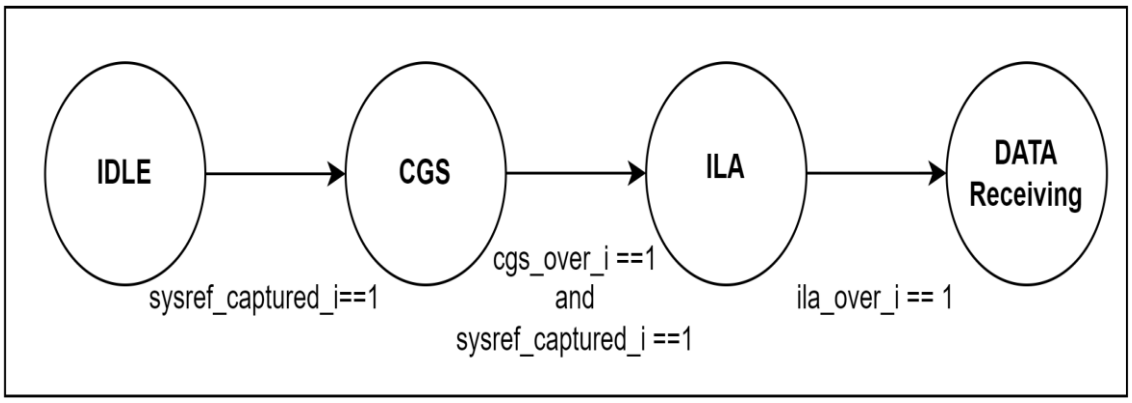


Figure 23. RX State Machine

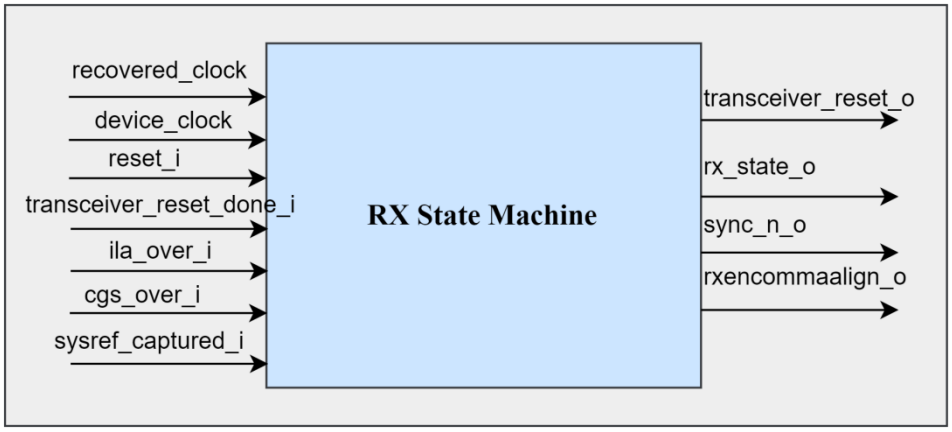


Figure 24. RX State Machine I/O signals

Signal	Direction	Bus Width	Description
recovered_clock	IN	1	Recovered clock from the PHY block
device_clock	IN	1	Device clock derived from the recovered clock
reset_i	IN	1	Active high reset signal
transceiver_reset_done_i	IN	1	Reset done signal from the PHY block
ila_over_i	IN	1	Status flag for indication of ILA data phase is completed
cgs_over_i	IN	1	Status flag for indication of CGS data phase is completed
sysref_captured_i	IN	1	Indication for detection of sysref event in subclass 1
transceiver_reset_o	OUT	1	Reset input to the transceiver
rx_state_o	OUT	2	RX state: ● 00 - IDLE ● 01 - CGS

			• 10 - ILA • 11 - Data acquisition
sync_n_o	OUT	1	Sync signal out from Rx
rxencommaalign_o	OUT	1	RX comma alignment enables signal

Table 21.RX state machine I/O signals description

4.4.2.5 Frame Boundary Indicator

Refer to the Frame Boundary Indicator module in the Transmitter section.

4.4.2.6 Character Replacement

- The character Replacement module monitors the alignment characters in the received data stream and does corresponding character replacement based on frame and multi-frame boundaries in the data acquisition phase and will be bypassed in the CGS and ILA phase
- Character replacement depends on whether scrambling has been enabled or disabled.
- When Scrambler is disabled, the procedure for character replacement is as follows:
  - When the received control character is /A/, that equals 0x7C at the present end of the frame and in the previous end, if there is a special character /A/ or /F/, then the present octet needs to be replaced with the previous of previous end of frame data
  - When the received control character is /F/ that equals 0xFC at the present end of the frame, then it needs to be replaced with the previous end of frame data
- When Scrambler is enabled, there won't be any character replacement process since it will be taken care of by the descrambler module

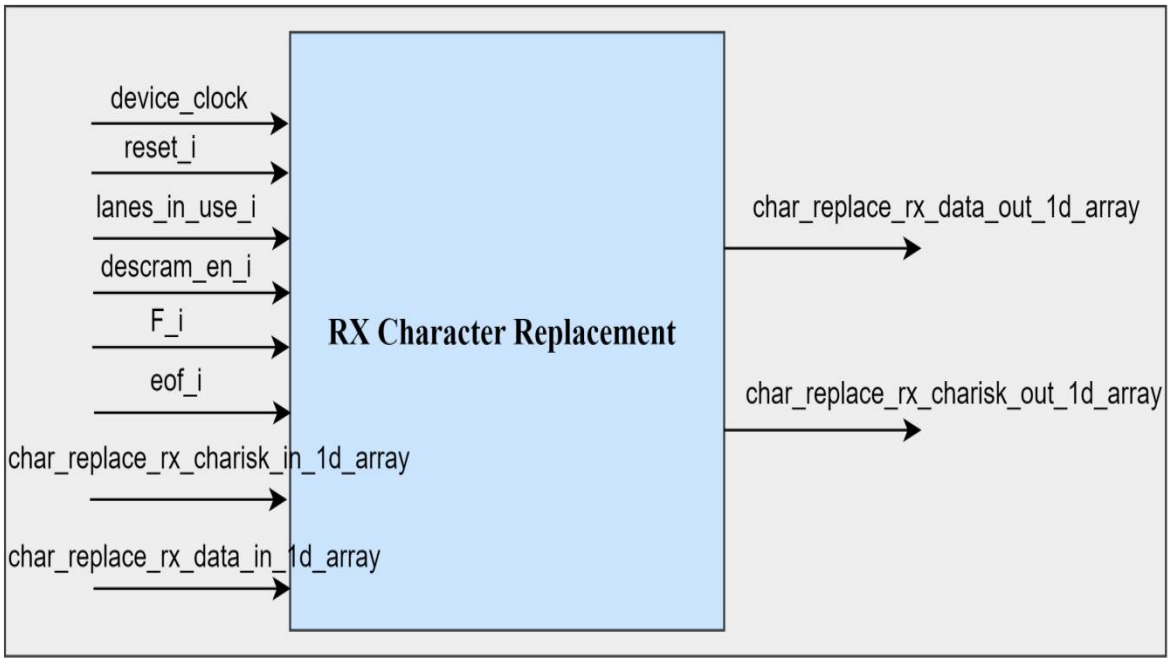


Figure 25. RX character Replacement I/O Signals

Signal	Direction	Bus Width	Description
Device_clk	IN	1	Device clock derived from the recovered clock
reset_i	IN	1	Active high reset signal
lanes_in_use_i	IN	8	Number of lanes inactive
descram_en_i	IN	1	Indicates whether descrambler is enabled or disabled
char_replace_en_i	IN	1	Indicates whether Character replacement is enabled or disabled
eof_i	IN	4	Indicates the end of the frame
F_i	IN	8	Indicates the total number of octets in

			a Frame
char_replace_rx_charisk_in_1d_array	IN	L*4	Indication of K character on the input data
char_replace_rx_data_in_1d_array	IN	L*32	Input data to the character replacement module
char_replace_rx_data_out_1d_array	OUT	L*32	Output data after the character replacement
char_replace_rx_charisk_out_1d_array	OUT	L*4	Indication of K character on the output data

Table 22. RX character replacement I/O signal description

4.4.2.7 Descrambler

- The descrambler module descrambles the incoming data based on the enabled signal.
- In the CGS and ILA phases, the descrambler is disabled
- In the data acquisition phase, the descrambler is enabled. Based on the enabled signal, it transmits original or descrambled data.
- The polynomial used for descrambling the data is $1 + x^{14} + x^{15}$

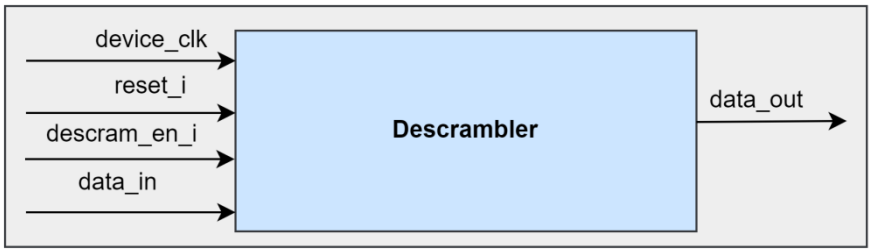


Figure 26. Descrambler Block I/O signals

Signal	Direction	Bus Width	Description

device_clock	IN	1	Device clock derived from the recovered clock
reset_i	IN	1	Active high reset signal
descram_en_i	IN	1	Enable signal for descrambler
data_in	IN	L*32	Input to the descrambler module
data_out	OUT	L*32	Descrambled or original data to the output

Table 23. Descrambler Block I/O signal Description

4.4.2.8 RX Gear Box

- This module handles the CDC between the data received from the Transceiver and the data processed inside the JESD204B RX IP.
- The FIFO module is used to take care of the clock domain crossing, where the write clock is the recovered clock from the transceiver for each lane, and the read clock is the device clock from the LMK.

4.4.3 Physical Interface

- JESD204b Physical layer includes Elitestek PMA and PCS Blocks.
- The PMA IP supports 20-bit data width. Maximum serial data rates support up to 5Gbps.
- Elitestek PMA example design contains 8b10b Decoding, word Alignment, and PMA initialization blocks. The same example design will be used for the JESD204b Physical layer.
- The following block diagram gives an overview of the example design of Elitestek RX PMA IP

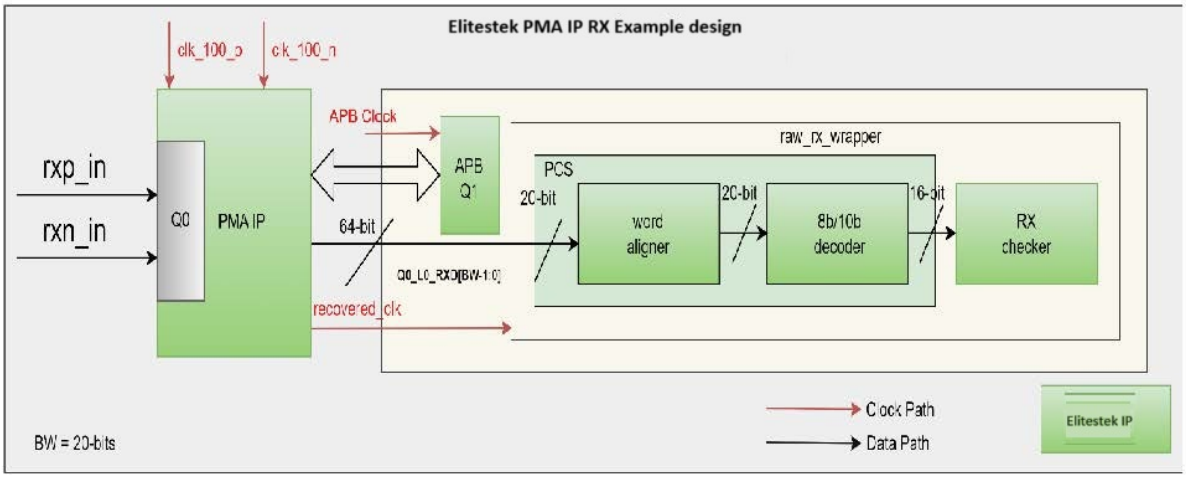


Figure 27. Elitestek PMA IP RX example design

The below diagram represents the RX valid data capture window

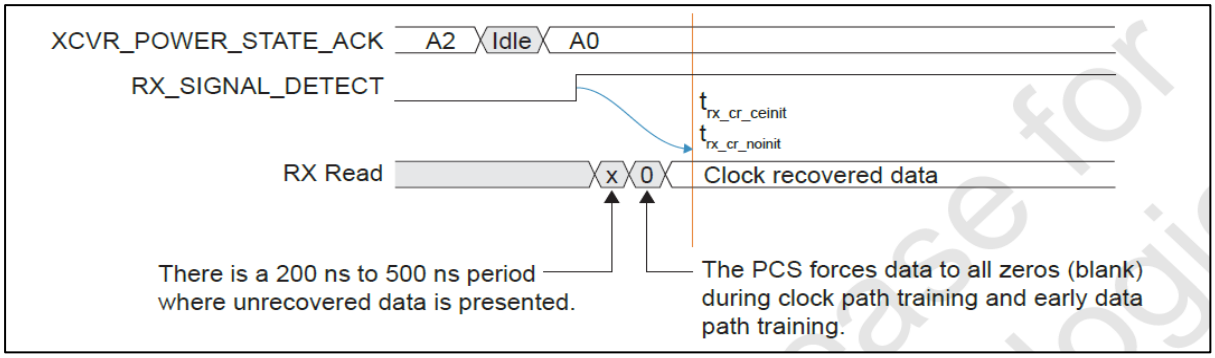


Figure 28.CDR Recovered Data window

4.4.3.1 Physical coding sublayer (PCS)

- The PCS module consists of the word aligner and 8b/10 decoder blocks
- The data received from the PMA IP is aligned using the word aligner block and passed to the decoder block.
- The 8b/10b decoding module receives the encoded data as input, recovers the clock from serial data, and decodes the encoded data.

4.4.3.2 Elitestek RX PMA IP

- The Elitestek RX PMA block consists of a timing flipflop, FIFO, and byte deserializer.

- The PMA RX block has two different modes of operation: FIFO mode and register mode.
- The FIFO path has extra latency but better timing, and the Register mode has lower latency with timing closure

Signal	Direction	Bus Width	Description
clk_100_p	IN	1	Onboard differential reference clock to the PHY block
clk_100_n	IN	1	Onboard differential reference clock to the PHY block
sys_reset_i	IN	1	System reset
recovered_clock	OUT	1	Output clock from the PHY block
reset_done_o	OUT	1	Reset done signal from the PHY block
rxn_in	IN	L	Serial Differential signal in
rxp_in	IN	L	Serial Differential signal in
rxdata_out	OUT	L*32	Data received on lane:- N
rxcharisk_out	OUT	L*4	Indicator for K character in received data on lane-

Table 24. PHY Block I/O Signals

4.4.4 Receiver Register Interface

The JESD204B RX core is configured using an AXI4-Lite Register Interface. The register map is shown in the table below.

Offset	Bits	Mode	Default	Description
0x1	31:12	**R**	20'h0	**Reserved**
	11	**R**	1'b0	**prbs_error_flag_i** 1: there is an error in PRBS data. 0: No error in PRBS data was received.
	10:0	**R**	0	**Reserved**
0x2	31:13	**R**	19'h0	**Reserved**
	12:0	**RW**	13'h20	**octets_per_mf_o** Number of octets per multi frame.
0x8	31:1	**R**	31'h0	**Reserved**
	0	**RW**	1'b0	**reg_ip_reset_o** Reset the JESD204b IP.
0xD	31:1	**R**	31'h0	**Reserved**
	0	**RW**	1'b1	**sub_class_o** 0: backward compatible with JESD204a. 1: uses external reference signal SYSREF.
0xF	31:24	**RW**	8'h3	**multi_frames_in_ila_o** Error counter for disparity errors received in transceiver lines.
	16	**RW**	1'b0	**scrambling_o** 0: Scrambler is disabled. 1: Scrambler is enabled.
	15	**RW**	1'b0	**prbs_en_o** 0: Incremental data. 1: PRBS data.
	14	**RW**	1'b0	**prbs_sync_o** Toggle this bit to reset the error flag.
	12:8	**RW**	5'h1f	**frames_per_multiframe_o** Number of Frames in a multi-frame.
	7:0	**RW**	8'h1	**octets_per_frame_o** Number of Octets per frame.
0x10	31:8	**R**	24'h0	**Reserved**
	7:0	**RW**		**lanes_in_use_o** Number of transceiver lanes in use.
0x11	31:13	**R**	19'h0	**Reserved**
	12:0	**RW**	13'h0	**buffer_adjust_o**

0x14	31:1	**R**	31'h0	**Reserved**
	0	**RW**	1'b0	**sysref_always_o** 0 - LMFC counter aligns for every SYSREF event. 1 - LMFC counter aligns only on the first SYSREF event after transceiver_reset_done and ignores all the subsequent SYSREF events.
0x18	31:3	**R**	29'h0	**Reserved**
	2	**R**		**sysref_alarm_i** Indicates the misalignment between LMFC and SYSREF.
	1	**R**		**sysref_captured_i**
	0	**R**	1'b0	**Reserved**

Table 25. Receiver Register Address Map

4.5 JESD204B Receiver Hardware Testing Overview

4.5.1 Hardware Testing Block Diagram

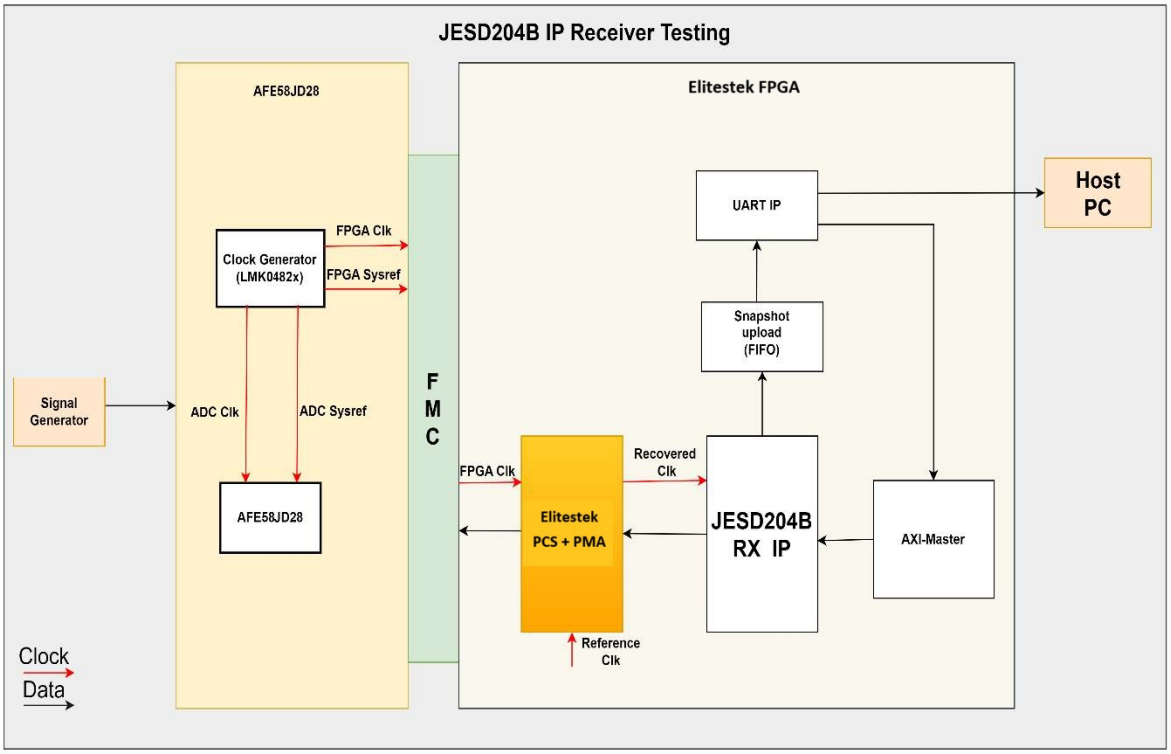


Figure 29.JESD204B IP Receiver Testing Block diagram

4.5.2 I/O Signal Description

Table 26. JESD204B RX application I/O signal description

Signal	Direction	Bus Width	Description
clk_100_p	IN	1	Positive differential reference clock
clk_100_n	IN	1	Negative differential reference clock
clk_25	IN	1	On-board system clock
sys_reset	IN	1	On-Board reset
uart_tx	OUT	1	UART TX signal
uart_rx	IN	1	UART RX signal
rxp	IN	L	Transceiver positive receiver signal
rxn	IN	L	Transceiver negative receiver signal
sysref_p	IN	1	LMK sysref clock to FPGA p/n
sysref_n	IN	1	
adc_sync_ab_p	OUT	1	SYNC signal from FPGA to ADC
adc_sync_ab_n	OUT	1	
adc_sync_cd_p	OUT	1	
adc_sync_cd_n	OUT	1	

Table 27. JESD204B RX application I/O signal description

4.5.3 Block Description

4.5.3.1 Snapshot upload

- The Snapshot upload module contains a FIFO of fixed size (64k samples) to store the incoming data.
- When the user requests data, the JESD204b Rx IP data is captured in this block and uploaded to the host machine using UART.

- This block cannot stream the data continuously. It is used only to analyze data from fixed samples.

4.5.3.2 UART IP

- The UART module is used for the user control interface
- The dynamic programming of the JESD204B IP Registers is done through the UART interface.

4.5.3.3 AXI- Master

- The AXI-Lite controller module will be used for the configuration of the register interface required for programming the register set of JESD204B RX IP
- This register set configuration is necessary to link up JESD204B IP.

4.6 RX Resource Utilization

- The following resource utilization is done for the JESD204B RX Link layer, Transport layer, Physical layer, and Application layer

Modules	Resources					
	LUTs	FFs	SRLs	ADDs	RAMs	DSP/MULTs
JESD204B RX link layer	4214	7903	0	237	288	0
Transport layer	460	396	0	0	0	0
Physical Layer	5361	4366	0	256	64	0
Application layer	1,875	1,950	76	313	256	0
TX_top_module	11910	14615	76	806	608	0
Available	362880	362880	67200	362880	2688	1344

Utilization %	3.28207672	4.027502205	0.113095238	0.222111993	22.61904762	0

Table 28. RX Resource Utilization

5 JESD204B Transmitter and Receiver Clocking Architecture

The below clock tree shows the JESD204B Transmitter and Receiver clocking scheme.

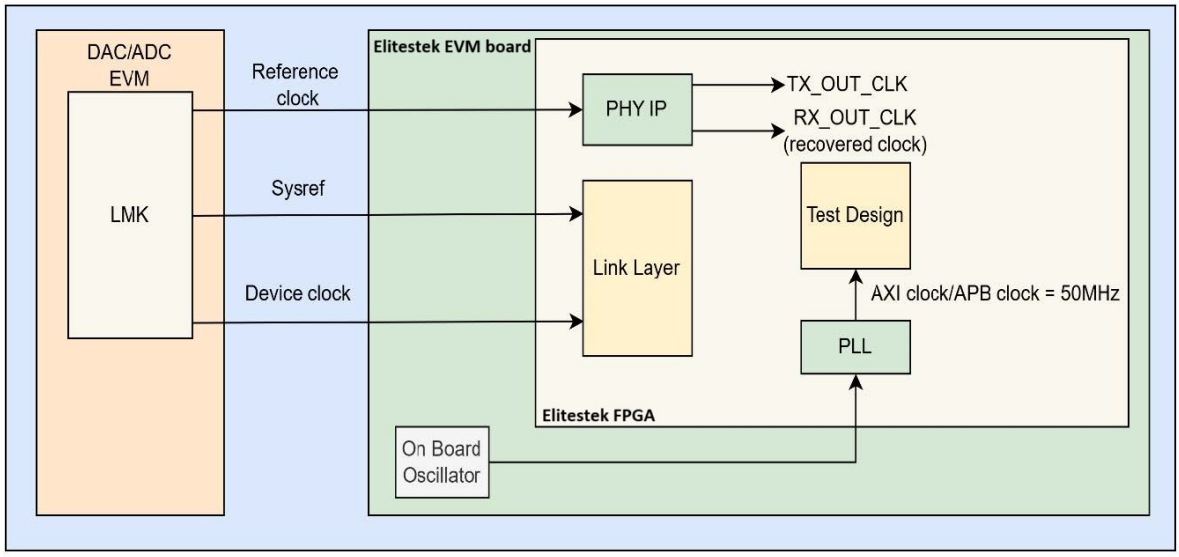


Figure 30.JESD204B IP clock tree

The table below describes the JESD204B Transmitter and Receiver clock signals

Clock Signal	Description
Reference clock	Differential reference clock as an input to the Transceiver
Sysref	Clock signal used for synchronization of the clocks and other parameters in DAC and ADC
Device clock	The link layer operates at this clock. The frequency is the same as the transceiver output clock
TX out clock	The transceiver TX output clock
RX out clock	Recovered clock from the transceiver
AXI clock	The test application modules operate at the AXI clock.

Table 29. RX Clock Signals description

6 JESD204B Simulation

6.1 Simulation Architecture

The following block design describes the simulation flow for testing the JESD204B TX and RX Design with the Elitestek PMA IP.

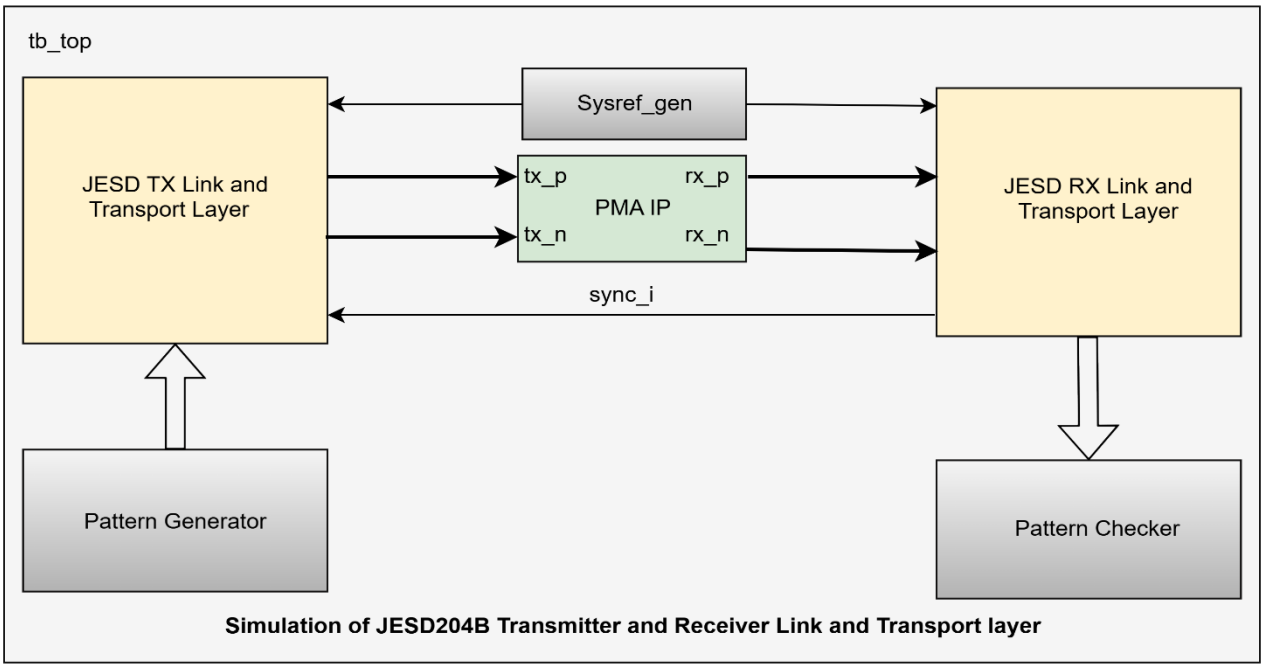


Figure 31. Simulation architecture for the JESD204B Link and Transport Layer

6.2 Block Waveform Captures

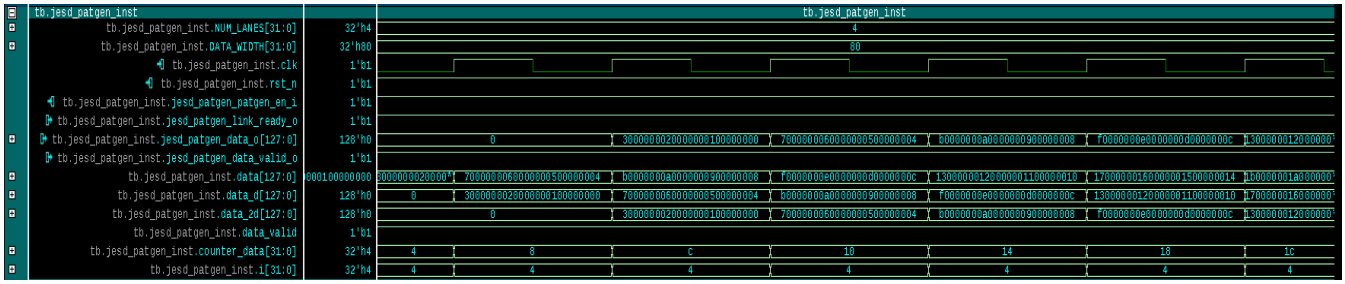
The simulation is done for the following JESD204B configuration:

- Number of Lanes = 4
- Number of octets (F) = 2 (0,1)
- Number of Frames per multi-frame (K) = 32 (0,1,2….31)
- Number of Octets per frame = F x K = 64

6.2.1 JESD204b TX

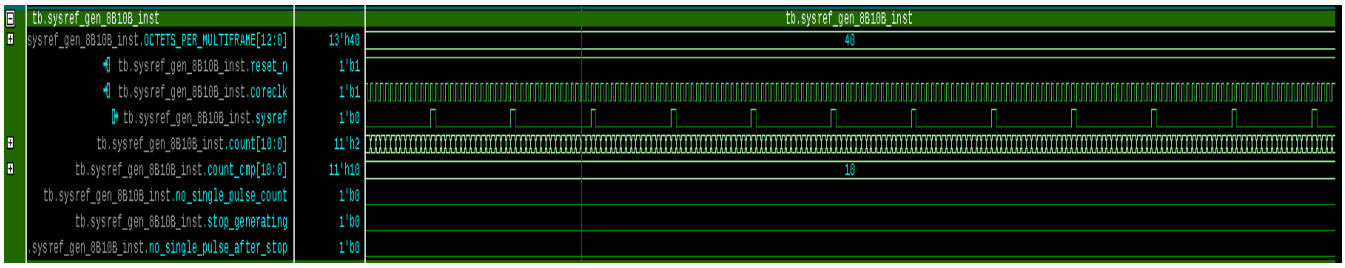
➢ Pattern Generator module

The pattern generator module is instantiated in the test bench top module (tb. v) and generates the incremental data



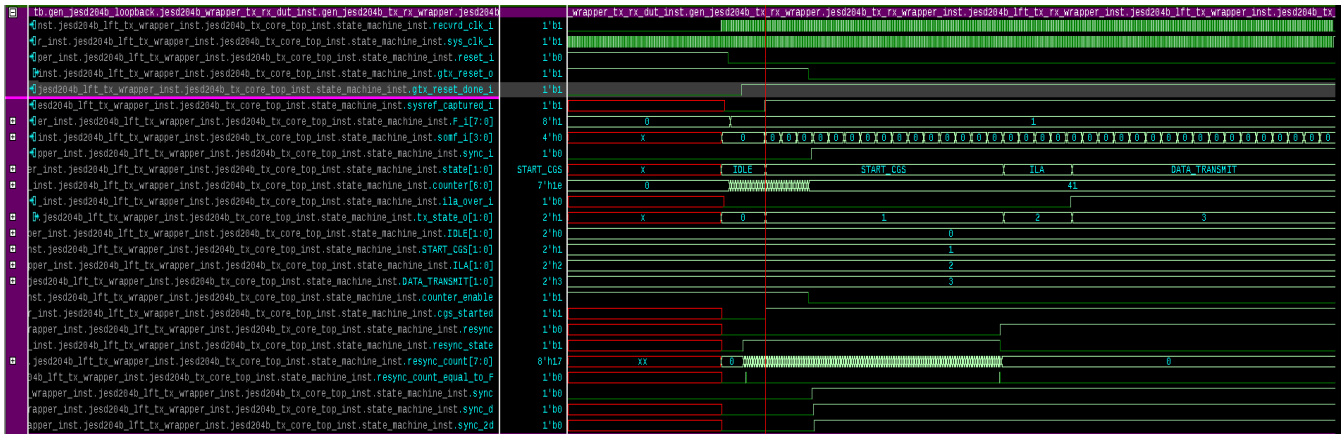
- Sysref Generation module

  The sysref generator module is instantiated in the test bench top module (tb. v) and generates the sysref signals in terms of pulses for subclass 1



- TX State module

  The below waveform describes the transition of different states concerning the control signal.

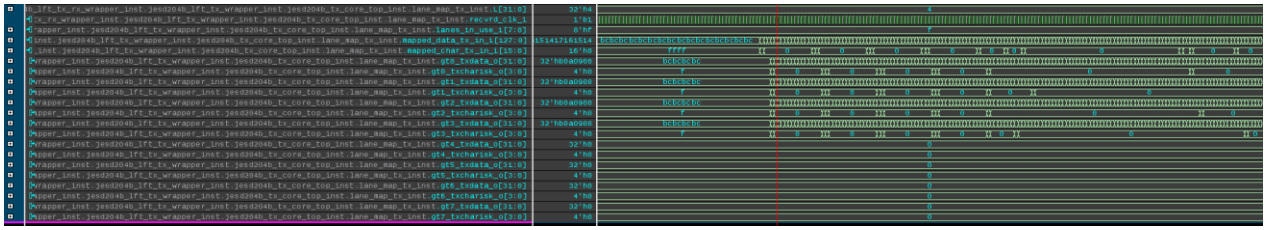


- TX CGS ILA Data

  The below waveform represents the CGS and ILA data generated with respect to the states.

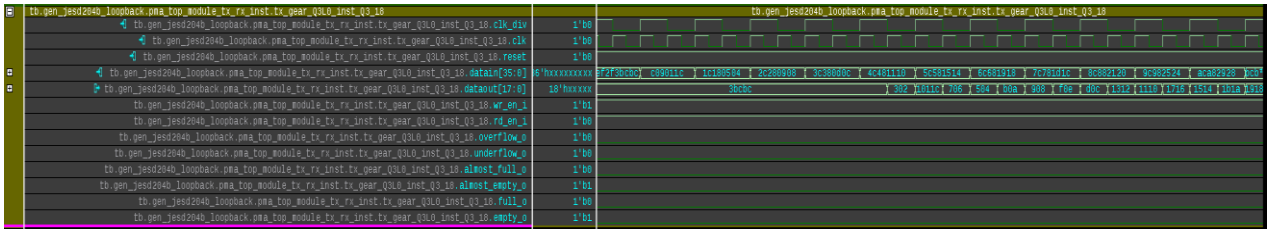
- TX lane mapping

  The TX data is transmitted to the selected four lanes of the transceiver



- TX Gear Box

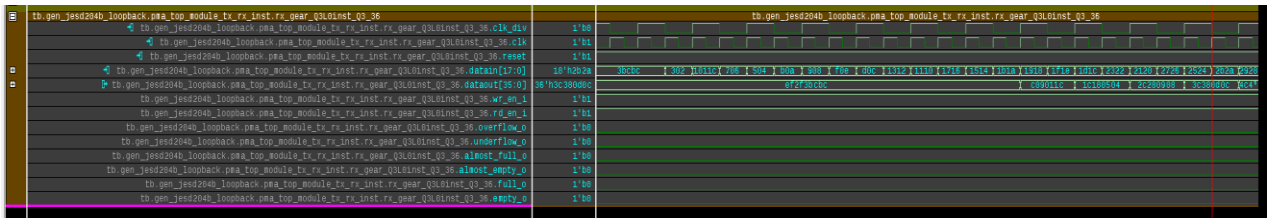
  The 36-bit data (32-bit data and 4-bit character indicator) is converted to 18-bit data (16-bit data and 2-bit character indicator) and transmitted to the Physical layer.



6.2.2 JESD204B RX

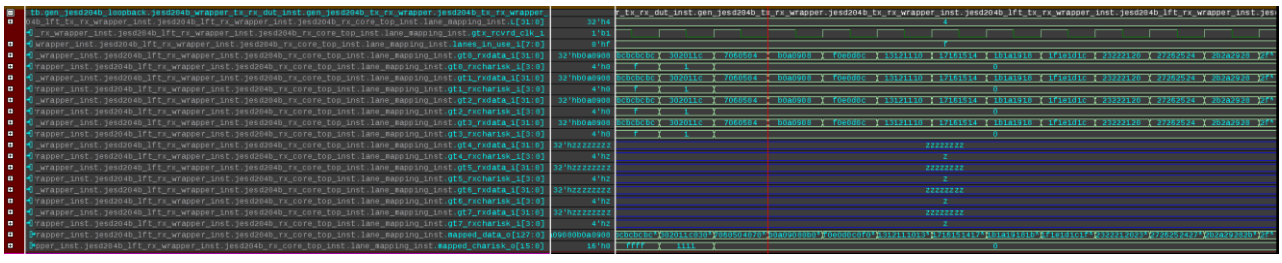
- RX Gear Box

  On the receiver end, the 18-bit data from the physical layer is converted to 36-bit data and transmitted to the RX link layer.



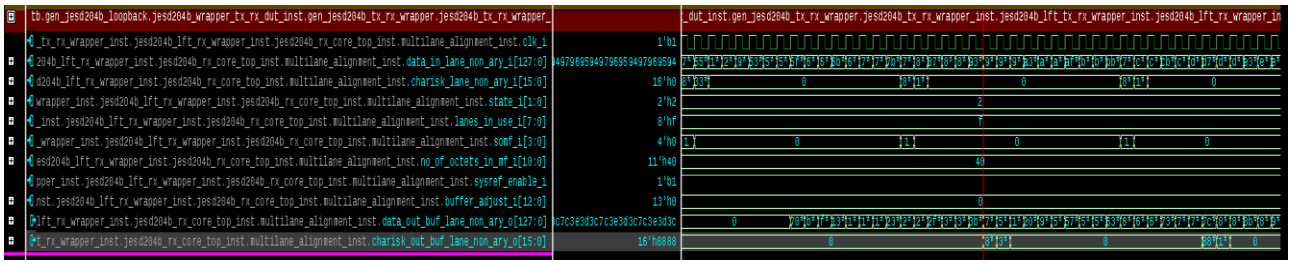
- RX lane mapping

  The 32-bit data received from 4 lanes are mapped to 128-bit for further processing.



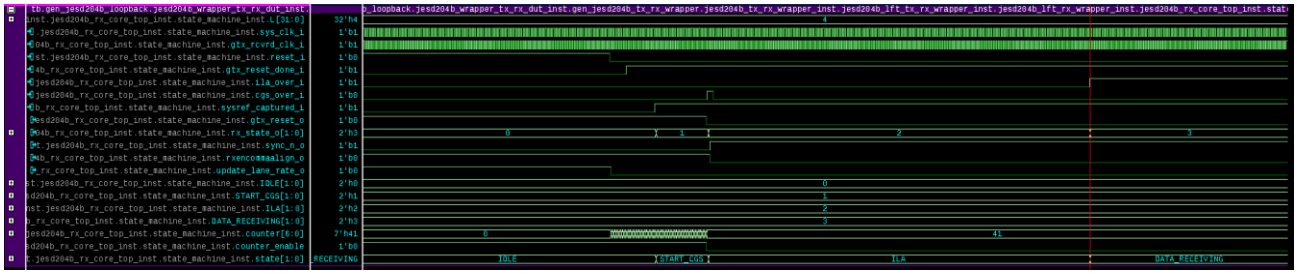
- Multilane alignment

In this module, the data is released when an R character is received on all the lanes for subclass 0 and for subclass 1 when an R character is received and an LMFC rising edge is detected.



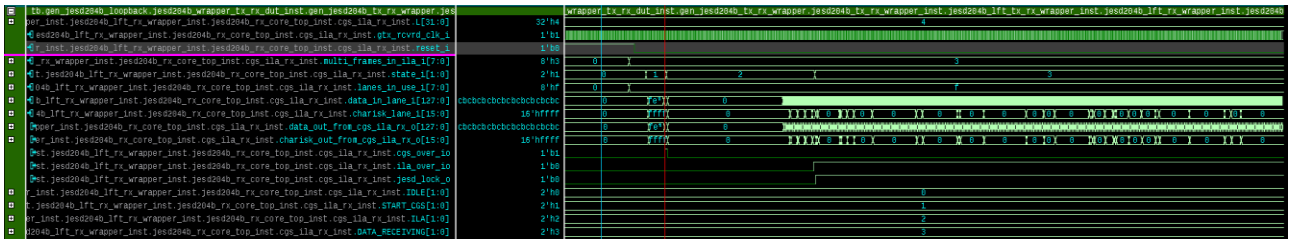
- RX State module

The waveform below describes the transition in the RX states concerning the received control signals.



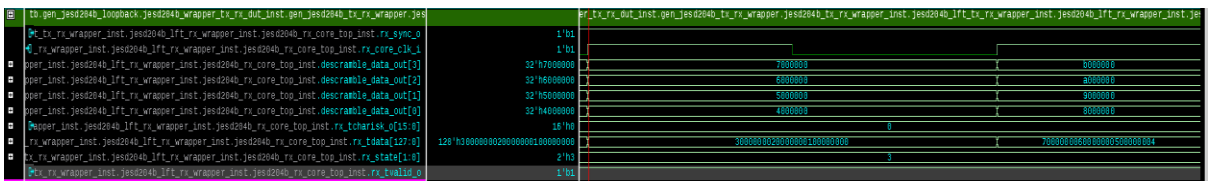
- RX CGS ILA data

The detection of CGS and ILA data concerning the states.



- RX out data

The output data is descrambled and transmitted to the Transport layer



6.3 Simulation Steps

Simulation is done using the Quest Sim IDE in the Linux Environment

The following are the steps to run the JESD204B TX and RX simulation with PMA IP:

1. Go to the demo sim directory and execute the following to run the simulation:
    a. Export the Questa Sim software by the command:
    export PATH=/Disk_Drive/Software/Questa_sim-2023.4/questasim/bin:$PATH
    b. Run the design using the command: make simqrun mode=FIFO
    c. Once the simulation is run, to load the waveform, run the command: run the visualizer &
    d. Load the design.bin and wave.db file to check the waveforms

7 Hardware Validation for JESD204B Transmitter with DAC

7.1 Hardware Validation Block Diagram

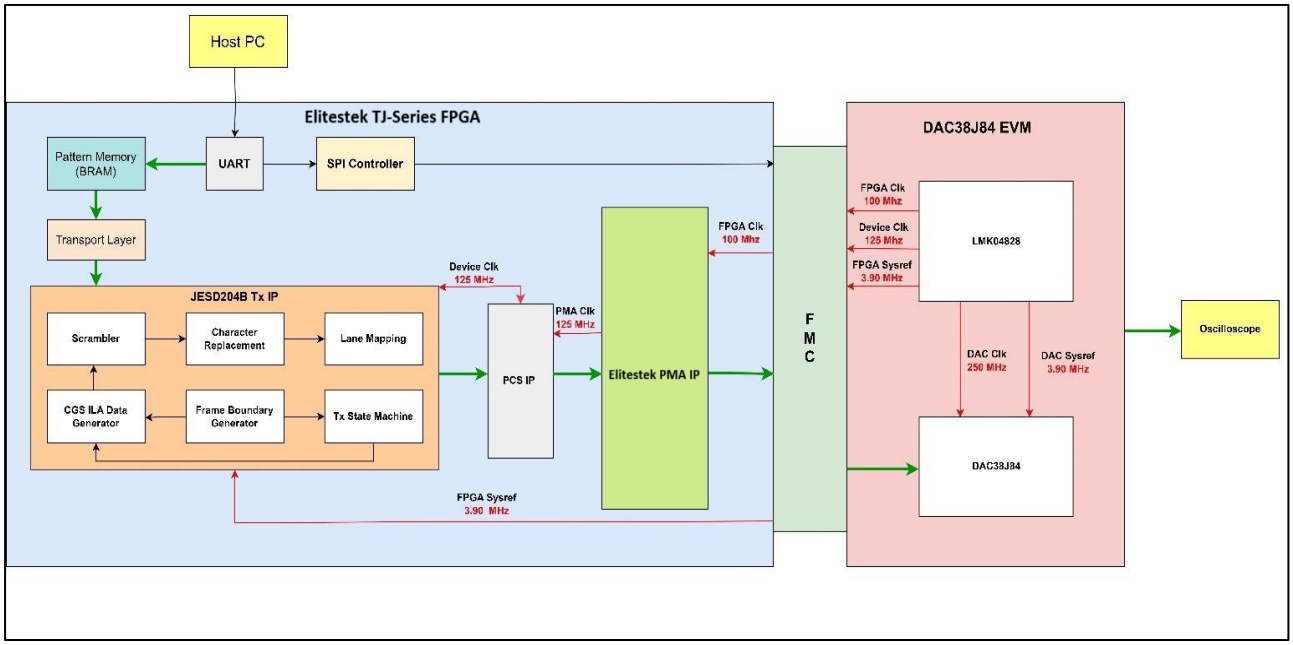


Figure 32. Hardware Validation Block Diagram of JESD204B Transmitter with DAC38J84 at 5 Gbps Line Rate

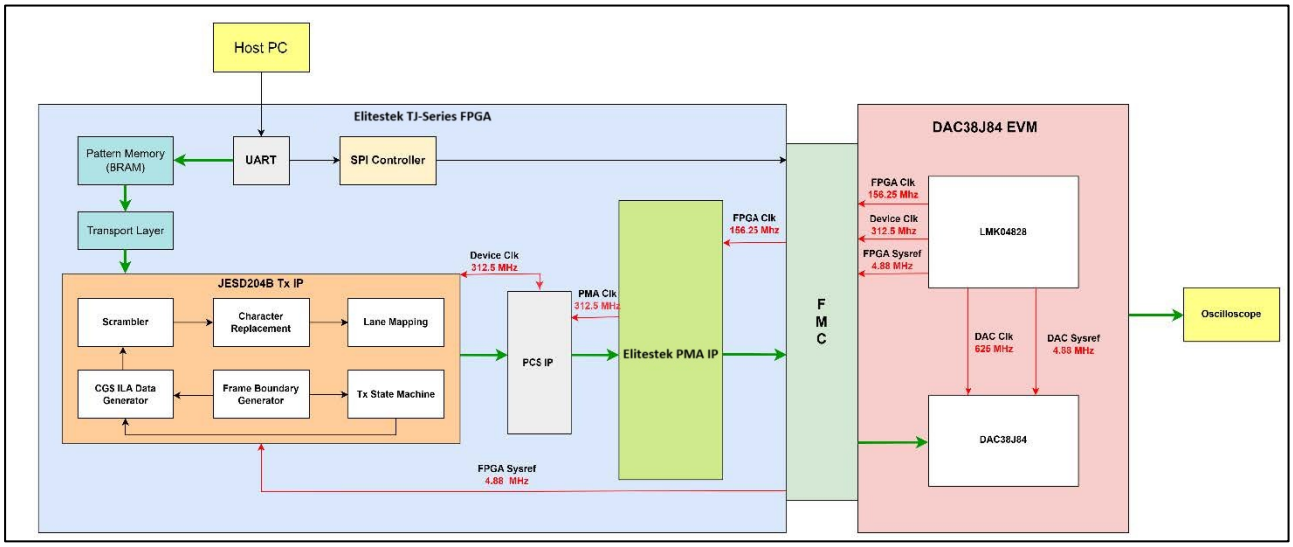


Figure 33: Hardware Validation Block Diagram of JESD204B Transmitter with DAC38J84 at 12.5 Gbps Line Rate

Note: For Detailed information on blocks, refer to section 3.5 (JESD204B Transmitter Hardware Testing Overview)

7.2 Test Set up of Elitestek Evaluation Board with DAC

7.2.1 Test Setup image

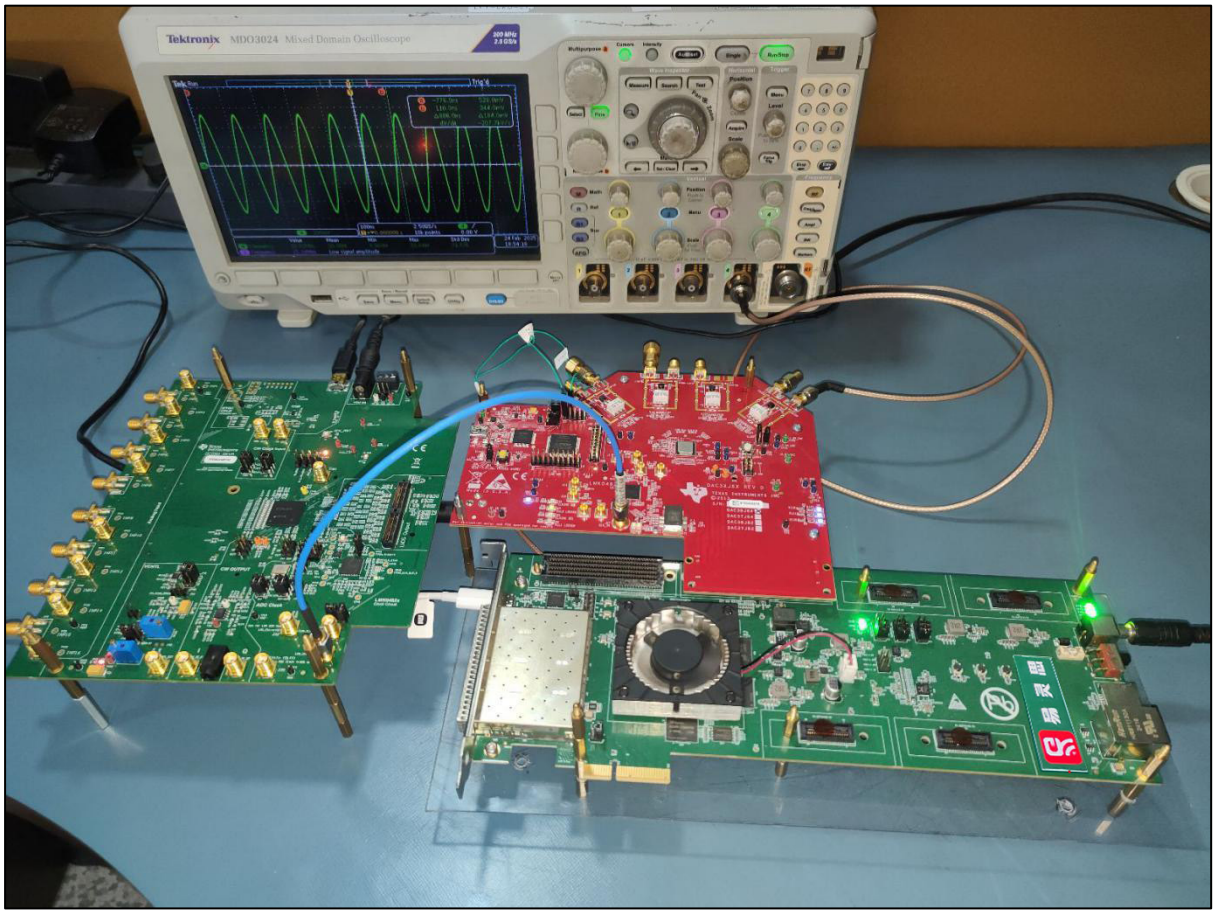


Figure 34. Test Setup of Elitestek Evaluation Board with DAC

7.2.2 Hardware Test Equipment

Following are the test set up equipments:

S. No.	Hardware Requirement for DAC Demo	Quantity
1	Elitestek TJ375N1156X Eval board	1
2	Type A to Type C USB cable	1
3	12V - 6A Power Adapter	1

4	DAC EVAL board	1
5	5V 3A power adapter	1
6	SMA Female connectors for DAC outputs	4
7	50-ohm terminations for DAC outputs	4
8	SMA to female header jumper cable	1
9	SMA to SMA cable	2
10	Scope probe	1
11	Some studs to make setup mechanically stable	20-25
12	Oscilloscope	1
13	Oscilloscope power cord	1
14	Laptop (should have Efinity 2024.2 and tcl installed in it)	1
15	Laptop charger	1

Table 30. Hardware Requirements for JESD204B Transmitter Demo

7.2.3 Software Used

7.2.3.1 LMK Tool

- The LMK Tool version used is v1.7.7.6
- This tool configures the LMK04828 chip in the DAC evaluation board.
- After selecting the LMK device, according to the required clock values, the user needs to make the settings in the GUI and update the register set values in the tcl procs accordingly.

7.2.3.2 DAC GUI

- The DAC GUI version used is 1.3.
- This tool configures the DAC chip DAC38J84 and the JESD204B Rx Protocol on the DAC38J84 EVM.

- According to the required mode, the user must select the settings in the DAC GUI and update the register set values in the tcl procs accordingly.

7.3 Test Procedure

7.3.1 Hardware Connection Procedure

1. Connect TI DAC EVM (TI DAC38J84)with the Elitestek TJ-Series Evaluation (TJ375N1156X) Board on the **J14 FMC connector** (Quad 3).
2. Connect host PC with Elitestek TJ-Series Evaluation Board via USB cable, which can be used as UART and JTAG
3. Start the Oscilloscope and connect it with DAC EVM through SMA cables.
4. Open the Efinity Programmer and program the required bit file or Hex file.
5. To provide a 100MHz clock input to the DAC LMK, you can either connect the SMA cable from the "J28" SMA connector of the ADC to the "J17" SMA connector of the DAC or supply the clock from an external clock generator and connect it to the "J17" SMA connector of the DAC.
6. If Clock is through ADC , make sure to upload the ADC configuration file for 100MHz LMK output

7.3.2 TCL Script Sequence Test Procedure

1. The following steps to be followed for the installation of LFT TCL Software
    i. Go to Control Panel -> Add / Remove Program -> Turn Windows Feature on or off - > Enable.NetFramework 3.5
    ii. Let it be downloaded from Windows Update
    iii. Copy LFT_TCL folder present in the path : ..\JESD204B_Porting_Efinix_REL_1_0\TCL_Software inside the C:\
    iv. Install TclTk-8.3_for_N2X.exe
    v. Install vcredist_x86.exe

vi. Run Win_Driver.bat (present in the path LFT_TCL\bin_USB_UART) as Administrator to confirm the correct installation

2. There are two tcl files present inside the below path: ../JESD204B_Porting_Efinix_REL_1_0\JESD204B_TX_DAC_Files\TCL_Script_Software\TCL_Script:

   i. tclshrc.tcl: This TCL script contains the possible modes and is the main TCL script used to run the possible test cases.

   ii. jesd204b_tx_procs.tcl: This tcl contains the procs to configure LMK04828, DAC38J84, LFT JESD204B TX IP.

3. Keep the tclshrc.tcl file in the path: C:\Users\user (*Note: username can change from PC to PC*)

4. Make sure the jesd204b_tx_procs.tcl file is present in the path: C:\LFT_TCL\bin_USB_UART

5. Inside the path C:\LFT_TCL\bin_USB_UART, there is a Ukko_init.tcl file, where we need to set the baud rate and com port

   Set the baud rate to 115200 and the com port according to the detected port.

```
19
20  #g_comPort:   UART => UART COM Port#
21  set g_comPort 9
22  #g_comPort:   UART => UART BaudRate
23  set g_baudrate 115200
```

Figure 35.Com port and Baud rate settings for DAC

Note: Initially, while setting up the tcl, the user needs to make these directories

6. Ensure all sample input data hex files for different modes are inside the path: C:\LFT_TCL\bin_USB_UART. (These hex files are also separately present in the path D:\Effinity\Release\JESD204B_Porting_Efinix_REL_1_0\JESD204B_TX_DAC_Files\Sample_input_data)

7. Open the TCL IDE from the start menu by default. The required TCL script is sourced

8. The console will display 4 options to select the testing for the JESD204B Transmitter with DAC or JESD204B Receiver with ADC. Select option 1 to test the JESD204B Transmitter with DAC at 5 Gbps line Rate.

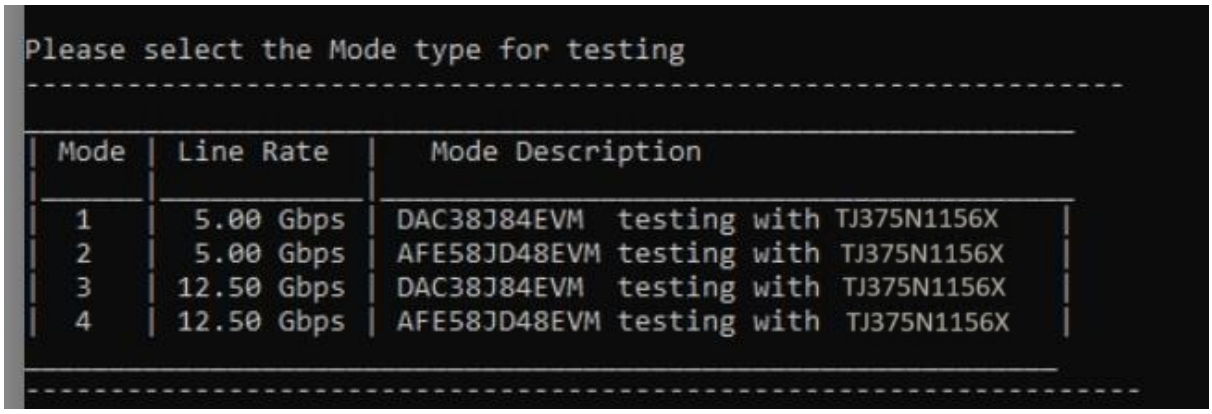


Figure 36.DAC TCL Consoleprints_1

9. The user must select the DAC test cases (Modes) and enter a number from 0 to 7 according to the requirement.

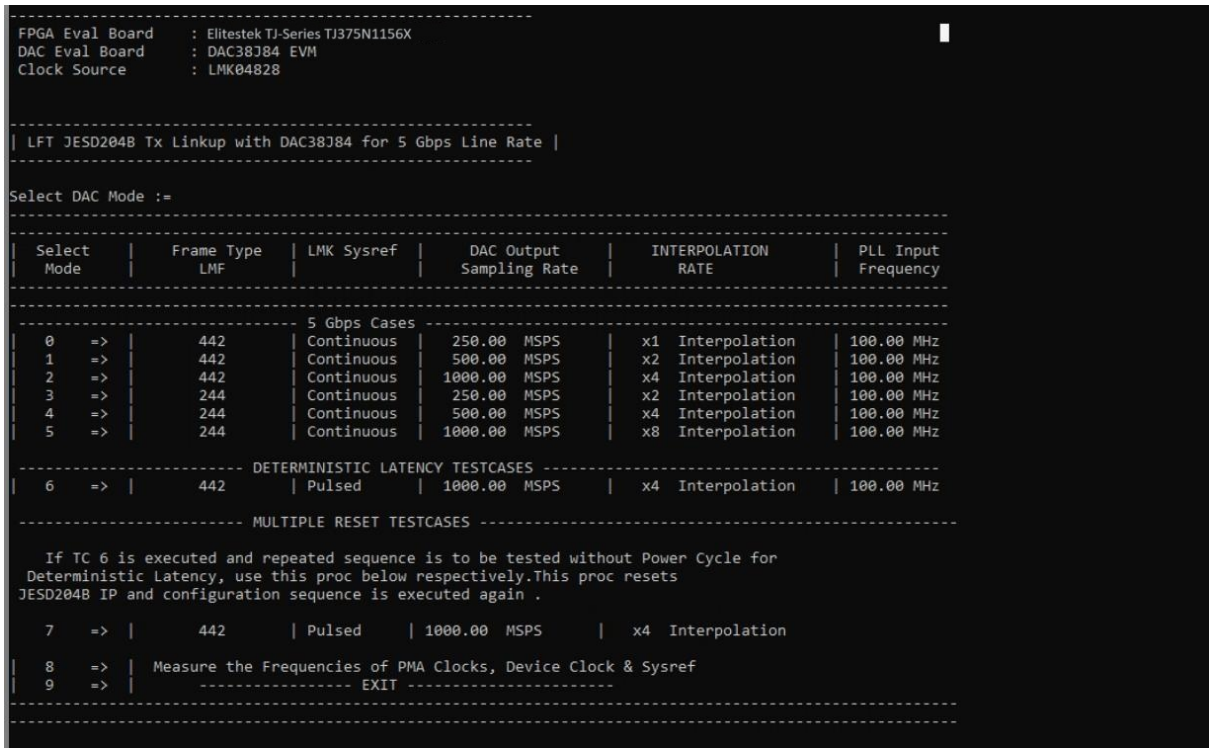


Figure 37. TCL console prints_2

10. The second input is the selection of the sub-modes,

    i. Selection of the mode ‘a’ is done when LMK04828 is configured for the first time after being powered up. This mode ensures that LMK04828 is configured so that clocks are available to Elitestek PMA IP, as it requires clocks before bit file configuration to generate the necessary PMA clocks.

    ii. Selecting mode ‘b’ will run the complete sequence required to link JESD204B TX IP with the DAC and configure the pattern memory with data samples.

    This mode runs the following procs in the order given below :

    a. LMK04828 Configuration
    b. DAC38J84 Configuration
    c. LFT JESD204B TX IP Configuration
    d. LFT JESD204B TX IP Reset
    e. DAC38J84 JESD204B RX IP reset
    f. JESD Lock Status checking
    g. Clear DAC Alarms
    h. Check DAC Alarms
    i. Sending DAC Samples
    j. Selection of the frequency

    Note: This mode should only be run after mode “a” has been run at least once after powering up.

```
6
**********************
Select the sub-mode :=
----- a - LMK04828 Configuration only:              ----------------------
        After Power cycle, LMK needs to be configured before Bitfile reprogamming to configure PMA clocks correctly
        Hence this mode required to be run atleast once immediately after Power cycle, then reprogram Bitfile again
----- b - LFT JESD204B Tx IP linkup with TI DAC38J84 ----------------------
        This mode should be only when run when mode 'a' has been run once after Power cycle
        This mode executes all the procedures required for valid linkup
```

Figure 38.DAC TCL Console image_3

11. On selection of ‘a’, LMK gets configured.

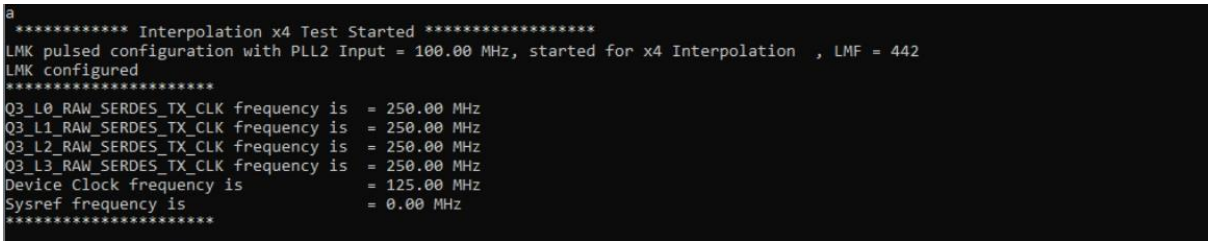


Figure 39.DAC TCL Console image_4

12. Reprogram the bit file after selection of the 'a' mode or, in the case of the MCS file programmed, power cycle only the Elitestek Evaluation Board

13. Select the 'b' option. This will display the JESD204B lock status and DAC errors

Figure 40.DAC TCL Console image_5

14. Select the input frequency

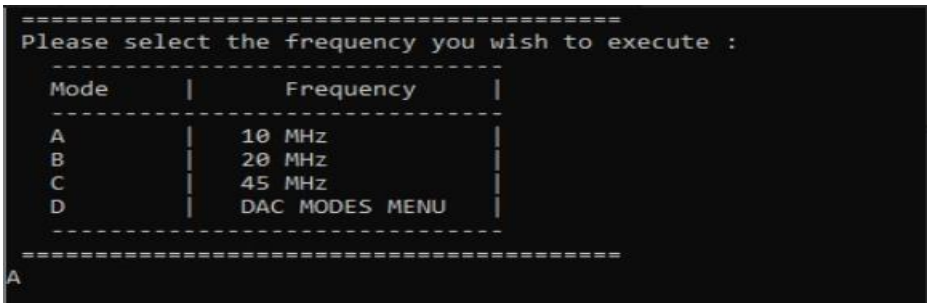


Figure 41.DAC TCL Console image_6

15. View the output waveform on the oscilloscope.

For example, the input frequency is 10MHz,

Figure 42.DAC output waveform for input frequency as 10MHz

7.4 Test Cases for 5Gbps

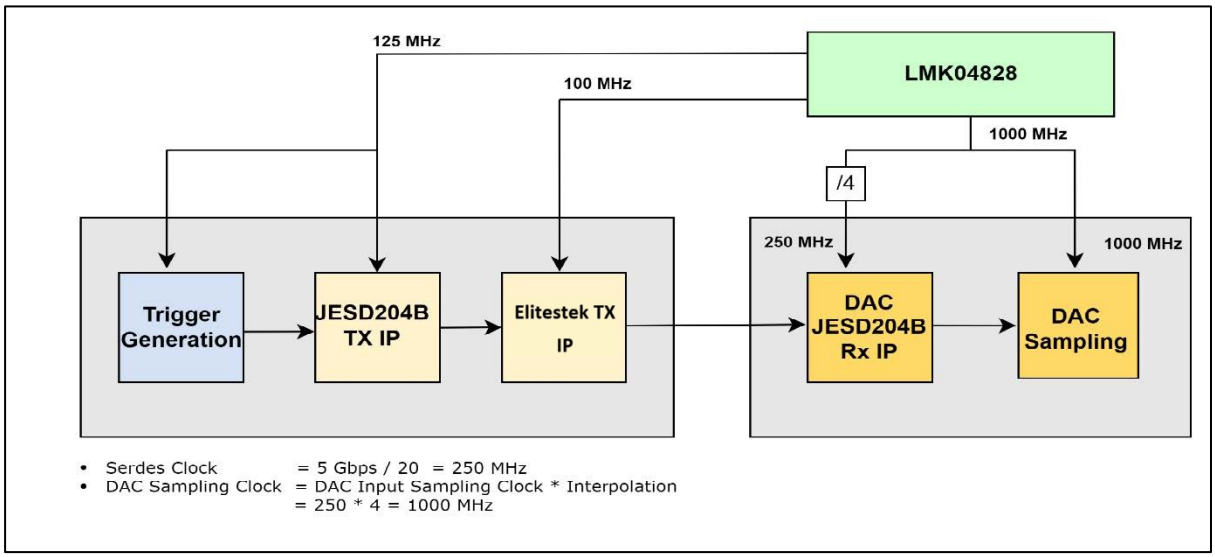


Figure 43: Block Diagram depicting Clock Architecture for 5 Gbps Line Rate

SerDes Clock = SerDes Rate / SerDes Data Width

Chipset	SerDes Rate	SerDes Data width (Resolution after 8b10b)	SerDes Clock
LFT JESD204B TX (Elitestek FPGA)	5 Gbps	40 bits	125 MHz
TI DAC38J84	5 Gbps	20 bits	250 MHz

Table 31. Elitestek Eval board and DAC Data rate Table

- Serdes Rate = 5 Gbps
- FPGA JESD204B Clock = 125 MHz
- FPGA Reference Clock = 100 MHz
- FPGA Sysref = 3.90 MHz
- DAC Clock = 250 MHz
- DAC Sysref = 3.90625 MHz
- No. Of Frames per MultiFrame (K) =32

DAC Input sampling rate = SerDes Rate / (DAC Resolution after 8b10b * No of converters in a single lane)

DAC Output sampling rate = DAC Input sampling rate * Interpolation Factor

The following are the different modes of testing done for DAC:

Test Case	Modes (LMF)	Interpolation	No. of converters in single-lane	DAC Input Sampling Rate (MSPS)	DAC Output Sampling Rate (MSPS)	LMK Sysref	PLL2 Input Frequency (MHz)
0	442	x1	1	250.00	250.00	Continuous	100.00
1	442	x2	1	250.00	500.00	Continuous	100.00

2	442	x4	1	250.00	1000.00	Continuous	100.00
3	244	x2	2	125.00	250.00	Continuous	100.00
4	244	x4	2	125.00	500.00	Continuous	100.00
5	244	x8	2	125.00	1000.00	Continuous	100.00
Deterministic Latency Testing							
6	442	x4	1	250.00	1000.00	Pulsed	100.00
Multiple Reset testing							
7	442	X4	1	250.00	1000.00	Pulsed	100.00

Table 32. JESD204B Transmitter Test Cases for 5 Gbps

7.4.1 Test Case 0 : LMF = 442, x1 interpolation

7.4.1.1 Input Frequency = 10MHz

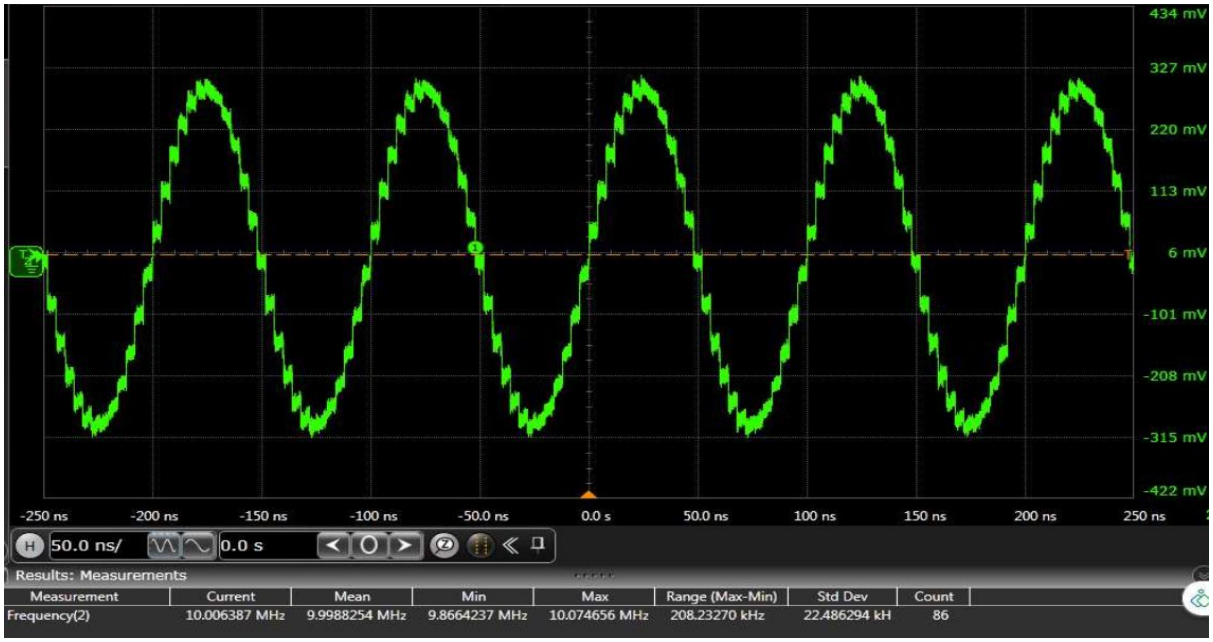


Figure 44. TC0 : Time domain 10 MHz output waveform for x1 interpolation, LMF = 442 mode

7.4.1.2 Input Frequency = 20MHz

Figure 45.TC0: Time domain 20 MHz output waveform for x1 interpolation, LMF = 442 mode

7.4.1.3 Input Frequency = 120MHz

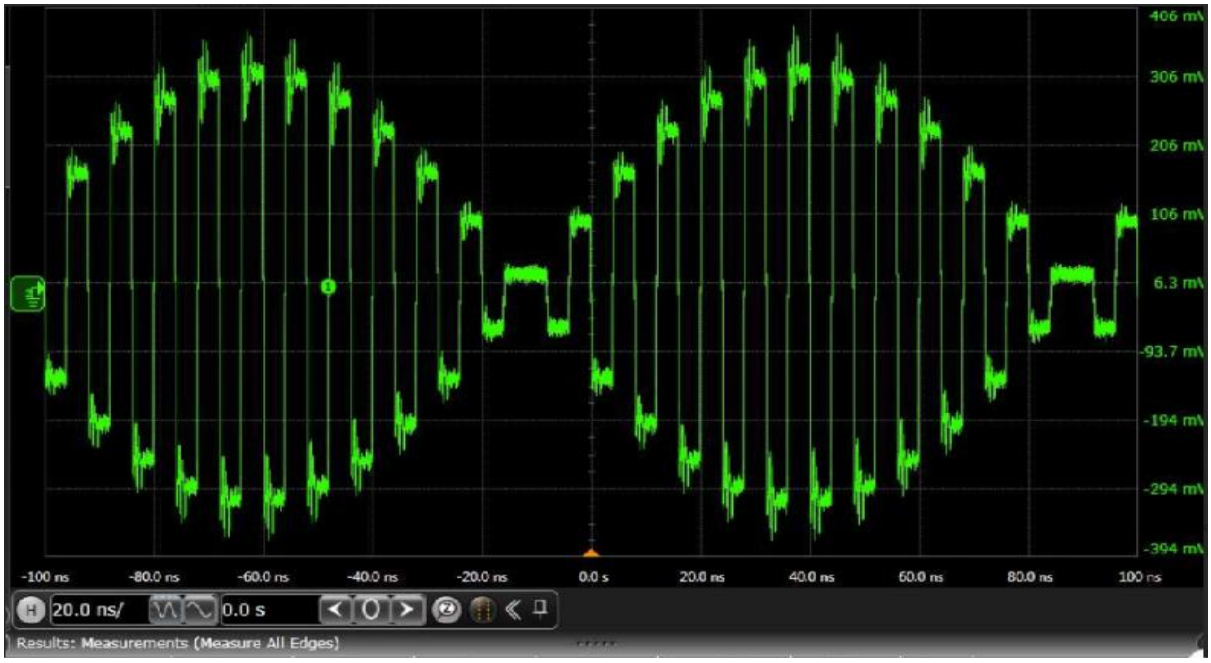


Figure 46.TC0: Time domain 120 MHz output waveform for x1 interpolation, LMF = 442 mode

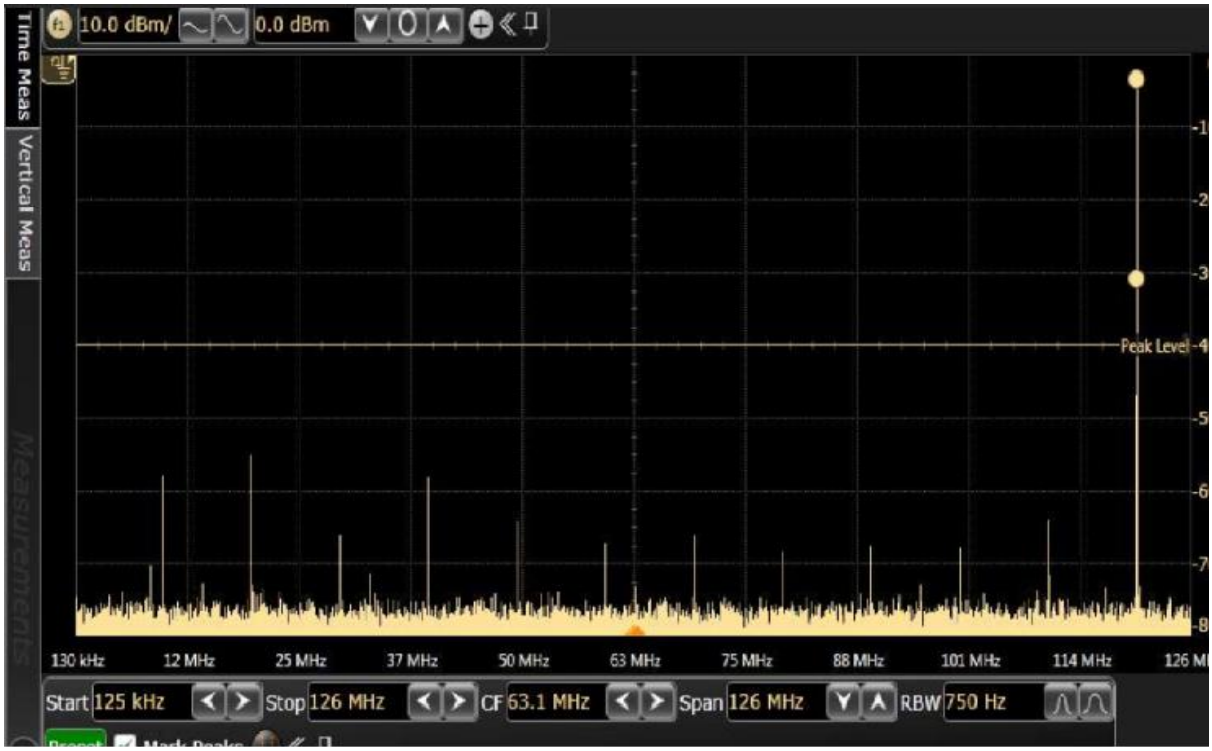


Figure 47.TC0: Frequency domain 120 MHz output waveform for x1 interpolation, LMF = 442 mode

7.4.2 Test Case 1: LMF = 442, x2 interpolation

7.4.2.1 Input Frequency = 10MHz

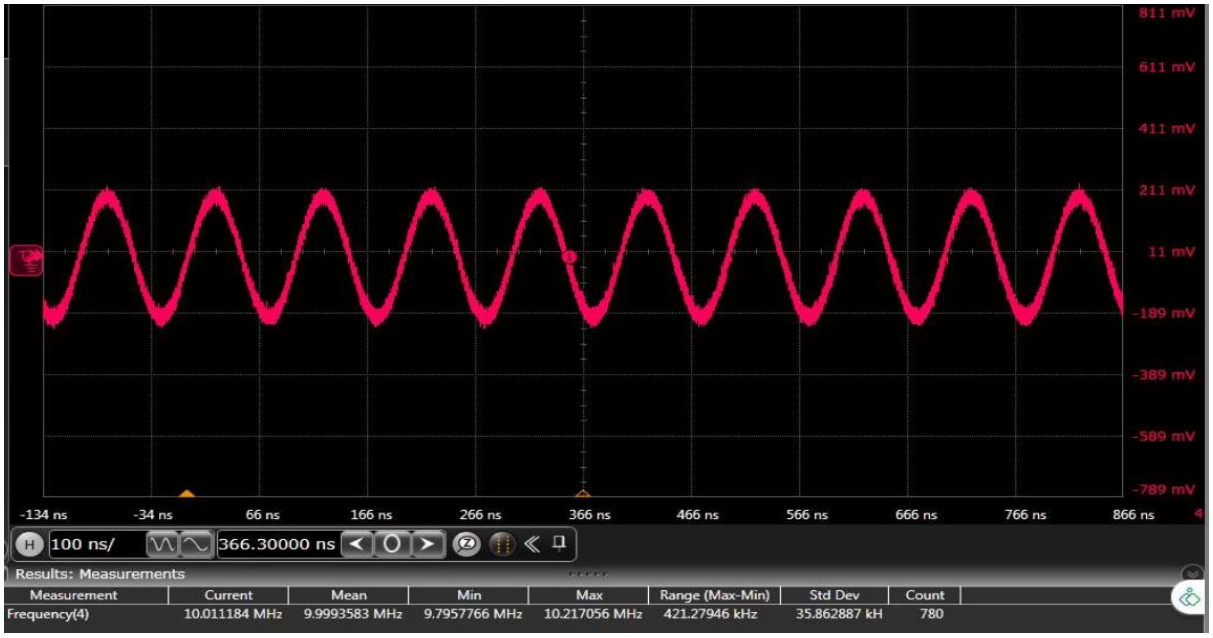


Figure 48.TC1: Time domain 10 MHz output waveform for x2 interpolation, LMF = 442 mode

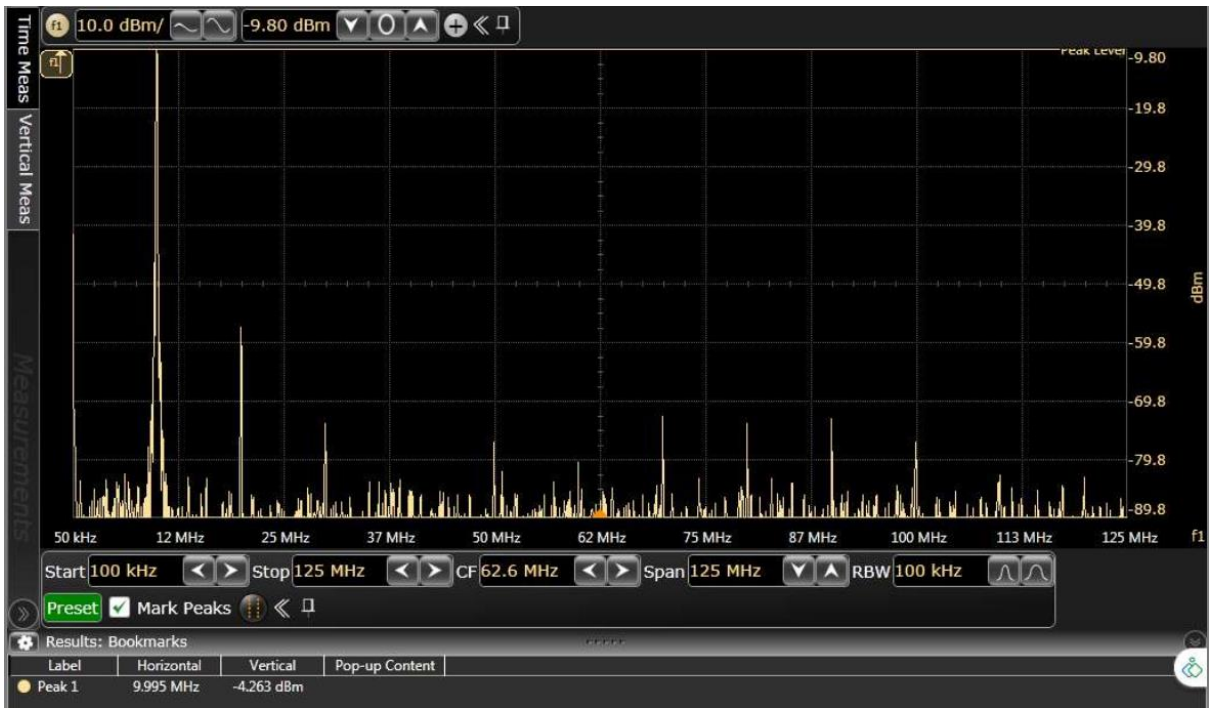


Figure 49.TC1: Frequency domain 10 MHz output waveform for x2 interpolation, LMF = 442 mode

7.4.2.2 Input Frequency = 20MHz

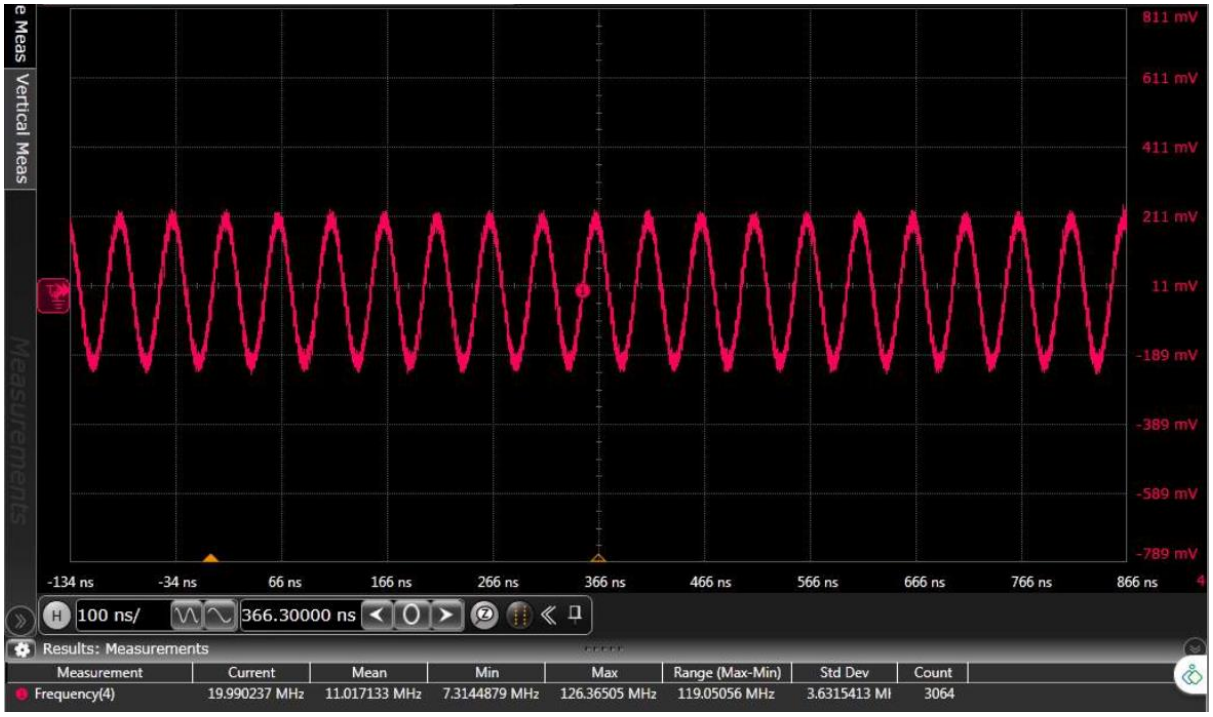


Figure 50.TC1: Time domain 20 MHz output waveform for x2 interpolation, LMF = 442 mode

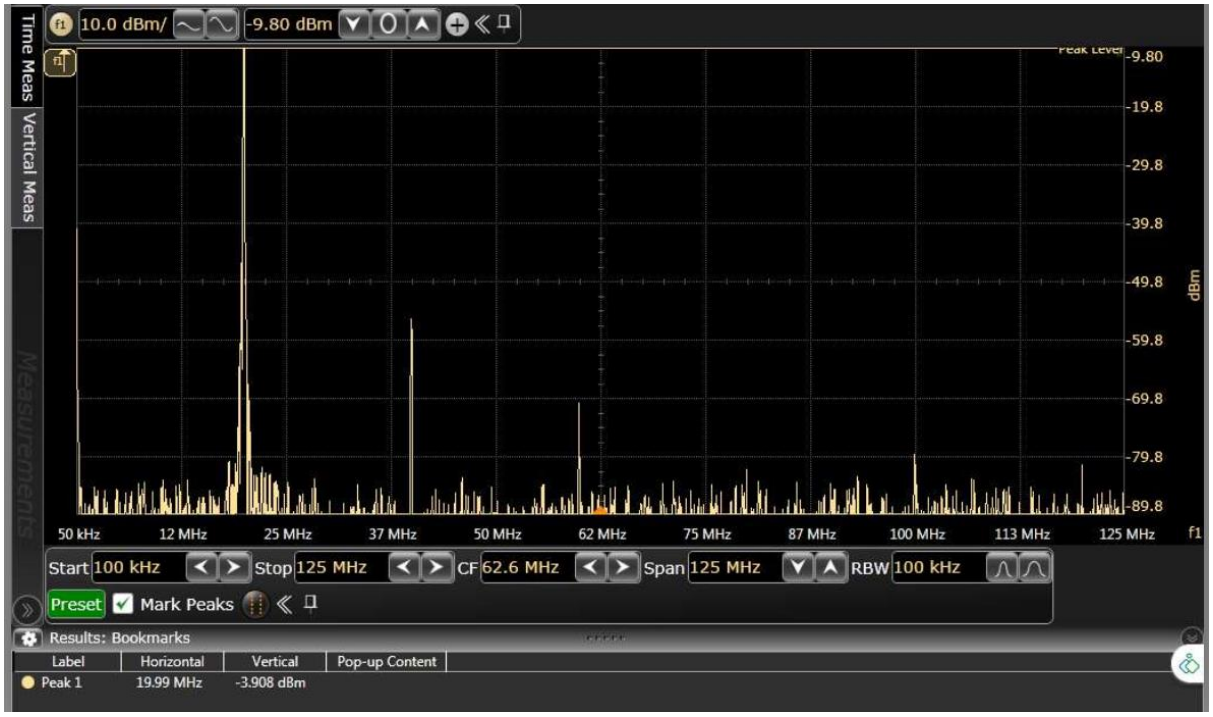


Figure 51.TC1 : Frequency domain 20 MHz output waveform for x2 interpolation, LMF = 442 mode

7.4.2.3 Input Frequency = 120MHz

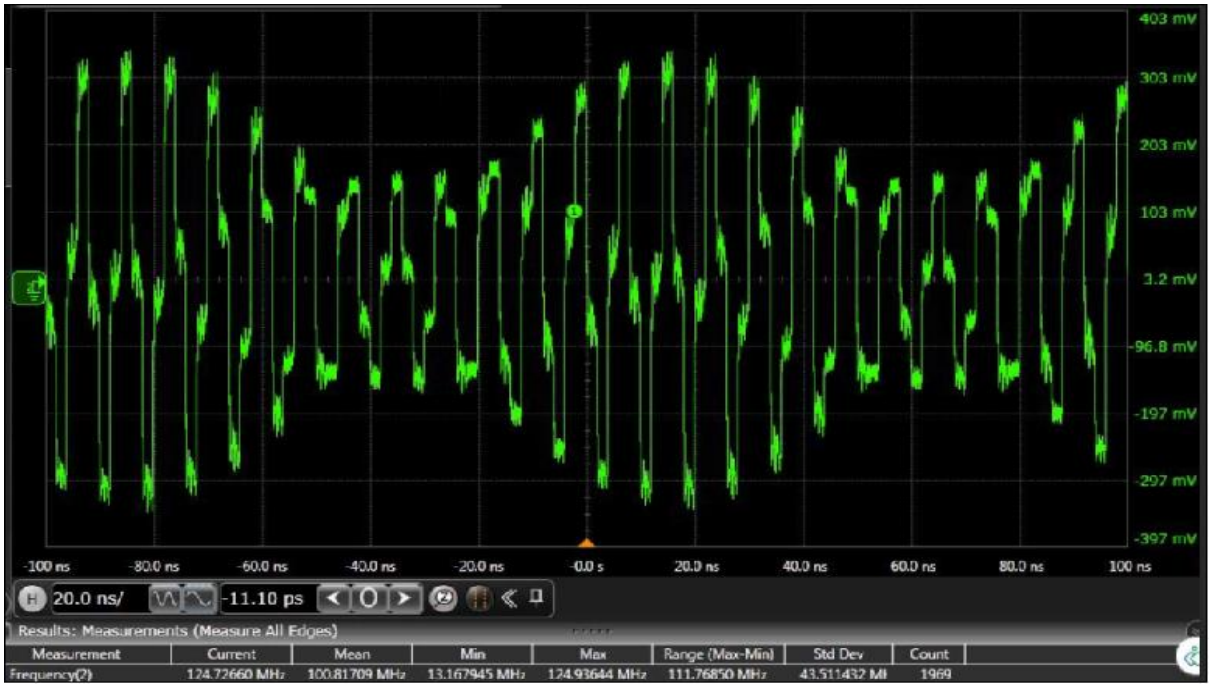


Figure 52.TC1: Time domain 120 MHz output waveform for x2 interpolation, LMF = 442 mode

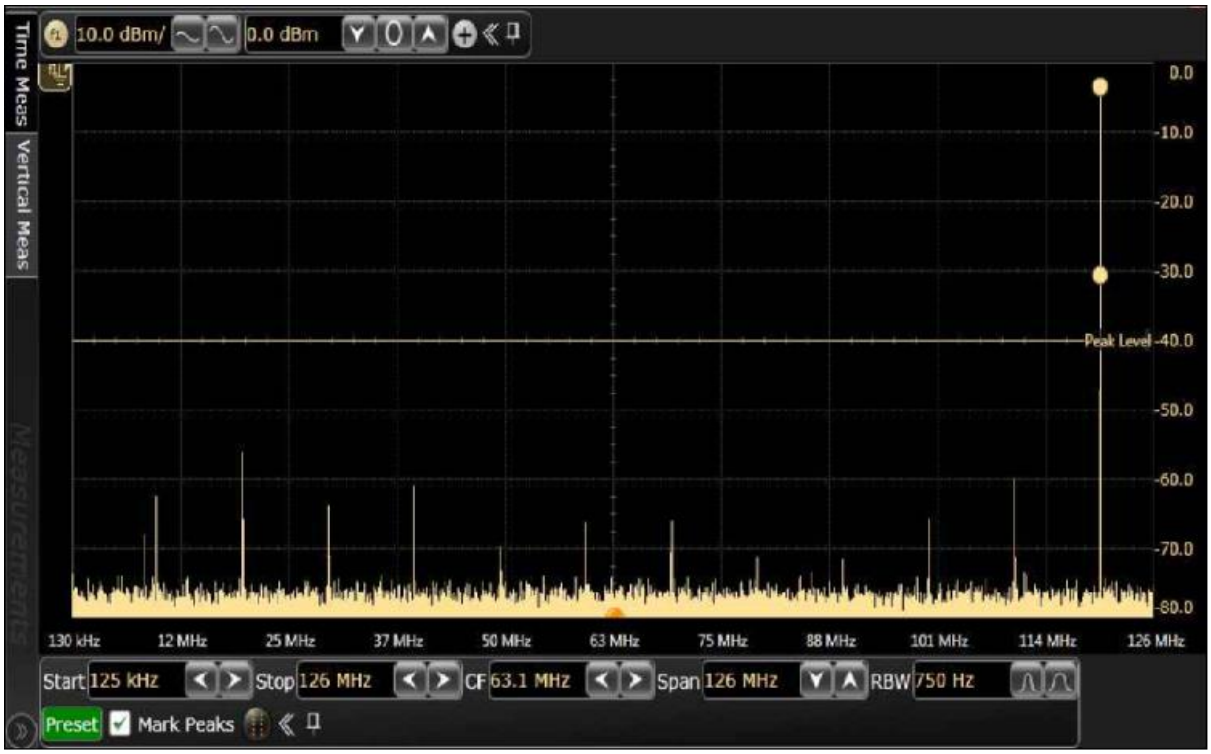


Figure 53.TC1: Frequency domain 120 MHz output waveform for x2 interpolation, LMF = 442 mode

7.4.3 Test Case 2 : LMF = 442, x4 interpolation

7.4.3.1 Input Frequency = 10MHz

Figure 54.TC2 : Time domain 10 MHz output waveform for x4 interpolation, LMF = 442 mode

7.4.3.2 Input Frequency = 20MHz

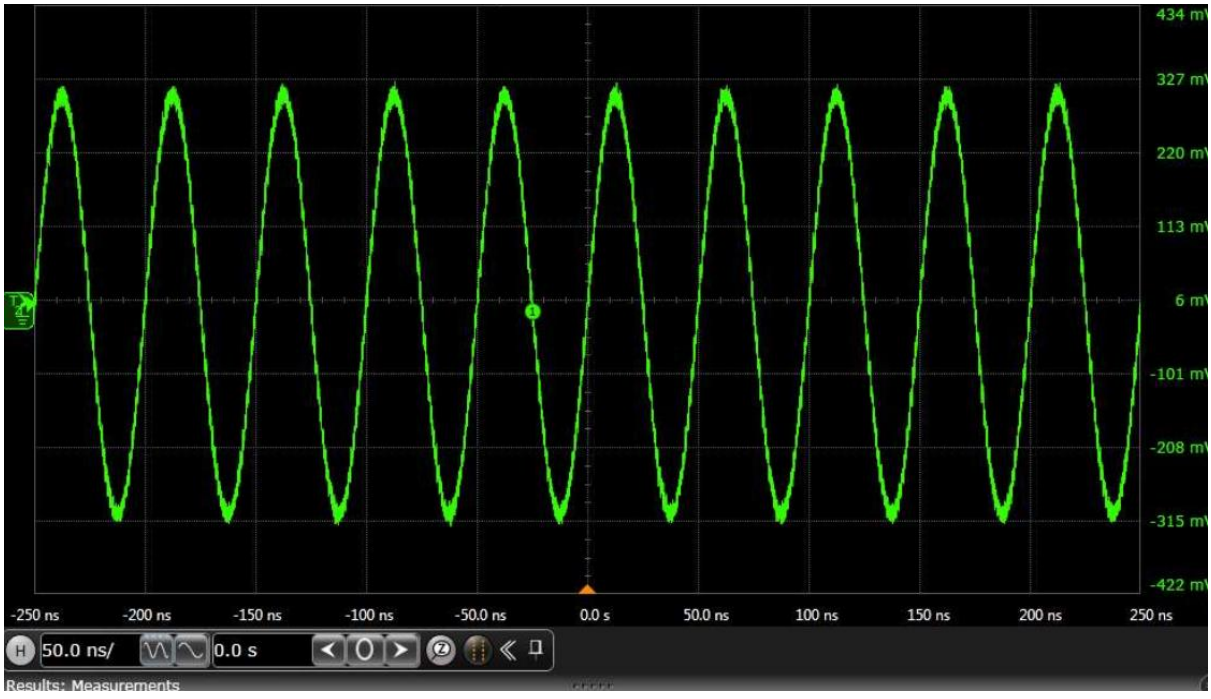


Figure 55.TC2 : Time domain 20 MHz output waveform for x4 interpolation, LMF = 442 mode

7.4.3.3 Input Frequency = 120MHz

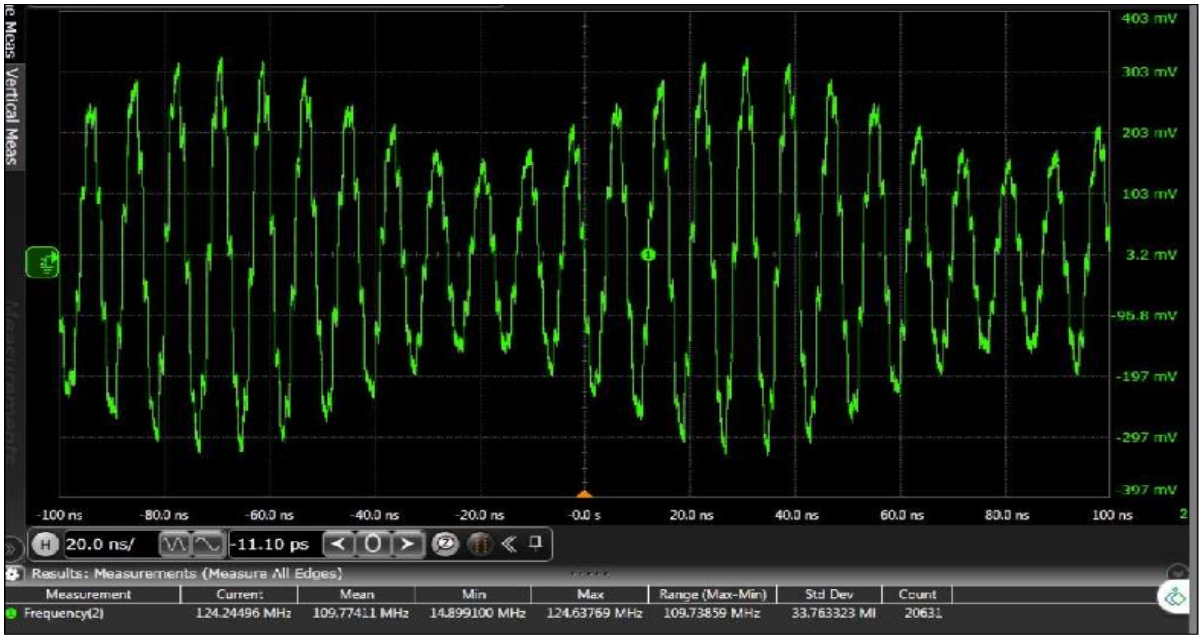


Figure 56.TC2: Time domain 120 MHz output waveform for x4 interpolation, LMF = 442 mode

Figure 57.TC2: Frequency domain 120 MHz output waveform for x4 interpolation, LMF = 442 mode

7.4.4 Test Case 3 : LMF = 244, x2 interpolation

7.4.4.1 Input Frequency = 10MHz

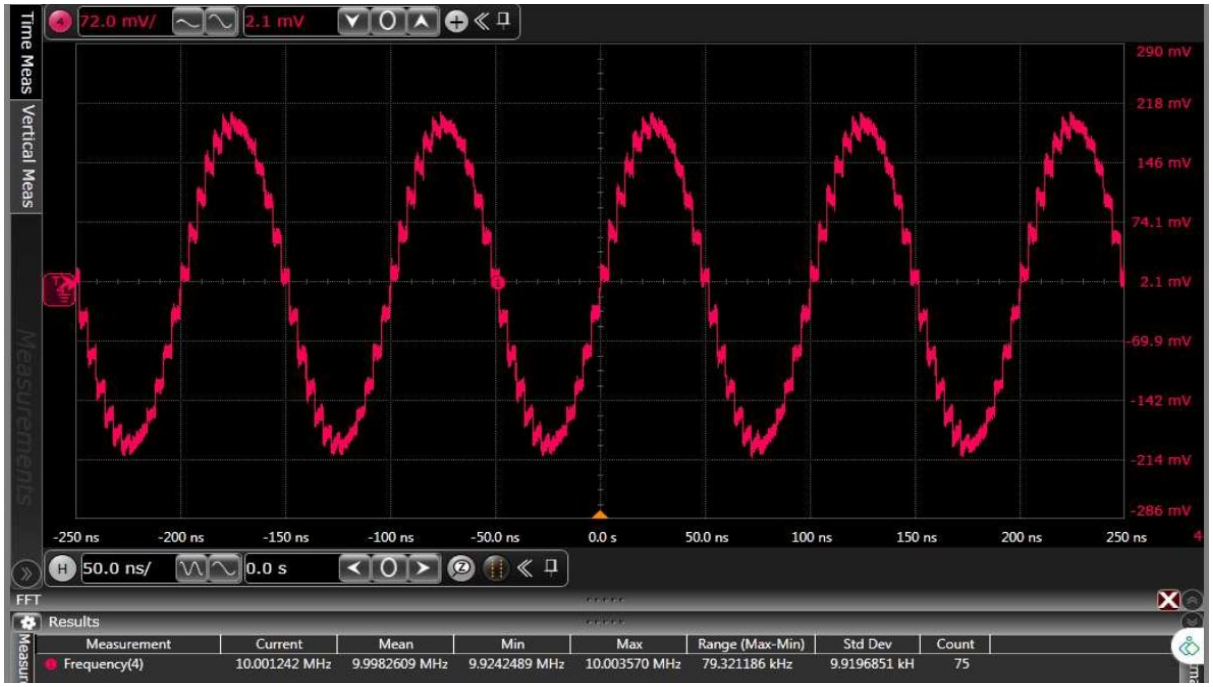


Figure 58.TC3: Time domain 10 MHz output waveform for x2 interpolation, LMF = 244 mode

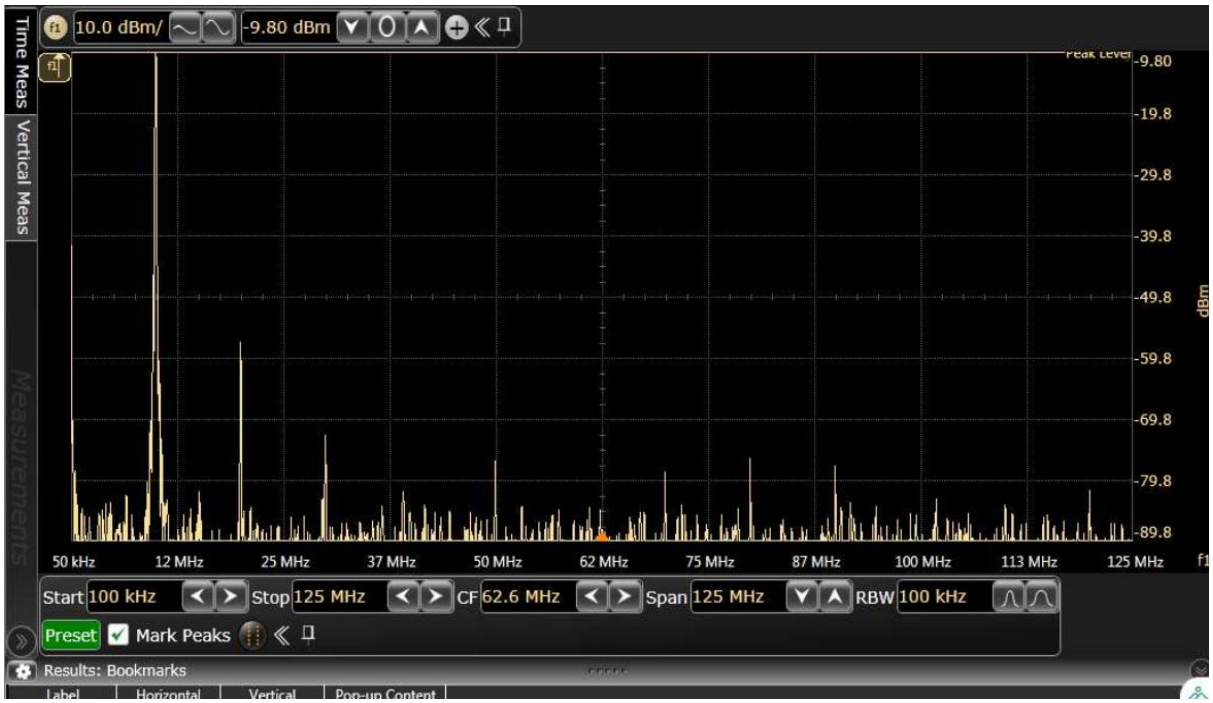


Figure 59.TC3: Frequency domain 10 MHz output waveform for x2 interpolation, LMF = 244 mode

7.4.4.2 Input Frequency = 20MHz

Figure 60.TC3: Time domain 20 MHz output waveform for x2 interpolation, LMF = 244 mode

Figure 61.TC3: Frequency domain 20 MHz output waveform for x2 interpolation, LMF = 244 mode

7.4.5 Test Case 4 : LMF = 244, x4 interpolation

7.4.5.1 Input Frequency = 10MHz

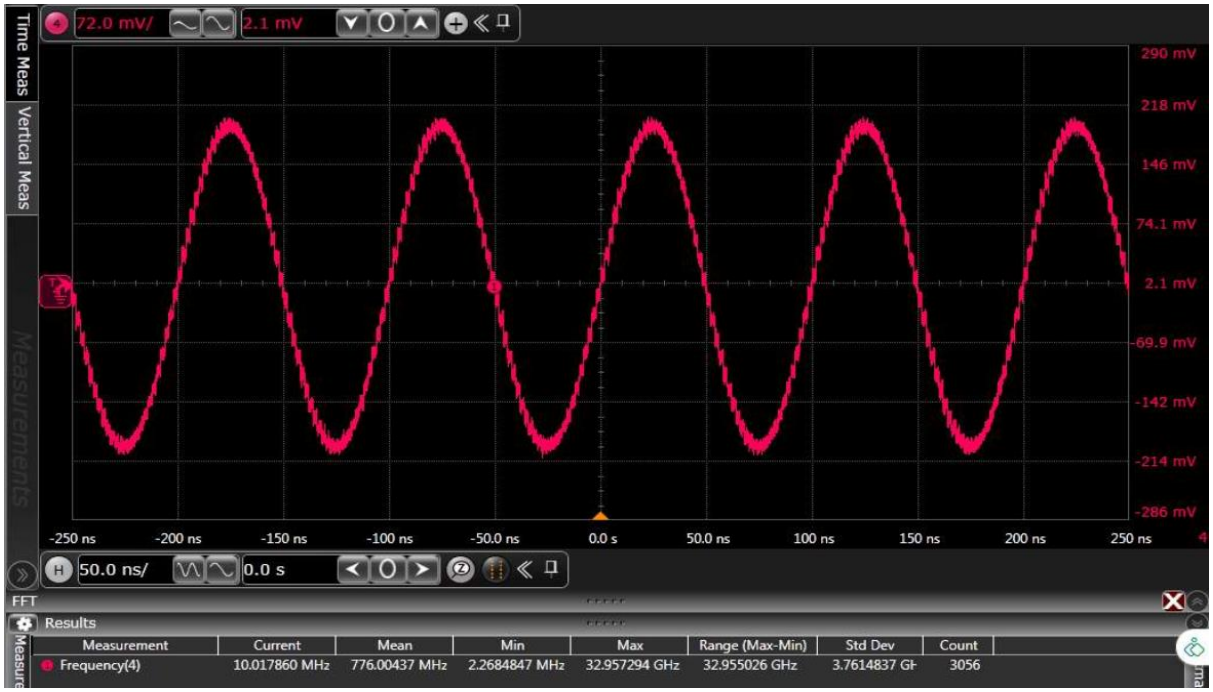


Figure 62.TC4: Time domain 10 MHz output waveform for x4 interpolation, LMF = 244 mode

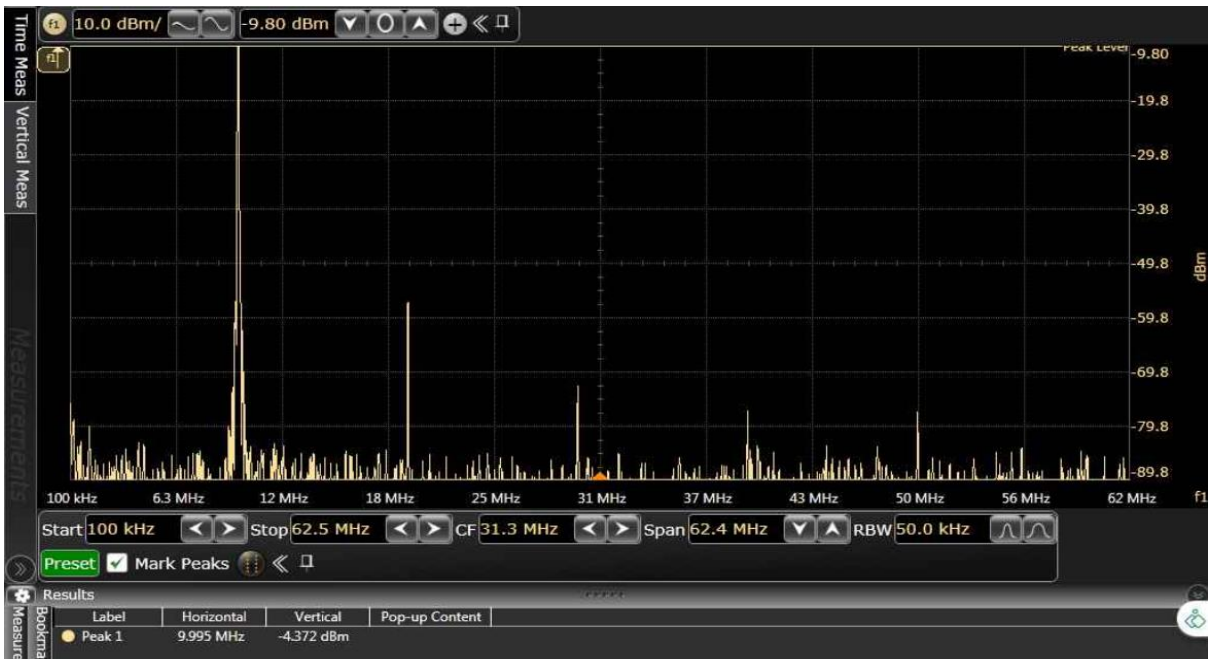


Figure 63.TC4 : Frequency domain 10 MHz output waveform for x4 interpolation, LMF = 244 mode

7.4.5.2 Input Frequency = 20MHz

Figure 64. TC4 : Time domain 20 MHz output waveform for x4 interpolation, LMF = 244 mode

Figure 65.TC4 : Time domain 20 MHz output waveform for x4 interpolation, LMF = 244 mode

7.4.6 Test Case 5 : LMF = 244, x8 interpolation

7.4.6.1 Input Frequency = 10MHz

Figure 66.TC5: Time domain 10 MHz output waveform for x8 interpolation, LMF = 244 mode

7.4.6.2 Input Frequency = 20MHz

Figure 67. TC5: Time domain 20 MHz output waveform for x8 interpolation, LMF = 244 mode

7.5 Test Cases for 12.5Gbps

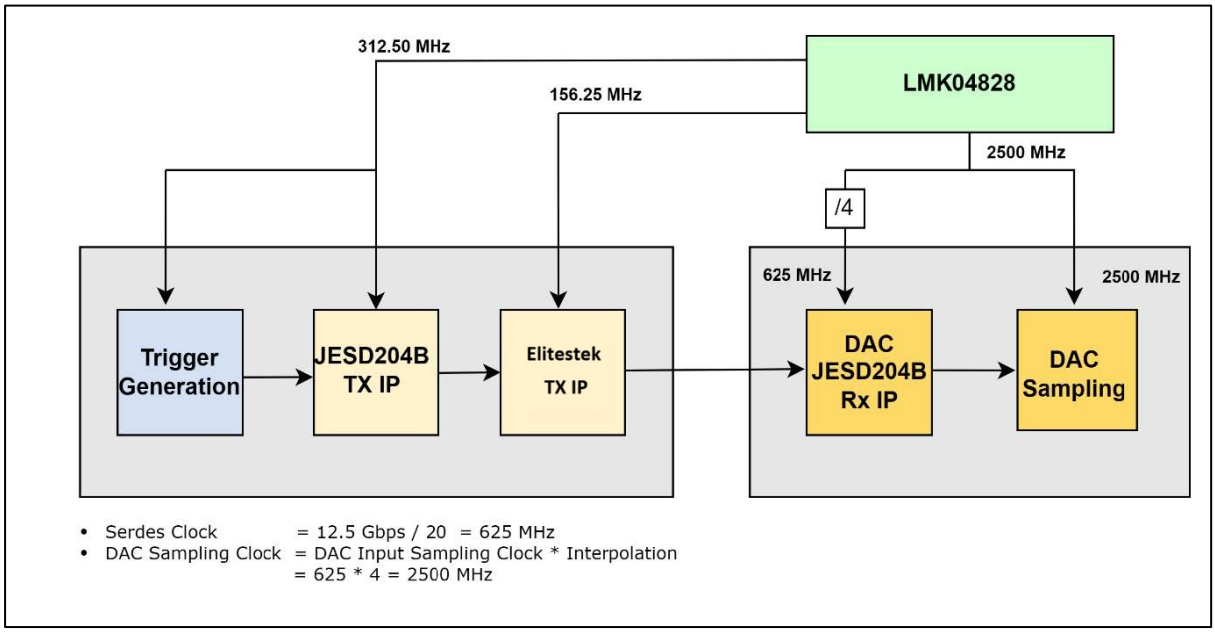


Figure 68: Block Diagram depicting Clocking Architecture for 12.5 Gbps

SerDes Clock = SerDes Rate / SerDes Data Width

Chipset	SerDes Rate	SerDes Data width (Resolution after 8b10b)	SerDes Clock
LFT JESD204B TX (Elitestek FPGA)	12.5 Gbps	40 bits	312.5 MHz
TI DAC38J84	12.5 Gbps	20 bits	625 MHz

Table 33. Elitestek Eval board and DAC Data rate Table

- Serdes Rate = 12.5 Gbps
- FPGA JESD204B Clock = 312.5 MHz
- FPGA Reference Clock = 156.25 MHz
- FPGA Sysref = 4.88 MHz
- DAC Clock = 625 MHz

- DAC Sysref = 4.88 MHz
- No. Of Frames per MultiFrame (K) =32

DAC Input sampling rate = SerDes Rate / (DAC Resolution after 8b10b * No of converters in a single lane)

DAC Output sampling rate = DAC Input sampling rate * Interpolation Factor

The following are the different modes of testing done for DAC:

Test Case	Modes (LMF)	Interpolation	No. of converters in single-lane	DAC Input Sampling Rate (MSPS)	DAC Output Sampling Rate (MSPS)	LMK Sysref	PLL2 Input Frequency (MHz)
0	442	x1	1	625.00	625.00	Continuous	100.00
1	442	x2	1	625.00	1250.00	Continuous	100.00
2	442	x4	1	625.00	2500.00	Continuous	100.00
3	244	x2	2	312.50	625.00	Continuous	100.00
4	244	x4	2	312.50	1250.00	Continuous	100.00
5	244	x8	2	312.50	2500.00	Continuous	100.00
Deterministic Latency Testing							
6	442	x4	1	625.00	2500.00	Continuous	100.00
Multiple Reset testing							
7	442	x4	1	625.00	2500.00	Continuous	100.00

Table 34: 12.5 Gbps Test Cases

7.5.1 Test Case 0 : LMF = 442, x1 interpolation

7.5.1.1 Input Frequency = 25MHz

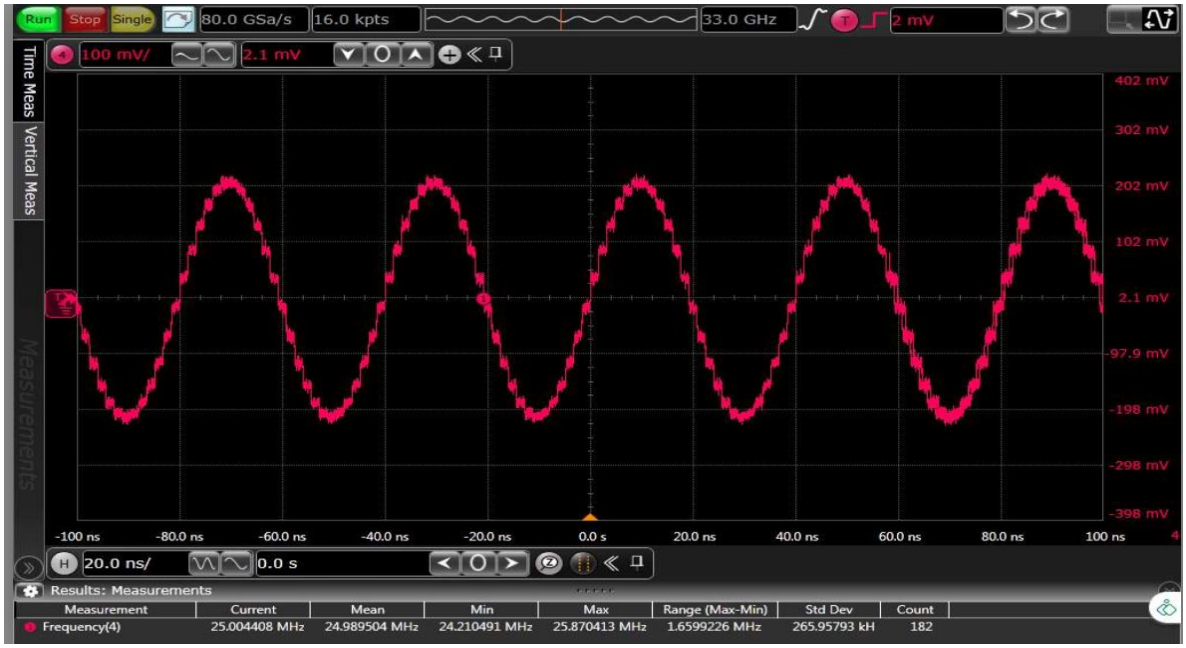


Figure 69:TC0: Time domain 25 MHz output waveform for x1 interpolation, LMF = 442 mode

7.5.1.2 Input Frequency = 75MHz

Figure 70. :TC0: Time domain 75 MHz output waveform for x1 interpolation, LMF = 442 mode

7.5.2 Test Case 1 : LMF = 442, x2 interpolation

7.5.2.1 Input Frequency = 25MHz

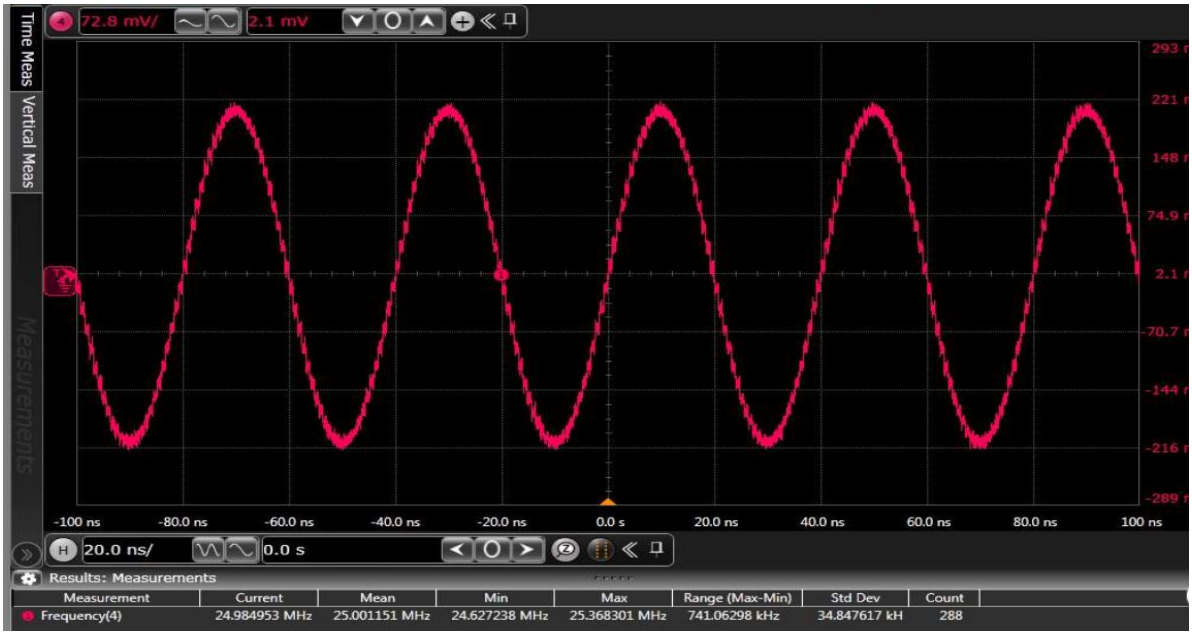


Figure 71. :TC1: Time domain 25 MHz output waveform for x2 interpolation, LMF = 442 mode

7.5.2.2 Input Frequency = 75MHz

Figure 72. :TC1: Time domain 75 MHz output waveform for x2 interpolation, LMF = 442 mode

7.5.3 Test Case 2 : LMF = 442, x4 interpolation

7.5.3.1 Input Frequency = 25MHz

Figure 73. :TC2: Time domain 25 MHz output waveform for x4 interpolation, LMF = 442 mode

7.5.3.2 Input Frequency = 75MHz

Figure 74:TC2: Time domain 75 MHz output waveform for x4 interpolation, LMF = 442 mode

7.5.3.3 Input Frequency = 250 MHz

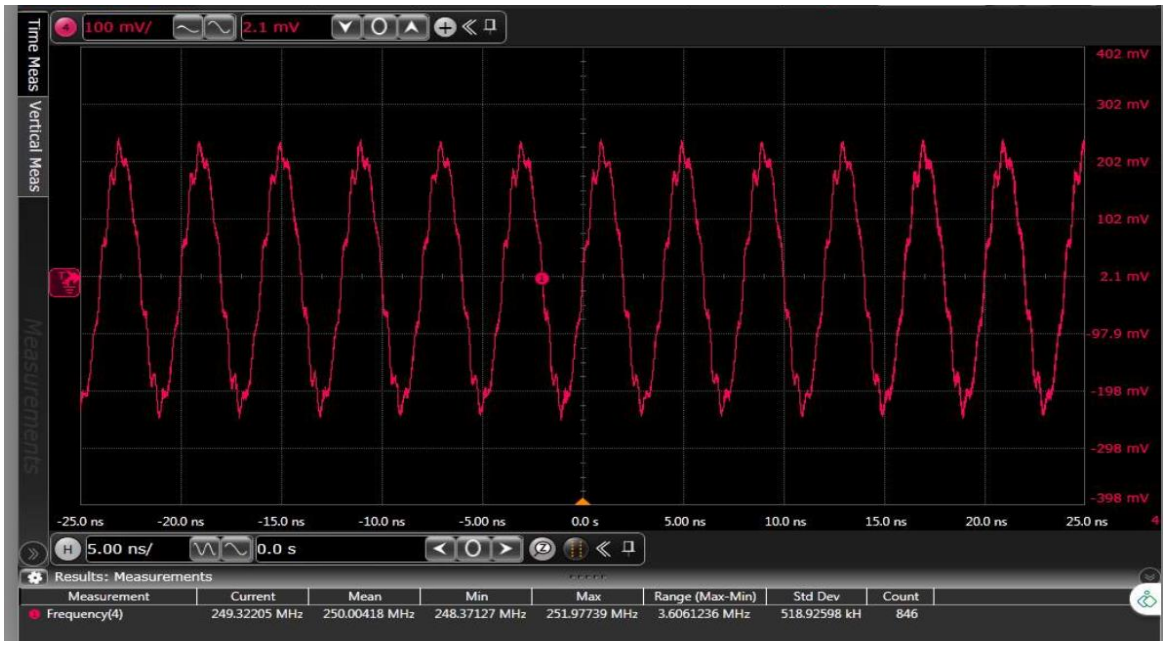


Figure 75:TC2: Time domain 250 MHz output waveform for x4 interpolation, LMF = 442 mode

7.5.3.4 Input Frequency = 310 MHz

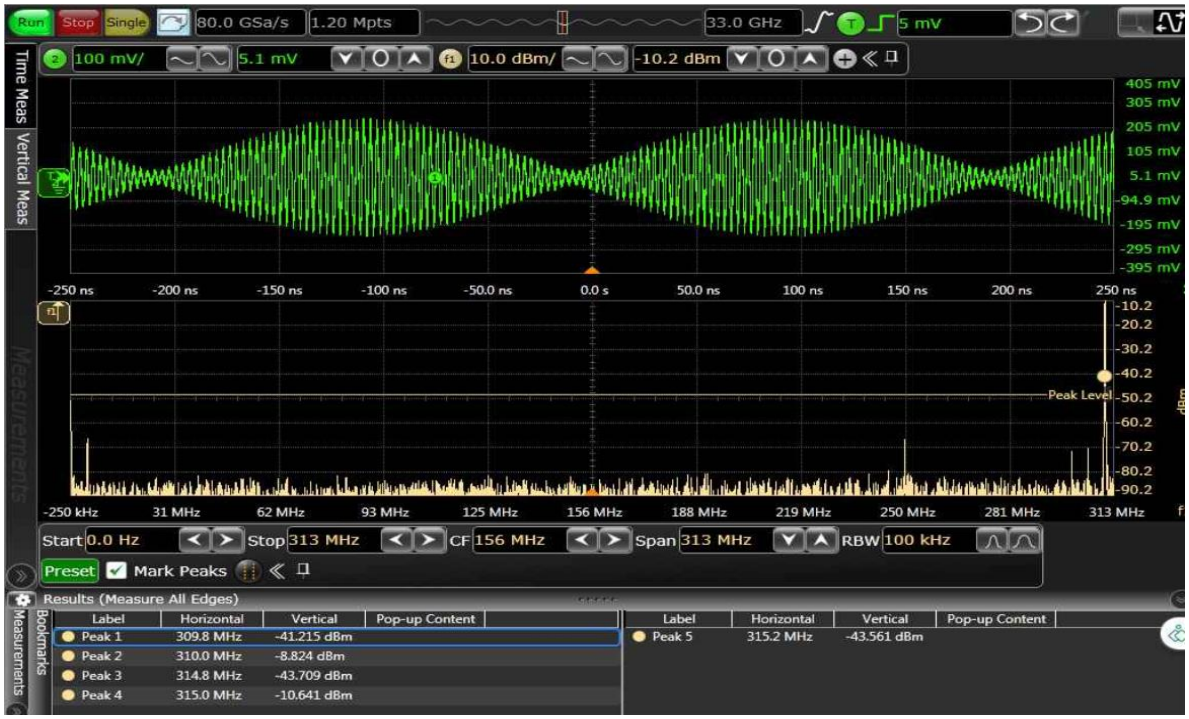


Figure 76:TC2: Time domain & Frequency Domain 310 MHz output waveform for x4 interpolation, LMF = 442 mode

7.5.4 Test Case 3 : LMF = 244, x2 interpolation

7.5.4.1 Input Frequency = 25MHz

Figure 77:TC3: Time domain 25 MHz output waveform for x2 interpolation, LMF = 244 mode

7.5.4.2 Input Frequency = 50MHz

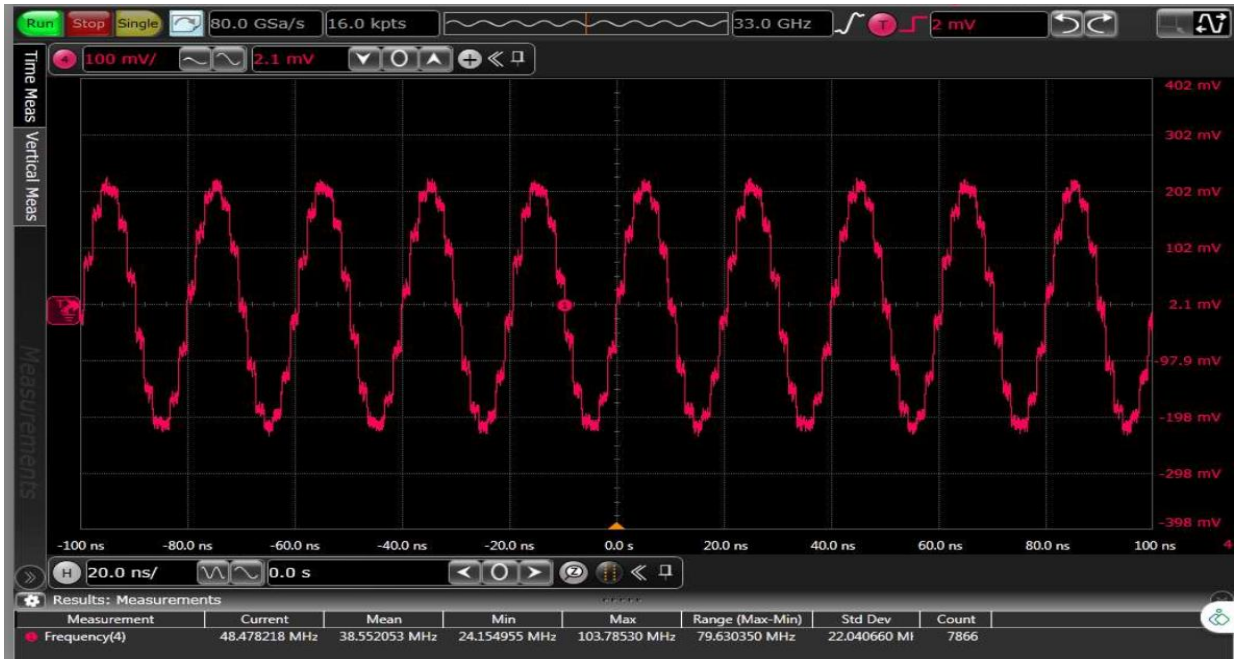


Figure 78:TC3: Time domain 50 MHz output waveform for x2 interpolation, LMF = 244 mode

7.5.5 Test Case 4 : LMF = 244, x4 interpolation

7.5.5.1 Input Frequency = 25MHz

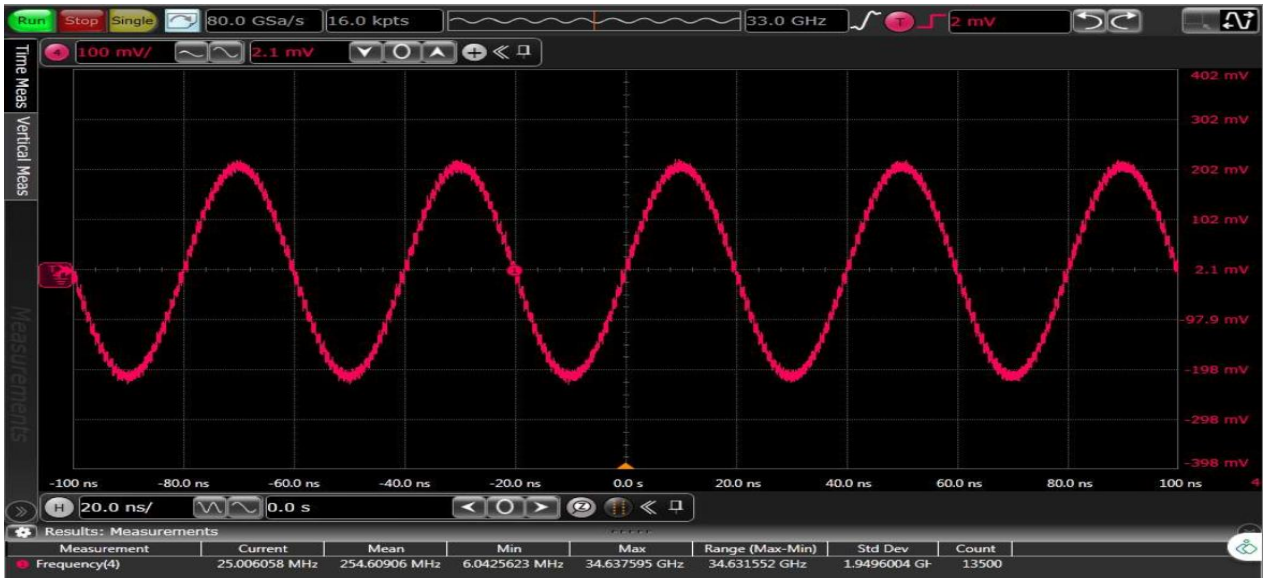


Figure 79: TC4: Time domain 25 MHz output waveform for x4 interpolation, LMF = 244 mode

7.5.5.2 Input Frequency = 50MHz

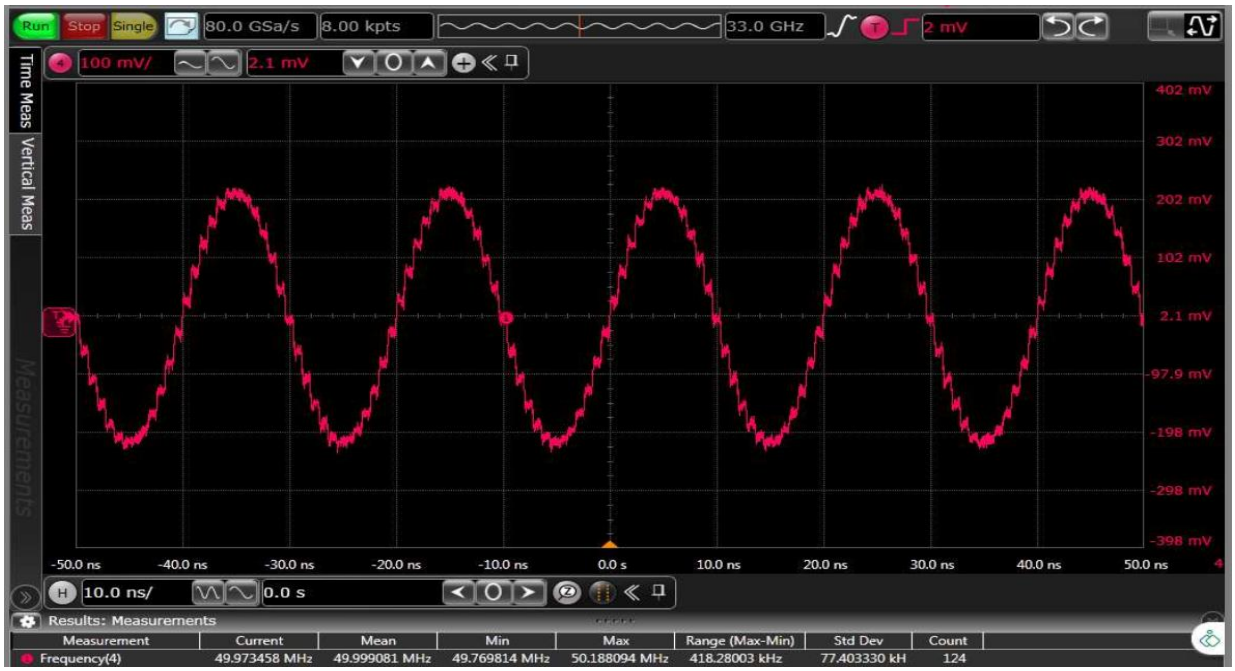


Figure 80: TC4: Time domain 50 MHz output waveform for x4 interpolation, LMF = 244 mode

7.5.6 Test Case 5 : LMF = 244, x8 interpolation

7.5.6.1 Input Frequency = 25MHz

Figure 81: TC5: Time domain 25 MHz output waveform for x8 interpolation, LMF = 244 mode

7.5.6.2 Input Frequency = 50MHz

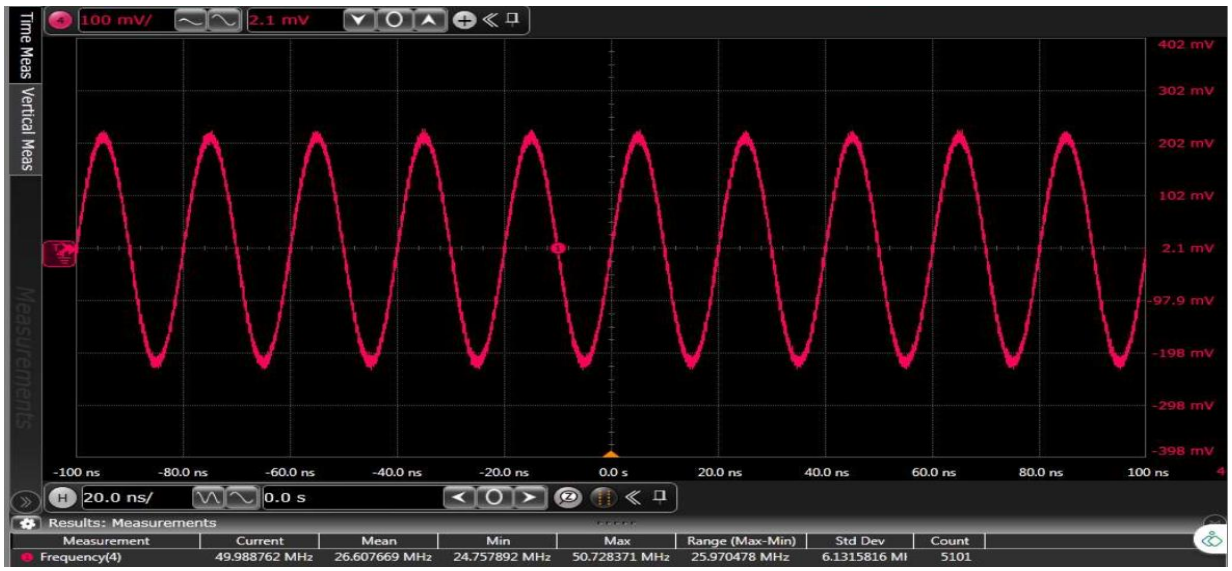


Figure 82: TC5: Time domain 50 MHz output waveform for x8 interpolation, LMF = 244 mode

7.6 DAC Mode Description

7.6.1 Mode = LMF = 442

Lanes	Lane Mapping			
Lane 0	DA0[15:8]	DA0[7:0]	DA1[15:8]	DA1[7:0]
Lane 1	DB0[15:8]	DB0[7:0]	DB1[15:8]	DB1[7:0]
Lane 2	DC0[15:8]	DC0[7:0]	DC1[15:8]	DC1[7:0]
Lane 3	DD0[15:8]	DD0[7:0]	DD1[15:8]	DD1[7:0]

Table 35. DAC Lane Mapping for LMF = 442

Note: Here, A, B, C, and D are the four converters in DAC. The Data from each converter are sent individually among the four lanes.

Parameter	Value	
Number of lanes	4	4
DAC SerDes Rate	5 Gbps	12.5 Gbps
DAC Resolution	20 bits	20 bits
No. of converters in single lane	1	1
DAC Input sampling rate	5/ (20*1) = 250MSPS	12.5/ (20*1) = 625 MSPS
DAC Output sampling rate for x1 interpolation	250MSPS*1 = 250MSPS	625 MSPS*1 =625 MSPS
DAC Output sampling rate for x2 interpolation	250MSPS*2 = 500MSPS	625 MSPS*2 = 1250 MSPS
DAC Output sampling rate for x4 interpolation	250MSPS*4 = 1000MSPS	625 MSPS*4 = 2500 MSPS

Table 36.DAC Parameter Values for LMF = 442

7.6.2 Mode = LMF = 244

Lanes	Lane Mapping			
Lane 0	DA0[15:8]	DA0[7:0]	DB0[15:8]	DB0[7:0]
Lane 1	DC0[15:8]	DC0[7:0]	DD0[15:8]	DD0[7:0]

Table 37. DAC Lane Mapping for LMF = 244

Note: The Data from two converters are sent across two lanes.

Table 38. DAC Parameter Values for LMF = 244

Parameter	Value	
Number of lanes	2	4
DAC SerDes Rate	5 Gbps	12.5 Gbps
DAC Resolution	20 bits	20 bits
No. of converters in single lane	2	2
DAC Input sampling rate	5/ (20*2) = 125MSPS	12.5/ (20*2) = 312.5 MSPS
DAC Output sampling rate for x2 interpolation	125MSPS*2 = 250MSPS	312.5 MSPS*2 = 625 MSPS
DAC Output sampling rate for x4 interpolation	125MSPS*4 = 500MSPS	312.5 MSPS*4 = 1250 MSPS
DAC Output sampling rate for x8 interpolation	125MSPS*8 = 1000MSPS	312.5 MSPS*8 = 2500 MSPS

8 Deterministic Latency for JESD204B Transmitter with DAC

8.1 Hardware Validation Block diagram for Deterministic Latency testing with DAC

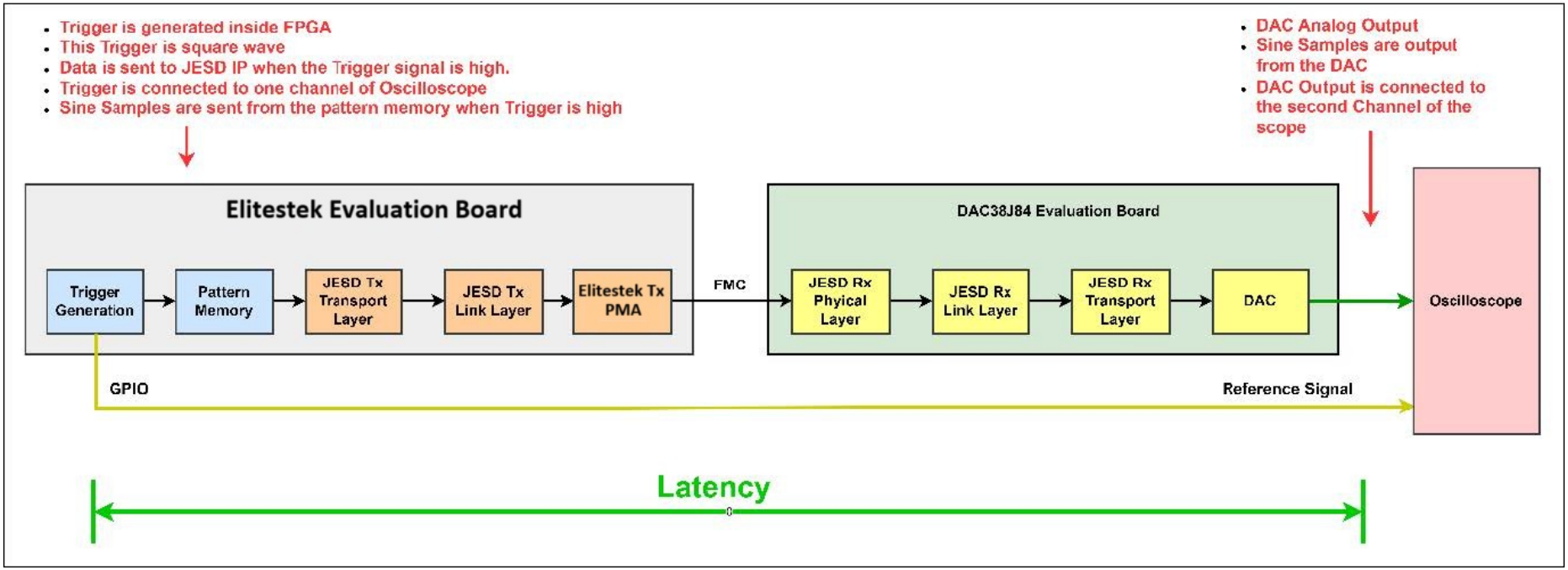


Figure 83. Deterministic Latency testing of JESD204B Transmitter with DAC

- The trigger signal is generated inside the FPGA in terms of a square wave, which is used as the reference signal for checking the deterministic latency
- When the trigger signal is high, the sine samples are transmitted from the FPGA to the DAC
- The deterministic latency is determined from the start of the trigger signal to the start of the DAC output sine wave.

8.2 Test Setup of Elitestek Evaluation Board with DAC for Deterministic Latency

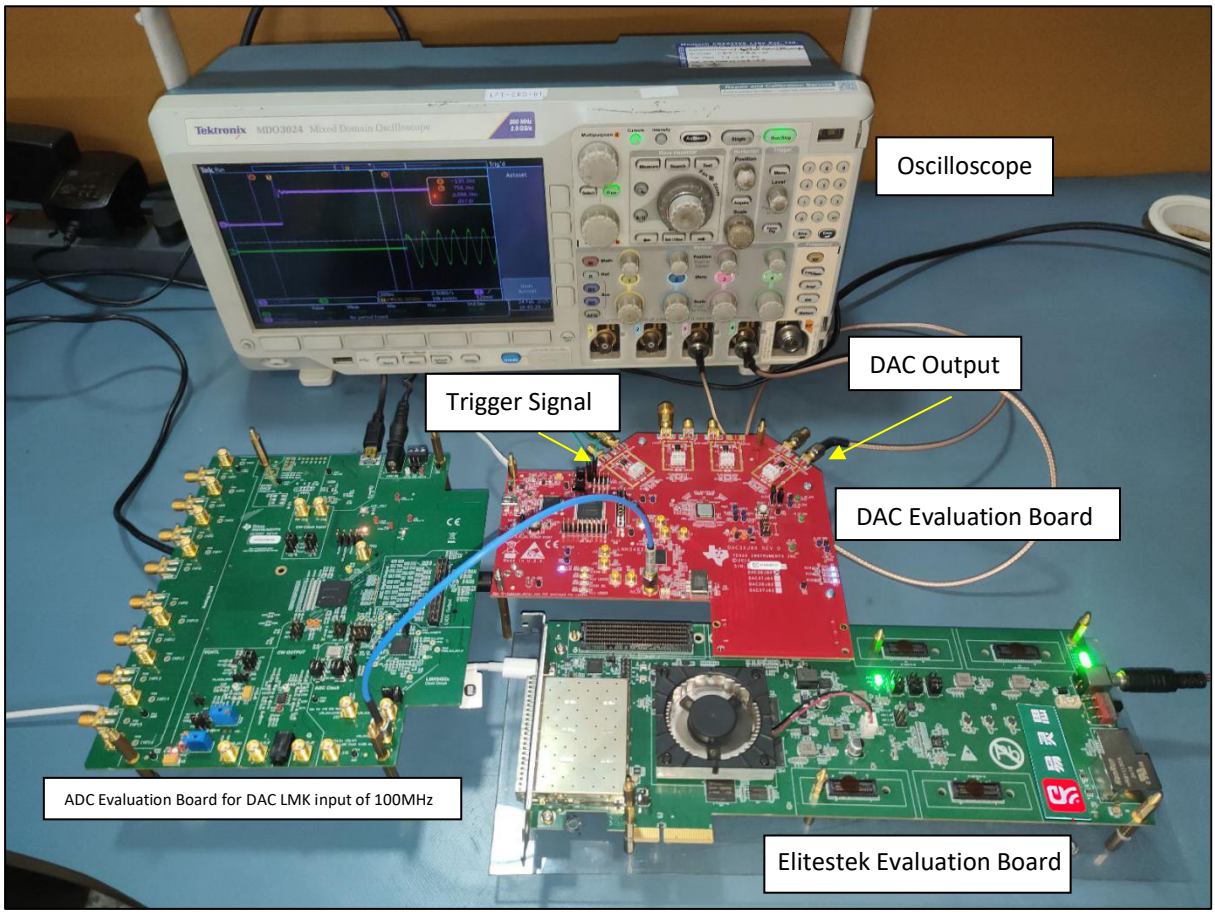


Figure 84.Test set up of Elitestek Evaluation Board with DAC for testing Deterministic Latency with external clock

- The Trigger signal from the DAC is connected to one channel of CRO and the DAC output is connected to another channel.
- The 100Mhz input to the DAC LMK is fed from the ADC LMK output.

The block diagram below explains the clocking structure for JESD204B Transmitter testing with DAC evaluation Board

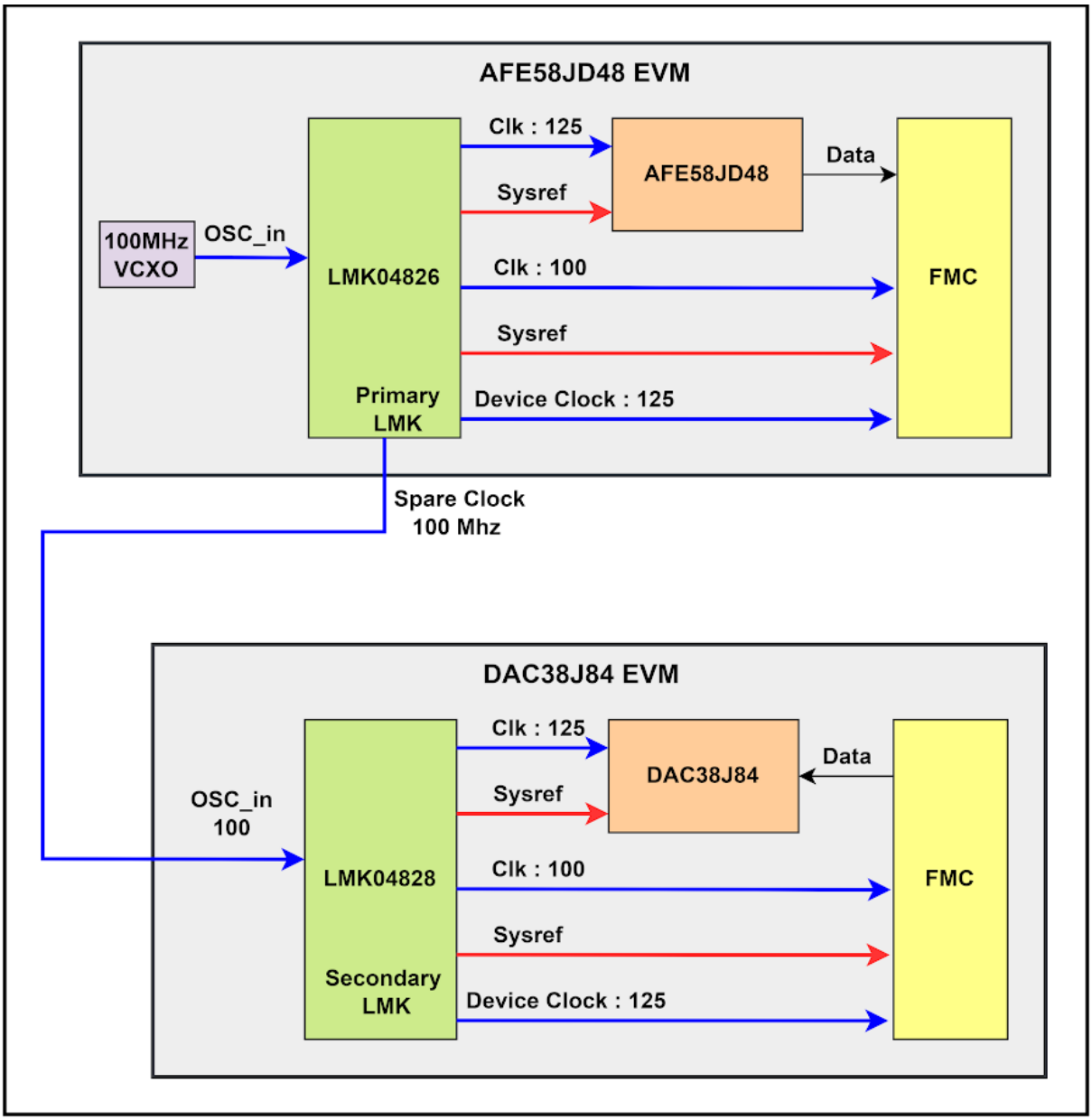


Figure 85.Clocking Structure for JESD204B Transmitter testing with DAC at 5 Gbps Line Rate (Here the oscillator input to the DAC LMK is ADC LMK clock output)

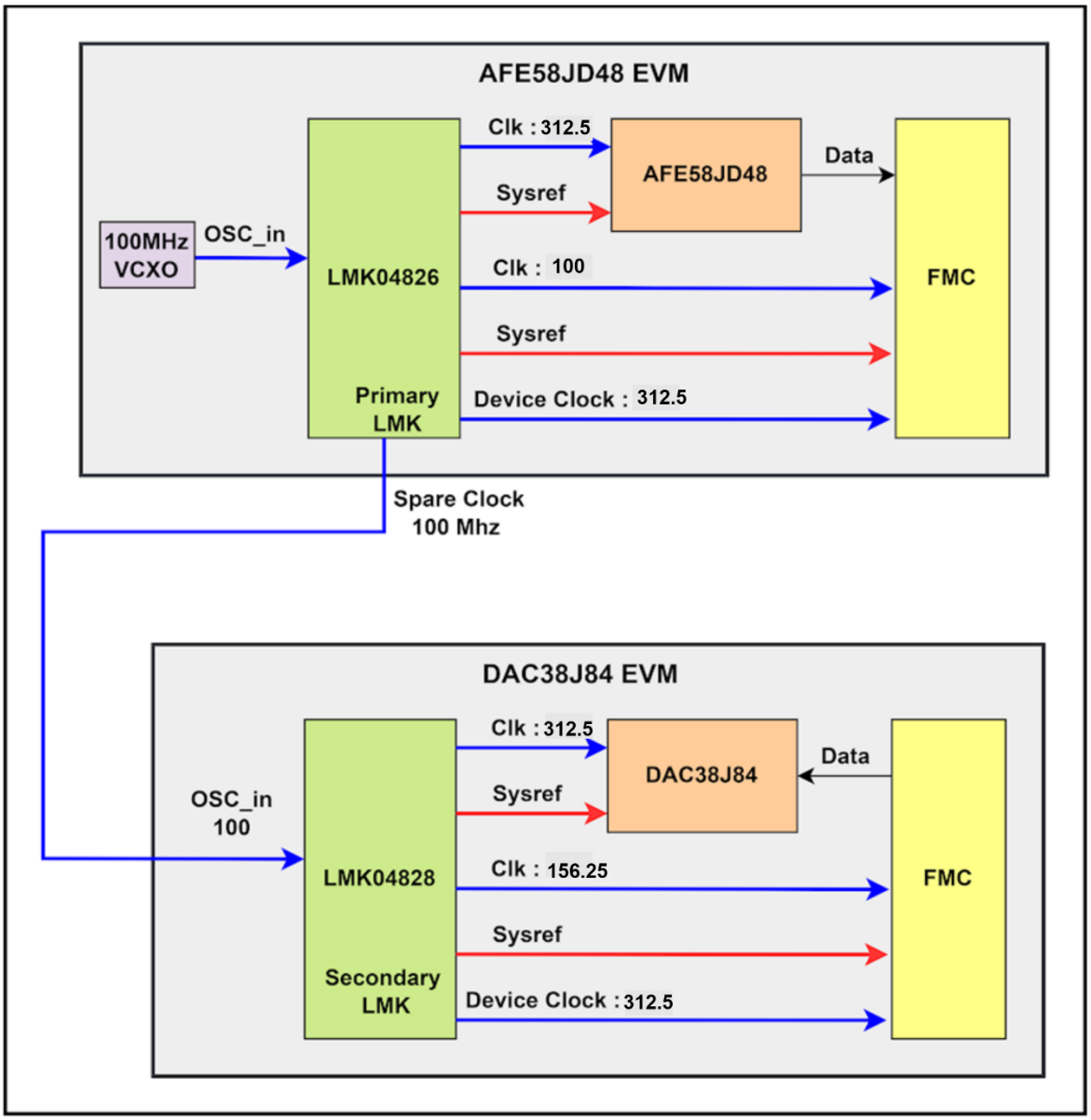


Figure 86: Clocking Structure for JESD204B Transmitter testing with DAC at 12.5 Gbps Line Rate (Here the oscillator input to the DAC LMK is ADC LMK clock output)

Note: Refer to sections 6.2.2 and 6.3.3 for the Hardware Test Equipment and Software used

8.3 Test Procedure

Note: The procedure to execute the test case for Deterministic Latency testing is the same as discussed in Section 6.3.

For Deterministic Latency testing, the trigger condition in the oscilloscope must be set up.

8.4 Test Cases

The 6th Test case mentioned in section 7.4 and Section 7.5 is used to test the deterministic latency for 5 Gbps and 12.5 Gbps respectively.

8.4.1 LMF = 442, x4 interpolation (5 Gbps Deterministic Latency)

8.4.1.1 Input Frequency = 10Mhz

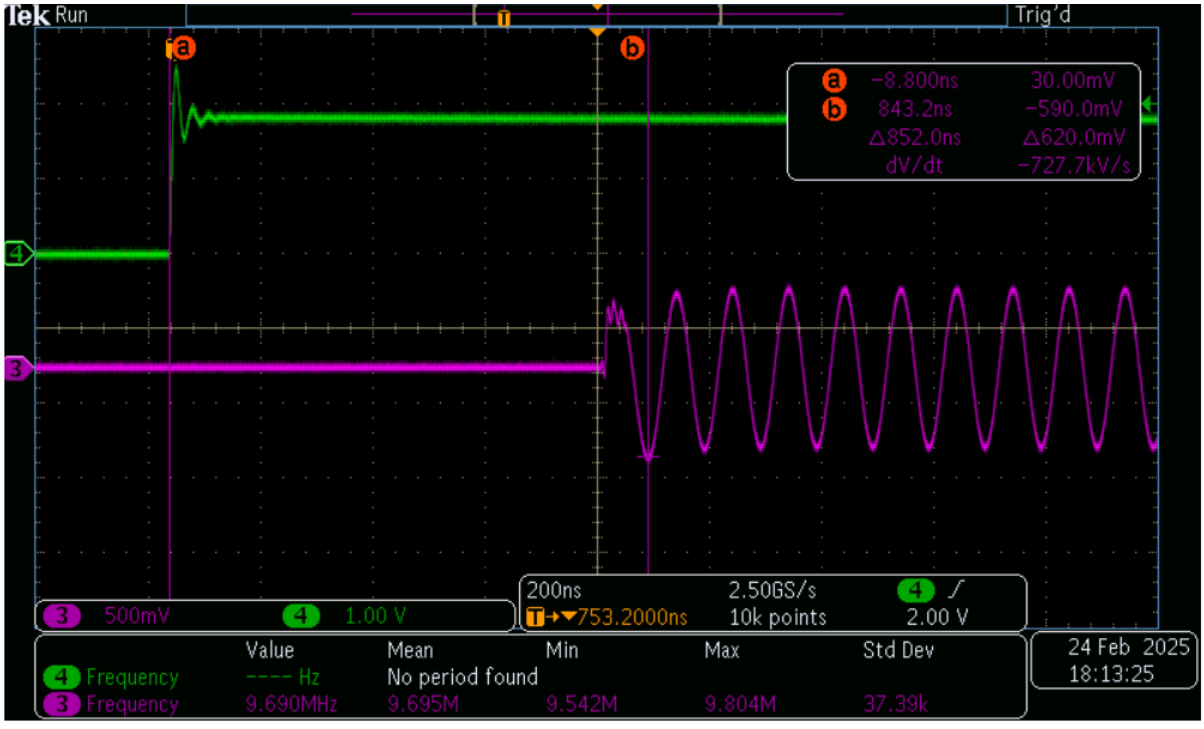


Figure 87.Deterministic Latency capture between trigger signal and DAC output at input frequency of 10MHz

The green color waveform is the trigger and pink color waveform is the DAC output at 10MHz input frequency captured for data rate 5Gbps at LMF = 442 with x4 interpolation

Deterministic latency in the path is in range of 850.00 ns with variation of 150ps on every power cycle.

Reset Type	Mode (LMF)	Interpolation	Min Value (ns)	Typical Value (ns)	Max Value (ns)	No. of Iterations	Variation (ps)
Cold	442	x4	852.00	852.00	852.15	30	150
Warm	442	x4	852.00	852.00	852.10	30	100

Table 39: Deterministic latency variation table for JESD204B TX testing with DAC for 5Gbps

8.4.2 LMF = 442, x4 interpolation (12.5 Gbps Deterministic Latency)

8.4.2.1 Input Frequency = 250 MHz

Figure 88.: Deterministic Latency capture between trigger signal and DAC output A at input frequency of 250MHz

The green color waveform is the trigger and pink color waveform is the DAC output A at 250MHz input frequency captured for data rate 12.5 Gbps at LMF = 442 with x4 interpolation

Deterministic latency in the path is in range of 317.00 ns with variation of 150ps on every power cycle

Reset Type	Mode (LMF)	Interpolation	Min Value (ns)	Typical Value (ns)	Max Value (ns)	No. of Iterations	Variation (ps)
Cold	442	X4	317.800	317.805	317.933	30	133
Warm	442	x4	317.800	317.805	317.947	30	147

Table 40: Deterministic latency variation table for JESD204B TX testing with DAC for 5Gbps

8.5 Deterministic latency variation with respect to Heat Sink on Elitestek Eval Board

8.5.1 Test on Board with Heat Sink

Figure 89: Deterministic Latency Delay of 327.17 ns with Heat Sink for input waveform of 75 MHz at 12.5 Gbps Line Rate

Deterministic Latency is around 327.17 ns for the FPGA Eval Board with Heat Sink attached. Green waveform represents the trigger to BRAM and pink waveform represent the DAC Output of 75 MHz.

8.5.2 Test on Board without Heat Sink

Figure 90: Deterministic Latency Delay of 327.17 ns without Heat Sink for input waveform of 75 MHz at 12.5 Gbps Line Rate

Deterministic Latency is around 327.17 ns here also for the FPGA Eval Board without Heat Sink attached. Green waveform represents the trigger to BRAM and pink waveform represent the DAC Output of 75 MHz

Hence, it can be concluded that Heat Sink does not have noticeable effect on Deterministic Latency when compared to FPGA Eval Board without Heat Sink .

Reset Type	Mode (LMF)	Interpolation	Min Value (ns)	Typical Value (ns)	Max Value (ns)	No. of Iterations	Variation (ps)
Cold	442	x4	327.095	327.177	327.242	30	0.147
Warm	442	x4	327.095	327.177	327.242	30	0.147

Table 41: Deterministic Latency variation at 12.5 Gbps for 75 MHz input to DAC

8.6 Deterministic latency variation with respect to different DAC Output Channels

FPGA Evaluation Board used for this test is without the Heat Sink. Input Waveform Frequency used is 250 MHz .

8.6.1 DAC Channel A

Figure 91: DAC Channel A output waveform at 12.5 Gbps Line Rate

Deterministic Latency is around 317.805 ns here for the FPGA Eval Board without Heat Sink attached. Green waveform represents the trigger to BRAM and pink waveform represent the DAC Output of 250 MHz .

For DAC Channel A , Minimum value of deterministic Latency Value comes out to be 317.800 ns and Maximum value being 317.933 ns, typical value being 317.805 ns. This results in a delay variation of 133 ps for DAC Channel A.

8.6.2 DAC Channel B

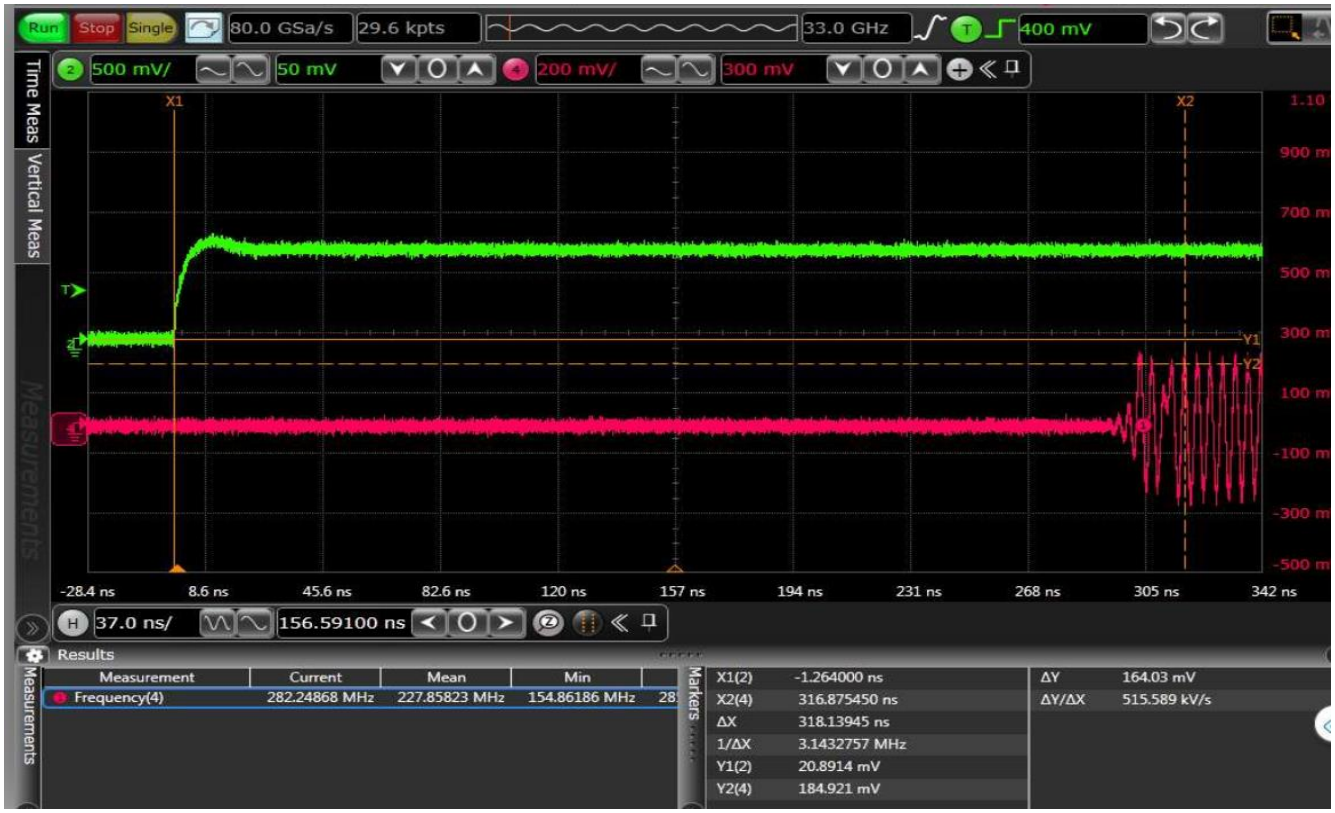


Figure 92: DAC Channel B output waveform at 12.5 Gbps Line Rate

Deterministic Latency is around 318.139ns here for the FPGA Eval Board without Heat Sink attached. Green waveform represents the trigger to BRAM and pink waveform represent the DAC Output of 250 MHz .

For DAC Channel B , Minimum value of deterministic Latency Value comes out to be 318.045 ns and Maximum value being 318.181 ns, typical value being 318.139 ns. This results in a delay variation of 136 ps for DAC Channel B.

8.6.3 DAC Channel C

Figure 93: DAC Channel C output waveform at 12.5 Gbps Line Rate

Deterministic Latency delay is around 318.005 ns here for the FPGA Eval Board without Heat Sink attached. Green waveform represents the trigger to BRAM and pink waveform represent the DAC Output of 250 MHz .

For DAC Channel C , Minimum value of deterministic Latency Value comes out to be 317.947 ns and Maximum value being 318.082 ns, typical value being 318.004 ns. This results in a delay variation of 135 ps for DAC Channel C.

8.6.4 DAC Channel D

Figure 94: DAC Channel D output waveform at 12.5 Gbps Line Rate

Deterministic Latency delay is around 318.005 ns here for the FPGA Eval Board without Heat Sink attached. Green waveform represents the trigger to BRAM and pink waveform represent the DAC Output of 250 MHz .

For DAC Channel D , the Minimum value of the deterministic Latency Value comes out to be 317.947 ns, the Maximum value being 318.005 ns, and the typical value being 318.080 ns. This results in a delay variation of 133 ps for DAC Channel D.

Mode (LMF)	Interpolation	DAC Channel	Min Value (ns)	Typical Value (ns)	Max Value (ns)	No. of Iterations	Variation (ps)
442	x4	A	317.800	317.805	317.933	30	133
442	x4	B	318.045	318.139	318.181	30	136
442	x4	C	317.947	318.004	318.082	30	135
442	x4	D	317.947	318.005	318.080	30	133

Table 42: Deterministic Latency variation on different DAC Channels (Cold Reset, 12.5 Gbps Line Rate)

9 Hardware Validation for JESD204B Receiver with ADC

9.1 Hardware Validation Block Diagram

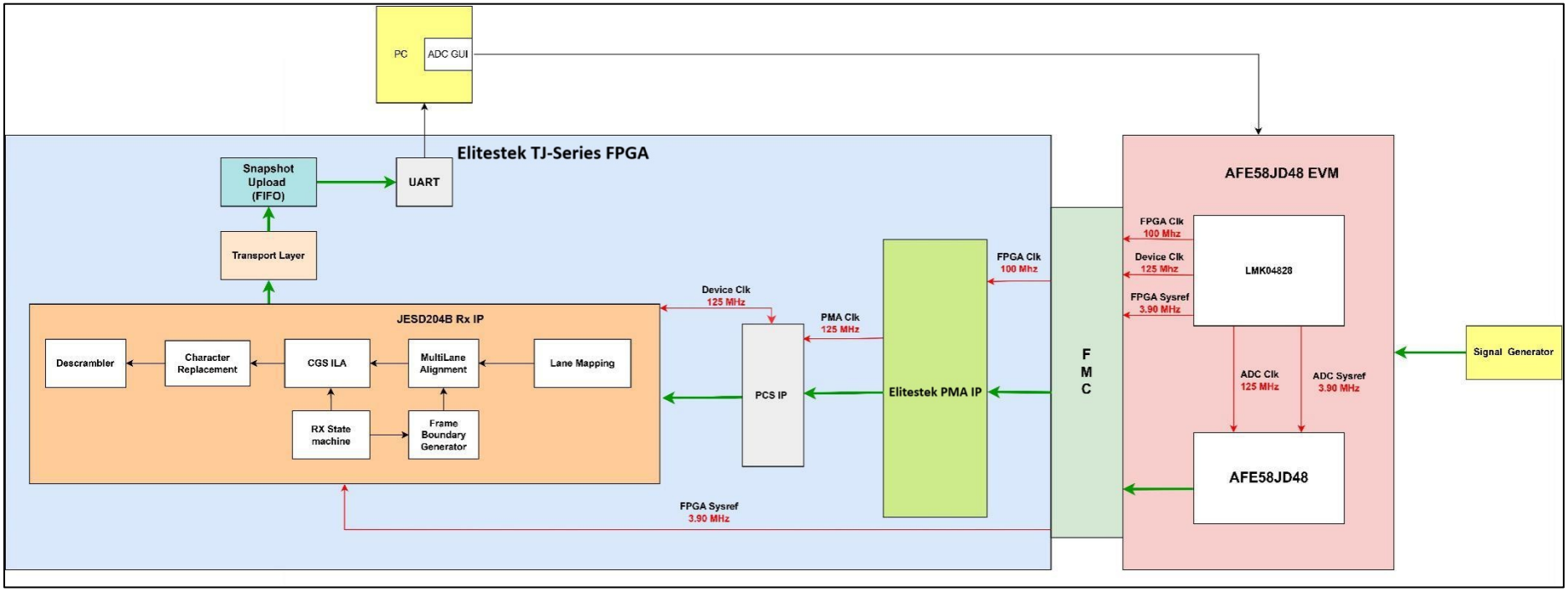


Figure 95. Hardware Validation Block Diagram of JESD204B Receiver with ADC AFE58JD48 at 5Gbps line rate

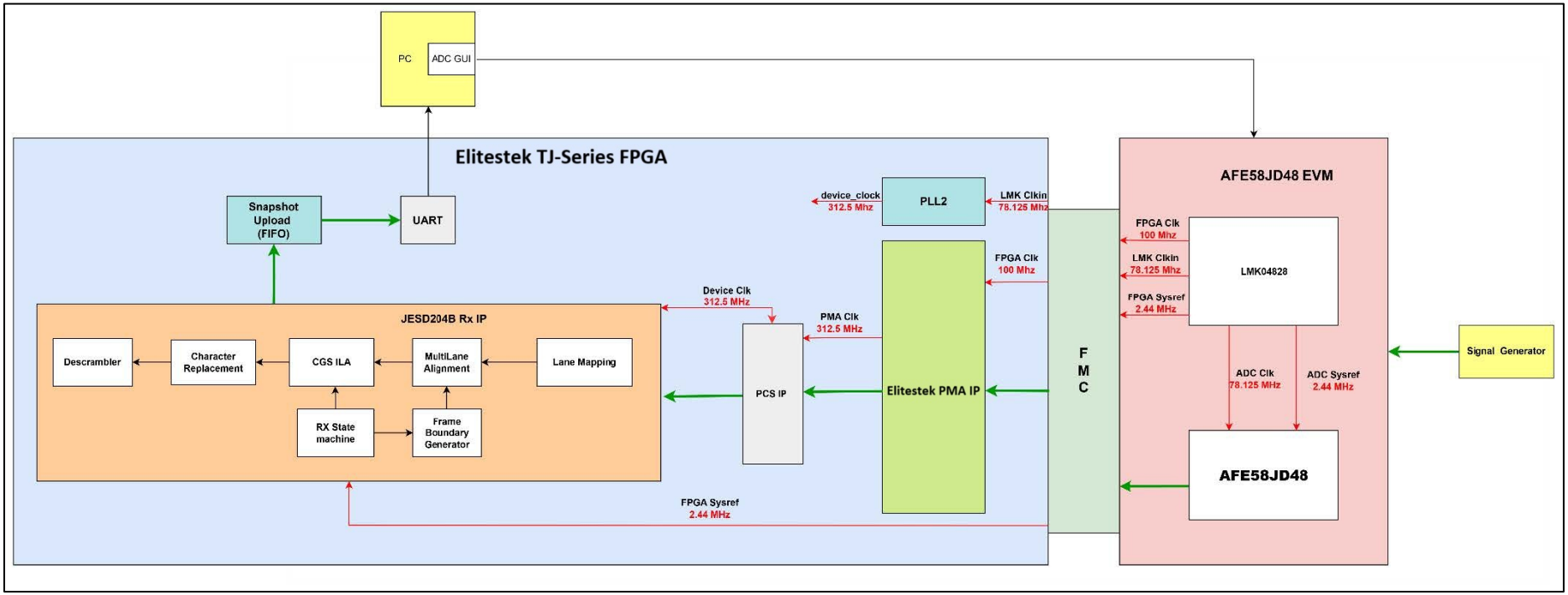


Figure 96. Hardware Validation Block Diagram of JESD204B Receiver with ADC AFE58JD48 at 12.5Gbps line rate

Note: The block information is mentioned in section 4.5 (JESD204B Receiver Hardware Testing Overview

9.2 Test Set up of Elitestek Evaluation Board with ADC

9.2.1 Test Setup image

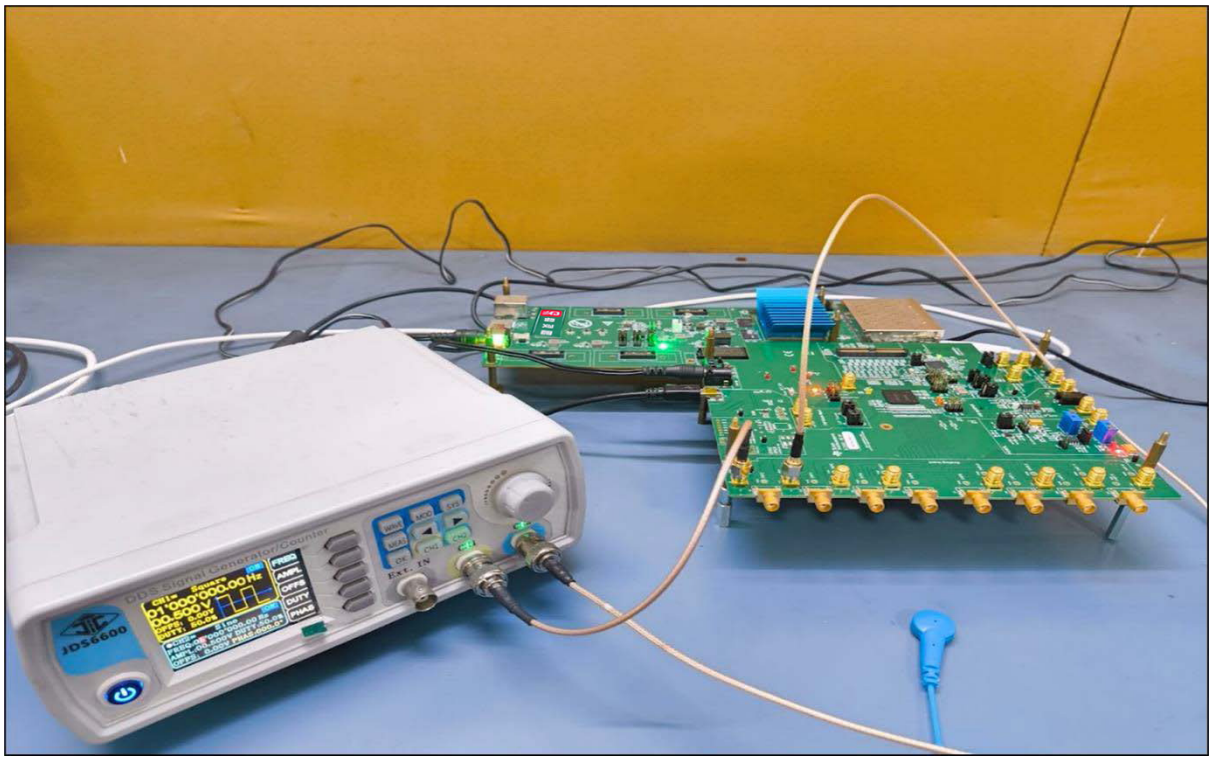


Figure 97. Test Set up of Elitestek Evaluation Board with ADC

9.2.2 Hardware Test Equipment

Following are the test set up equipments:

Sr No.	Hardware Requirement for ADC Demo	Quantity
1	Elitestek TJ375N1156X Eval board	1
2	Elitestek JTAG : Type A to Type C USB cable	1
3	Elitestek : 12V - 6A Power Adapter	1
4	AFE58JD48EVM board	1

5	Type A to Mini B USB cable	1
6	5V 3A power adapter	1
7	Power Splitter (currently we only have 1x6 power splitter)	1
8	Power attenuator	1
9	50-ohm terminations for power splitter spare ports	4
10	SMA to female header jumper cable	1
11	SMA to SMA cable	2
12	SMA to BNC cable	2
13	Some studs to make setup mechanically stable	20-25
14	Oscilloscope	1
15	Scope probe	1
16	Oscilloscope power cord	1
17	Laptop (should have Efinity, tcl and AFE58JD48EVM Gui installed in it)	1
18	Laptop charger	1
19	Signal generator (JDS6600)	1

Table 43.Hardware Requirement for ADC Demo

9.2.3 Software Used

9.2.3.1 LMK Tool

- The LMK Tool version used is v1.7.7.6
- This tool configures the LMK04826 chip in the ADC evaluation board.

- After selecting the LMK device, according to the required clock values, the user needs to make the settings in the GUI and update the register set values in the tcl procs accordingly.

9.2.3.2 ADC GUI

- The ADC GUI version used is 1.2.3
- This tool configures the ADC chip AFE58JD48 and the JESD204B TX protocol present on the ADC EVM.
- According to the required mode, the user must select the ADC GUI settings and save the configuration file.

9.2.3.3 Wave Vision Software

- The Wave Vision Software version used is 5.0.6.465 (P2R1 Beta).
- This software plots the waveform from the data received through UART IP.

9.3 Test Procedure

9.3.1 Hardware Connection Procedure

1. Connect TI ADC EVM (TI ADS54J66)with the Elitestek TJ-Series Evaluation (TJ375N1156X) Board on **J15 FMC connector** (Quad 2) .
2. Connect host PC with Elitestek TJ-Series Evaluation Board via USB cable, which can be used as UART and JTAG
3. Start the Signal Generator and connect it with ADC EVM through SMA cables.

9.3.2 ADC GUI Configuration Test Procedure

1. The ADC is configured through the GUI
2. Open the GUI and load the required configuration (.cfg) file through which we want to operate the ADC eval board GUI.
3. Select the File option → Open configuration → Go to folder : ../JESD204B_Porting_Efinix_REL_1_0\JESD204B_RX_ADC_Files\ADC_Configuration_Files and select the JESD 125MSPS_Subclass1_8L_updated.cfg for 5Gbps.
   select the JESD 31.25MSPS_Subclass1.cfg for 12.5Gbps

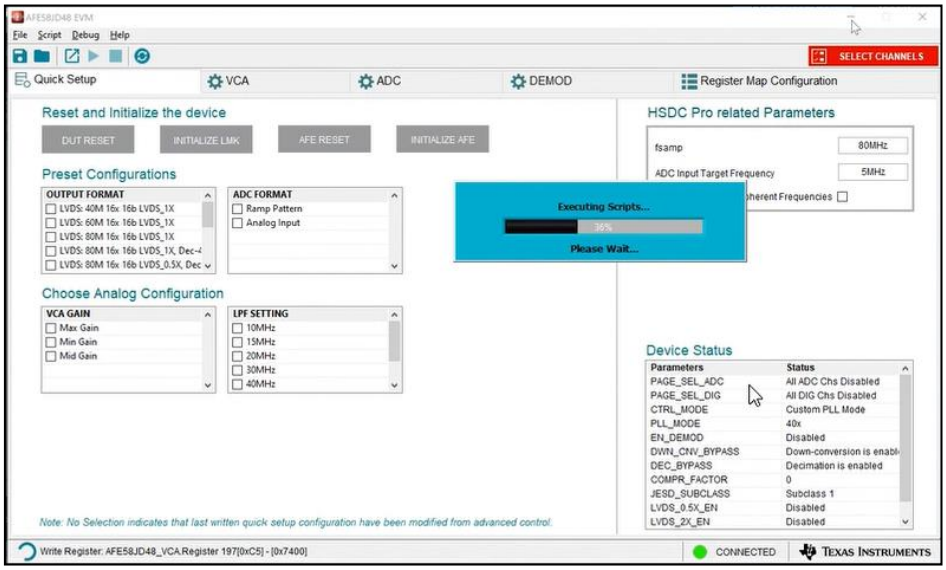


Figure 98.Configuration file loading in the ADC GUI

4. Once ADC is configured, program the bit file to the Elitestek evaluation board.

9.3.3 TCL Script Sequence Test Procedure

a) Following steps to be followed for the installation of LFT TCL Software

i. Go to Control Panel -> Add / Remove Program -> Turn Windows Feature on or off - > Enable .NetFramework 3.5

ii. Let it be downloaded from Windows Update

iii. Copy LFT_TCL folder present in the path : ..\JESD204B_Porting_Efinix_REL_1_0\TCL_Software inside the C:\

iv. Install TclTk-8.3_for_N2X.exe

v. Install vcredist_x86.exe

vi. Run Win_Driver.bat (present in the path LFT_TCL\bin_USB_UART) as Administrator to confirm correct installation

b) There are four tcl files present inside the folder : ../JESD204B_Porting_Efinix_REL_1_0\JESD204B_RX_ADC_Files\TCL_Script_Software\TCL_Script

i. tclshrc.tcl: Source file

ii. jesd204b_sequence_test_5Gbps.tcl/jesd204b_sequence_test_12_5Gbps.tcl: Automated sequence of procs for ADC

iii. streaming_8_channels.tcl: Script to decrypt the hex data received from the ADC

iv. jesd204b_rx_procs_verilog.tcl: Script that includes individual procs for ADC

c) Keep the tclshrc.tcl file on the following path: C:\Users\user (*Note: username can change from PC to PC*)

d) Make sure the file given below are in the path: C:\LFT_TCL\bin_USB_UART

i. jesd204b_tx_procs.tcl

ii. jesd204b_sequence_test_5Gbps.tcl

iii. jesd204b_sequence_test_12_5Gbps.tcl

iv. jesd204b_rx_procs_verilog.tcl

e) Make sure the file streaming_8_channels.tcl file is in the path: C:\LFT_TCL\scripts\tcl\efinix

f) Inside the path C:\LFT_TCL\bin_USB_UART, there is a Ukko_init.tcl file, where we need to set the baud rate and com port

Set the baud rate to 115200 and com port according to the detected port.

```
19
20  #g_comPort:   UART => UART COM Port#
21  set g_comPort 9
22  #g_comPort:   UART => UART BaudRate
23  set g_baudrate 115200
```

Figure 99.Com port and Baud rate settings for ADC

Note: Initially, while setting up the tcl user need to make these directories

g) Open the TCL IDE from the start menu by default the required TCL script is sourced

h) The console will display the option to select the testing for the JESD204B Transmitter with DAC or JESD204B Receiver with ADC. Select option 2 or 4 for testing the JESD204B Receiver with ADC with respect to the required line rate.

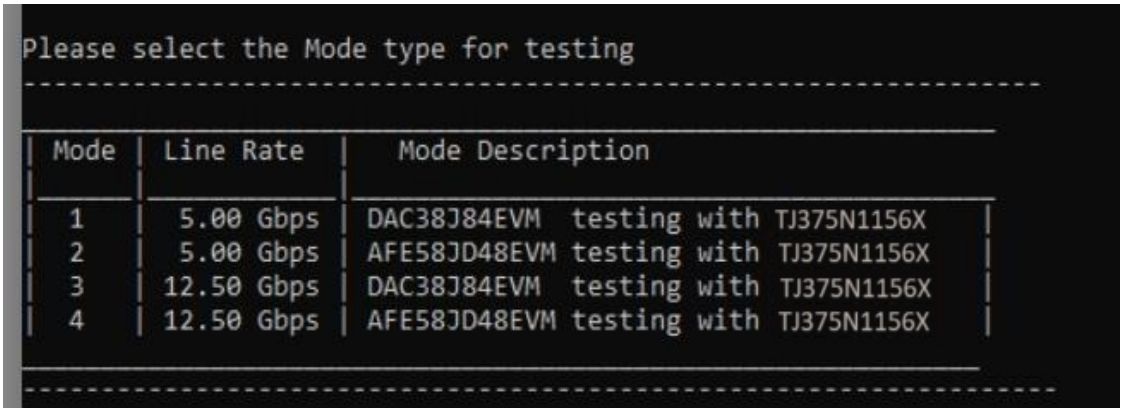


Figure 100.ADC TCL console image 1

i) The script jesd204b_sequence_test.tcl includes the complete sequence from the JESD204B configuration to the capturing of the data through snapshot streaming interface and data decryption for each ADC input

j) After selection of ADC testing the sequence of measuring the clock frequency, JESD204B RX IP configuration for 40X mode/160X mode and status of errors and link up information are displayed as shown in the below image

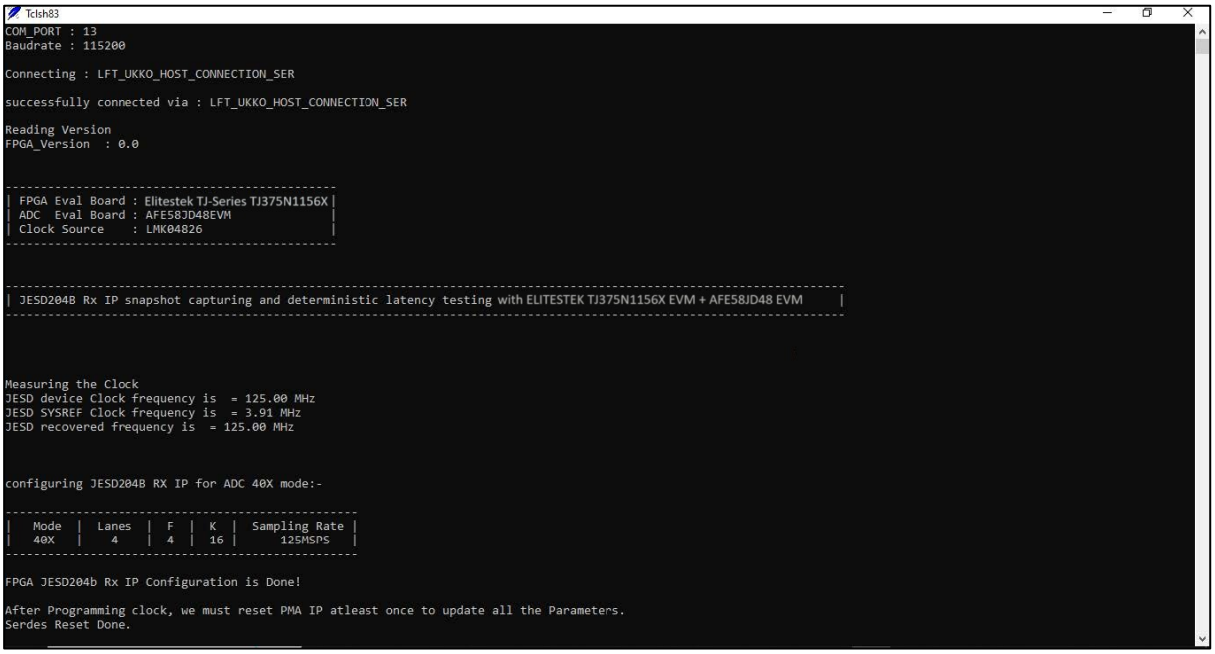


Figure 101. ADC TCL console image 2

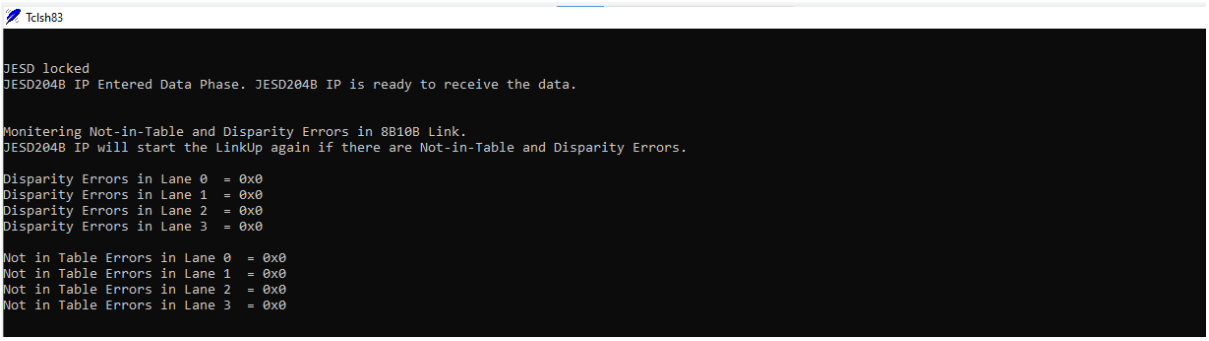


Figure 102. ADC TCL Console image 3

k) Once link up is done without any errors, the captured ADC sample data are uploaded to the host PC with user permission, if user wants to upload the data select the option 1

Figure 103. ADC TCL Console image 4

l) Once the decryption is done for captured samples, open the TI wave vision software to view the waveform for the captured file.

v. Open the WaveVision tool

vi. Once the GUI is open, select the import option from the plot

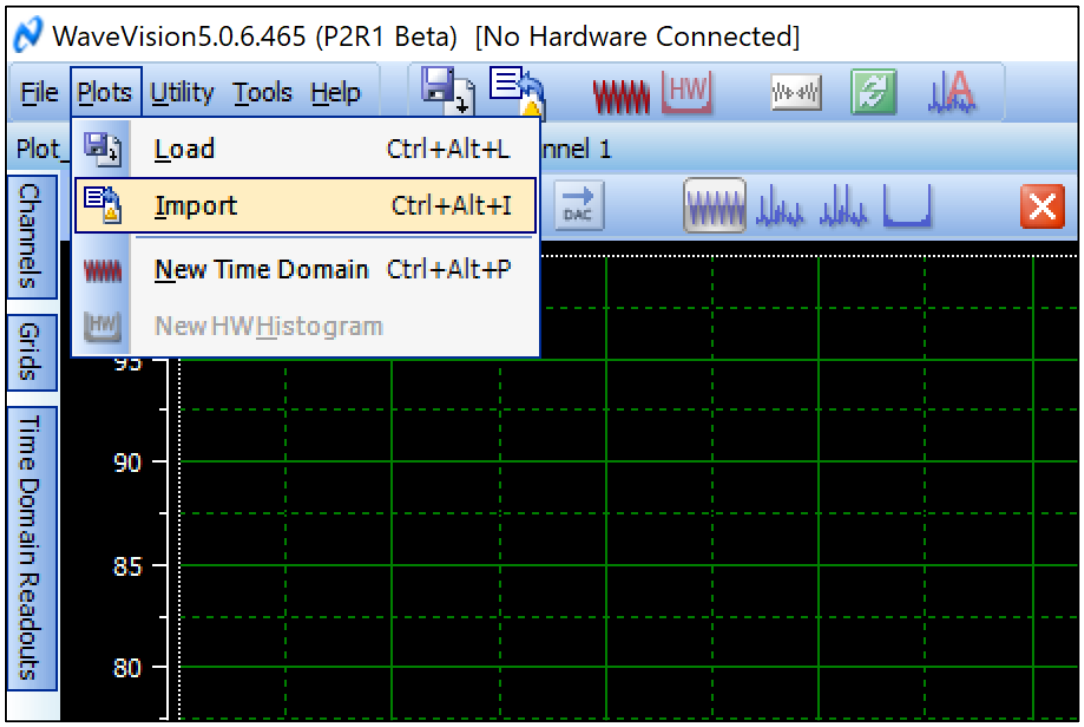


Figure 104. WaveVision Sofwtare GUI

vii. Select the required ADC decrypted samples.

viii. Mention the sampling frequency as 125MHz for 40X mode and the resolution as 16-bits

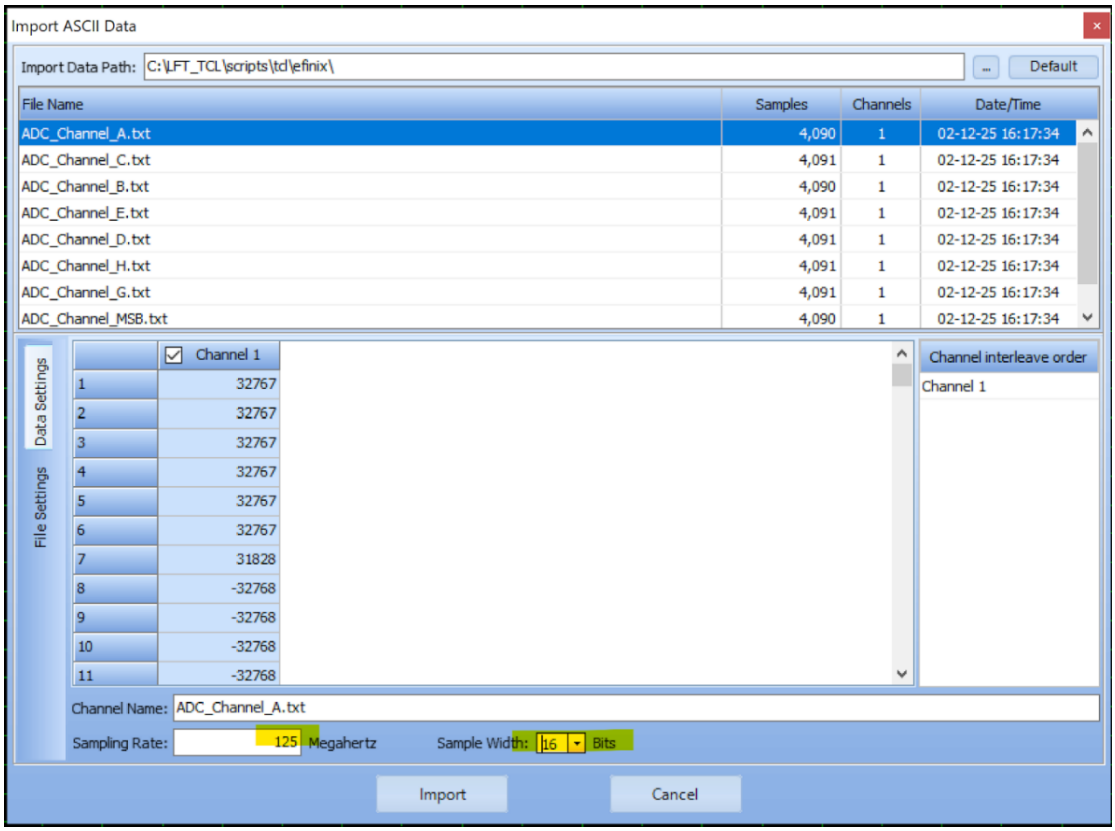


Figure 105. Selection of channel to view the waveform

ix. Click on the import after all configurations are done

x. Both frequency and time domain waveforms are plotted

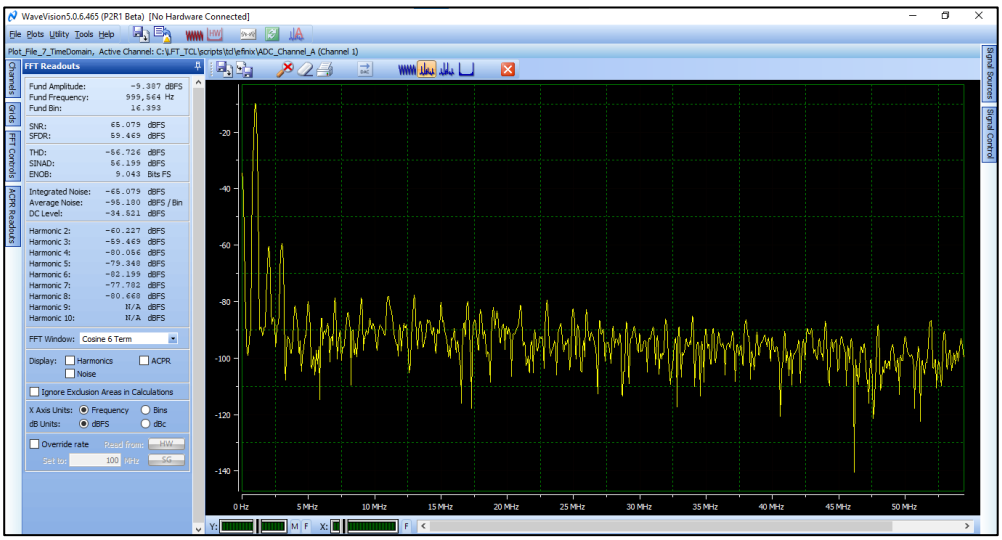


Figure 106. Frequency domain plot in WaveVision software

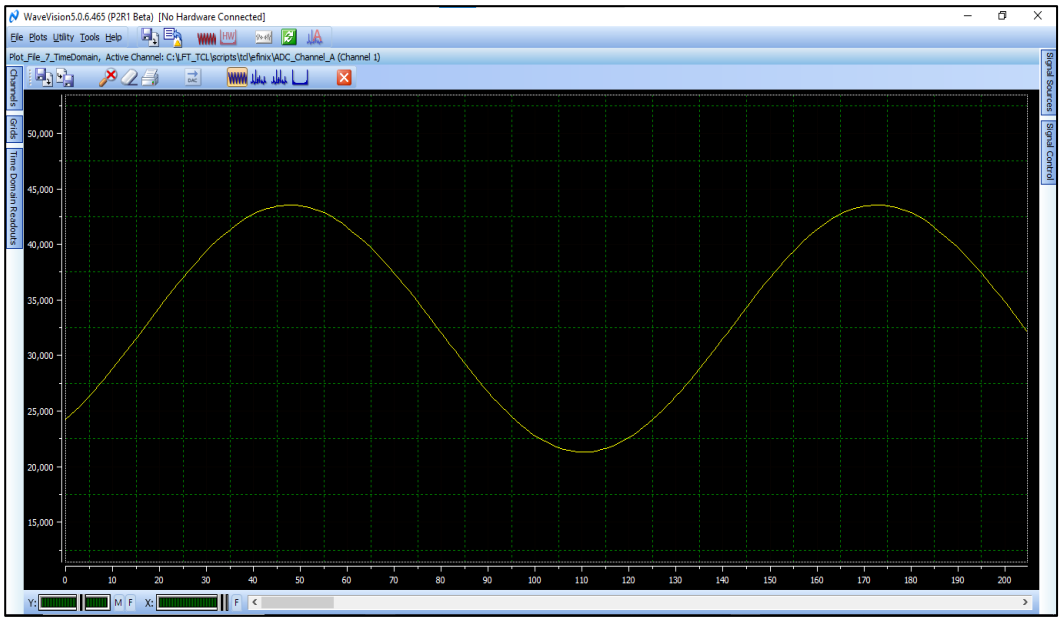


Figure 107. Time domain Plot in Wave Vision Software

9.4 Test Cases for 5 Gbps

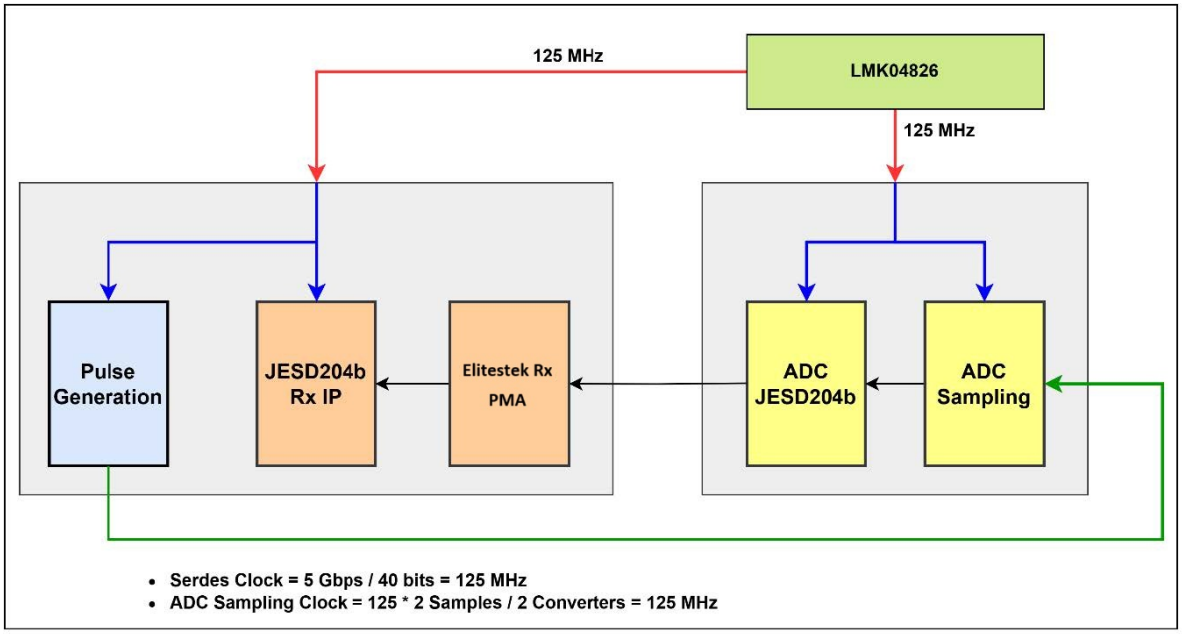


Figure 108 : Block Diagram depicting Clock Architecture for 5 Gbps Line Rate

SerDes Clock = SerDes Rate / SerDes Data Width

	SerDes Rate	**SerDes Data width (Resolution after 8b10b)**	**SerDes Clock**
LFT JESD204B RX(Elitestek FPGA)	5 Gbps	40 bits	125 MHz
TI ADC AFE58JD84	5 Gbps	40 bits	125 MHz

Table 44. Elitestek Eval board and DAC Data rate Table

The following are the different modes of testing done for ADC:

ADC Input sampling rate = SerDes Rate / (ADC Resolution after 8b10b * No of converters in a single lane)

Test Case	**Modes (LMF)**	**No. of converters in single lane**	**ADC Input Sampling Rate (MSPS)**	**ADC Output Sampling Rate (MSPS)**	**LMK Sysref**
0	484 (40X)	2	125.00	125.00	Continuous

Table 45 .JESD204B Transmitter Test Cases for 5 Gbps

9.4.1 Test Case 0 : LMF = 484 (40X Mode)

9.4.1.1 Input Frequency = 1MHz

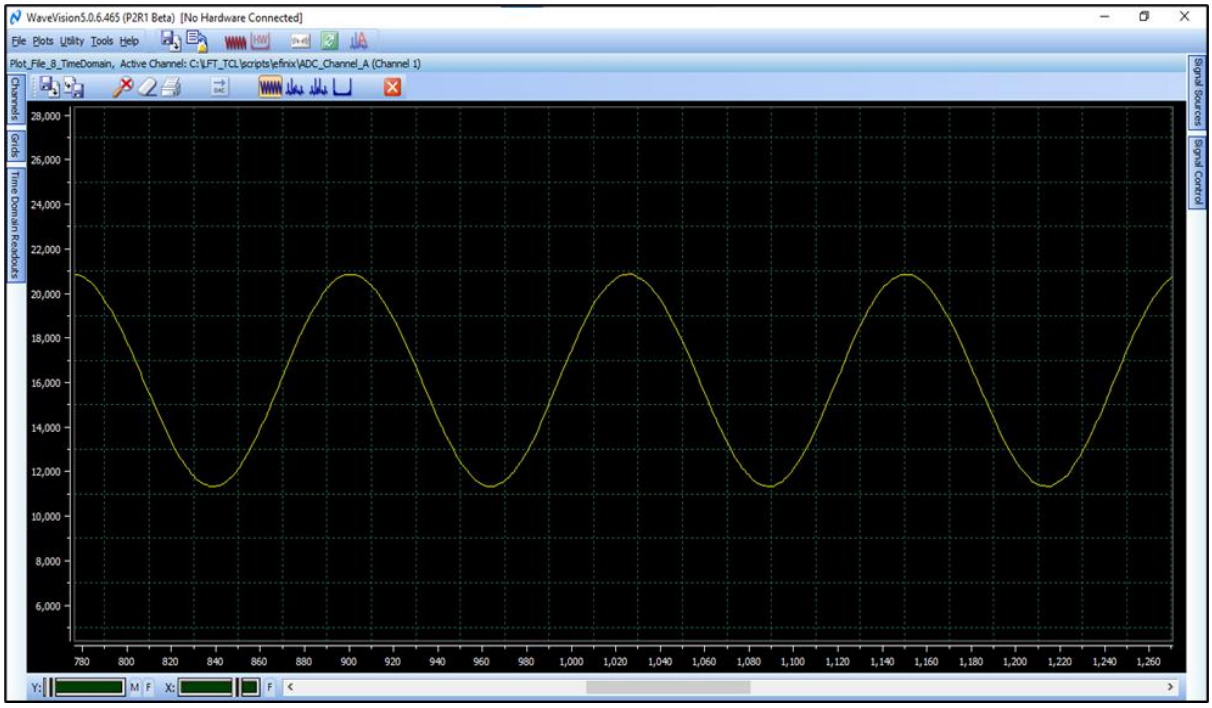


Figure 109 .TC 0: Time domain plot for captured waveform for input frequency of 1 MHz

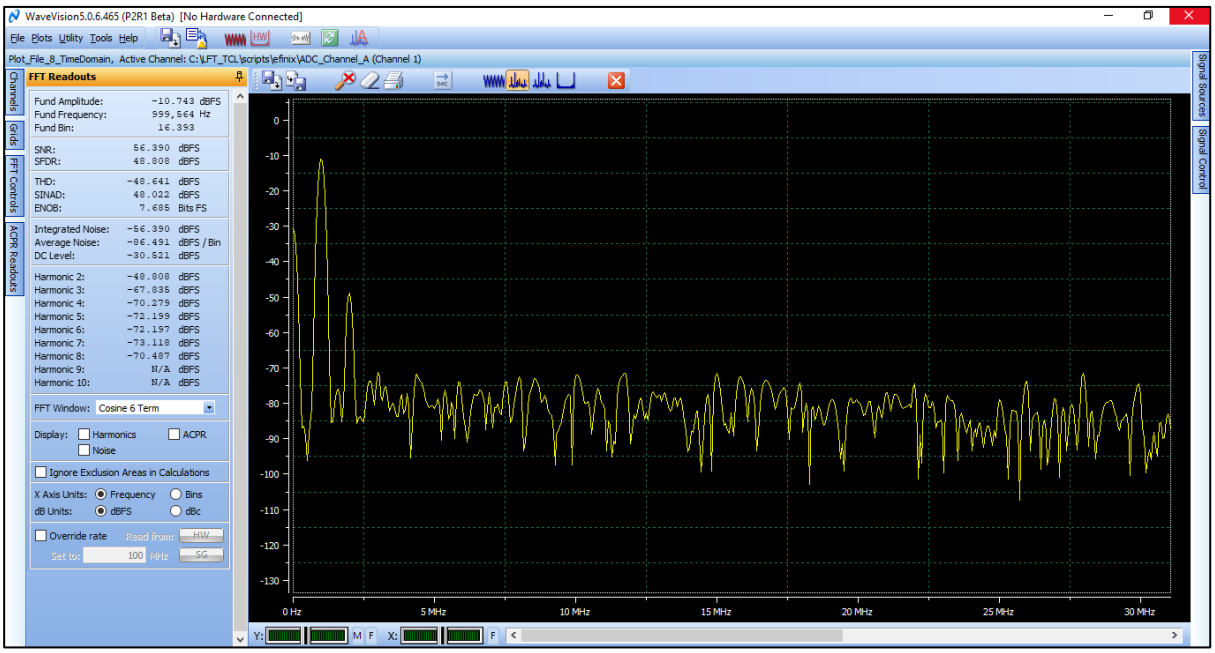


Figure 110.TC 0: Frequency domain plot for captured waveform for input frequency of 1 MHz

9.4.1.2 Input Frequency = 62.5 MHz

Figure 111.TC 0: Time domain plot for captured waveform for input frequency of 62.5 MHz

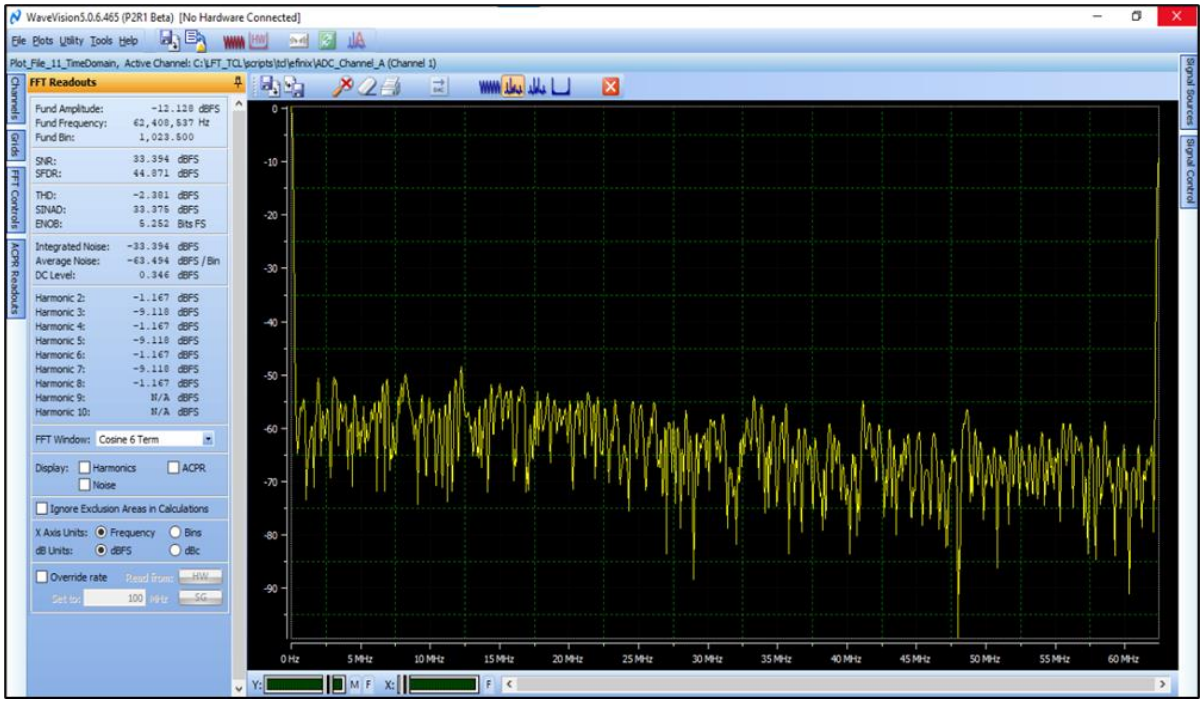


Figure 112.TC 0: frequency domain plot for captured waveform for input frequency of 62.5 MHz

Note: For reference purpose, Below is the waveform generated through the Octave Input frequency = 62.5 MHz with fs = 125MHz

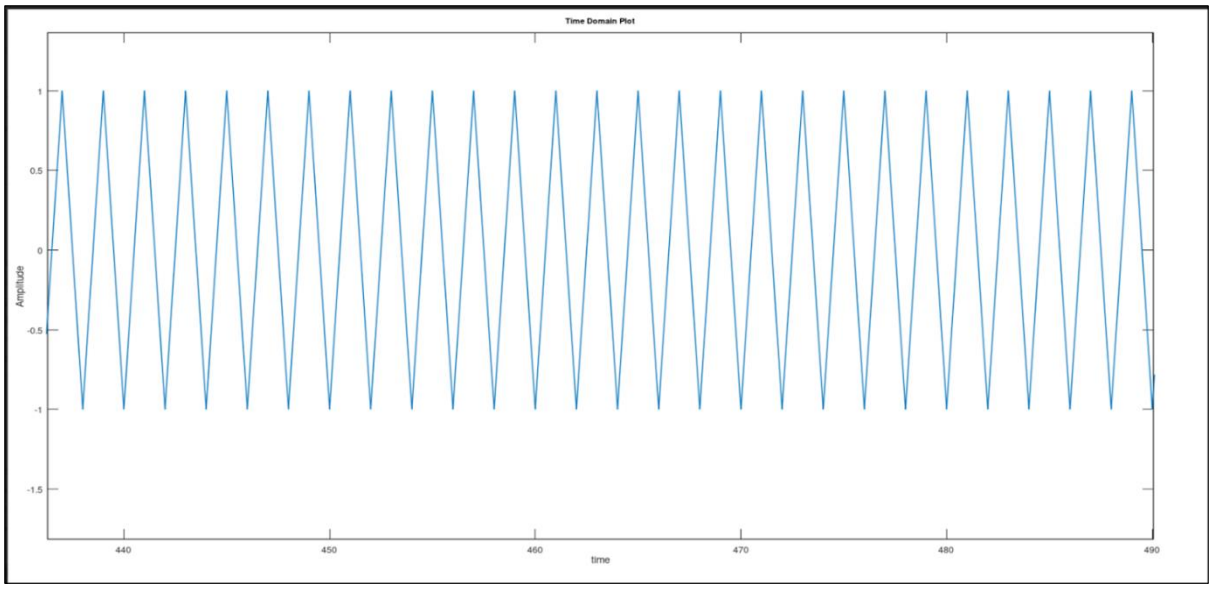


Figure 113. Waveform generated through octave code with Input frequency as 62.5MHz

9.5 ADC Mode Description

9.5.1 Mode 40X, LMF = 484

Lanes	Lane Mapping
Lane 0	D1, D2
Lane 1	D3, D4
Lane 2	D5, D6
Lane 3	D7, D8

Table 46. ADC Lane Mapping for LMF = 484

Note: Here, the Dx stands for the ADCx[15:0], with ADC1 data coming out first on the lane and ADC2 data coming out last from lane 0

Parameter	Value
Number of lanes	1
ADC SerDes Rate	5 Gbps
ADC Resolution after 8b/10b	20 bits
No. of converters in single lane	2
ADC Input sampling rate	5/ (20*2) = 125MSPS

Table 47. ADC Parameter Values for 40 X mode

9.5.2 Mode 160X, LMF = 148

Lanes	Lane Mapping
Lane 0	D1, D2, D3, D4, D5, D6, D7, D8

. ADC Lane Mapping for LMF = 148

Note: Here, the Dx stands for the ADCx[15:0]

Parameter	Value
Number of lanes	1
ADC SerDes Rate	12.5 Gbps
ADC Resolution after 8b/10b	20 bits
No. of converters in single lane	8
ADC Input sampling rate	12.5/ (20*8) = 78.125 MSPS

Table 48. ADC Parameter Values for 160 X mode

9.6 Test Cases for 12.5 Gbps

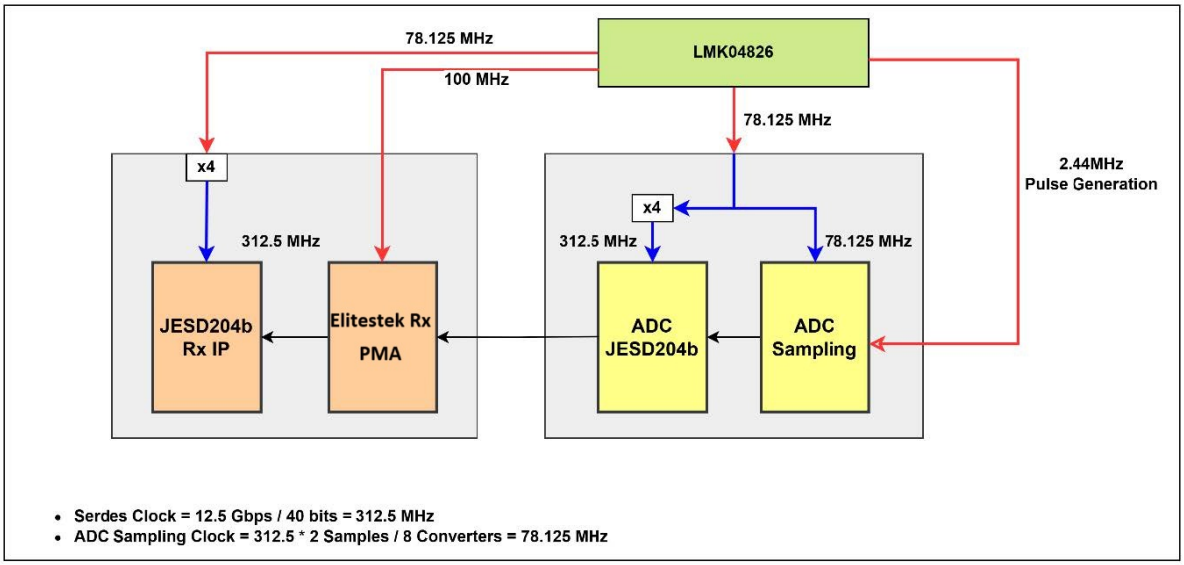


Figure 114: Block Diagram depicting Clock Architecture for 12.5 Gbps Line Rate

SerDes Clock = SerDes Rate / SerDes Data Width

	SerDes Rate	**SerDes Data width (Resolution after 8b10b)**	**SerDes Clock**
LFT JESD204B RX(Elitestek FPGA)	12.5 Gbps	40 bits	312.5 MHz
TI ADC AFE58JD84	12.5 Gbps	40 bits	312.5 MHz

Table 49. Elitestek Eval board and DAC Data rate Table

The following are the different modes of testing done for ADC:

ADC Input sampling rate = SerDes Rate / (ADC Resolution after 8b10b * No of converters in a single lane)

Test Case	**Modes (LMF)**	**No. of converters in single lane**	**ADC Input Sampling Rate (MSPS)**	**ADC Output Sampling Rate (MSPS)**	**LMK Sysref**

0	148 (160X)	8	78.125	78.125	Continuous

Table 50 .JESD204B Transmitter Test Cases for 12.5 Gbps

9.6.1 Test Case 0 : LMF = 148 (160X Mode)

9.6.1.1 Input Frequency = 1MHz

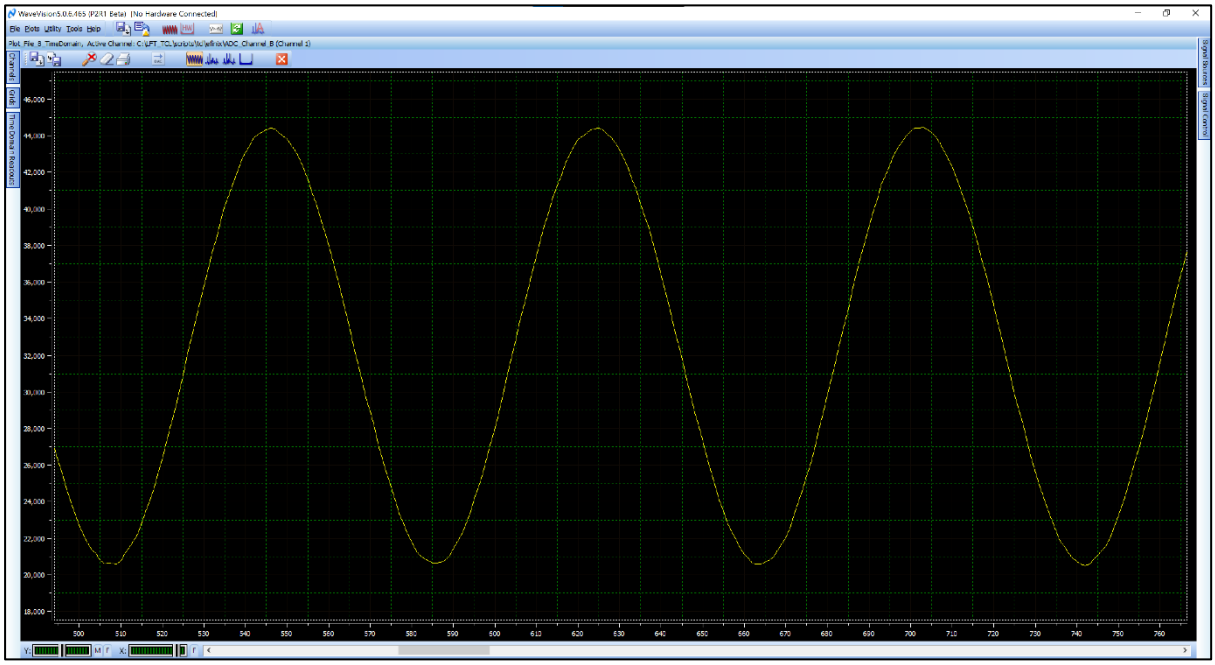


Figure 115 .TC 0: Time domain plot for captured waveform for input frequency of 1 MHz

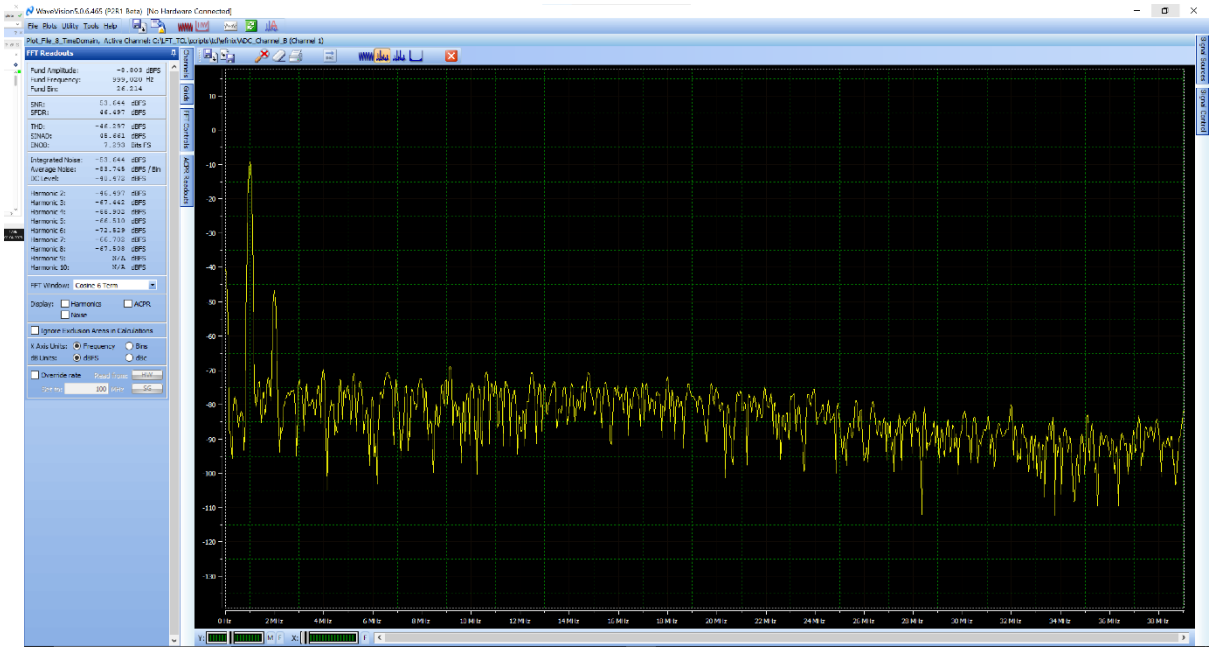


Figure 116.TC 0: Frequency domain plot for captured waveform for input frequency of 1 MHz

9.6.1.2 Input Frequency = 39.0625 MHz

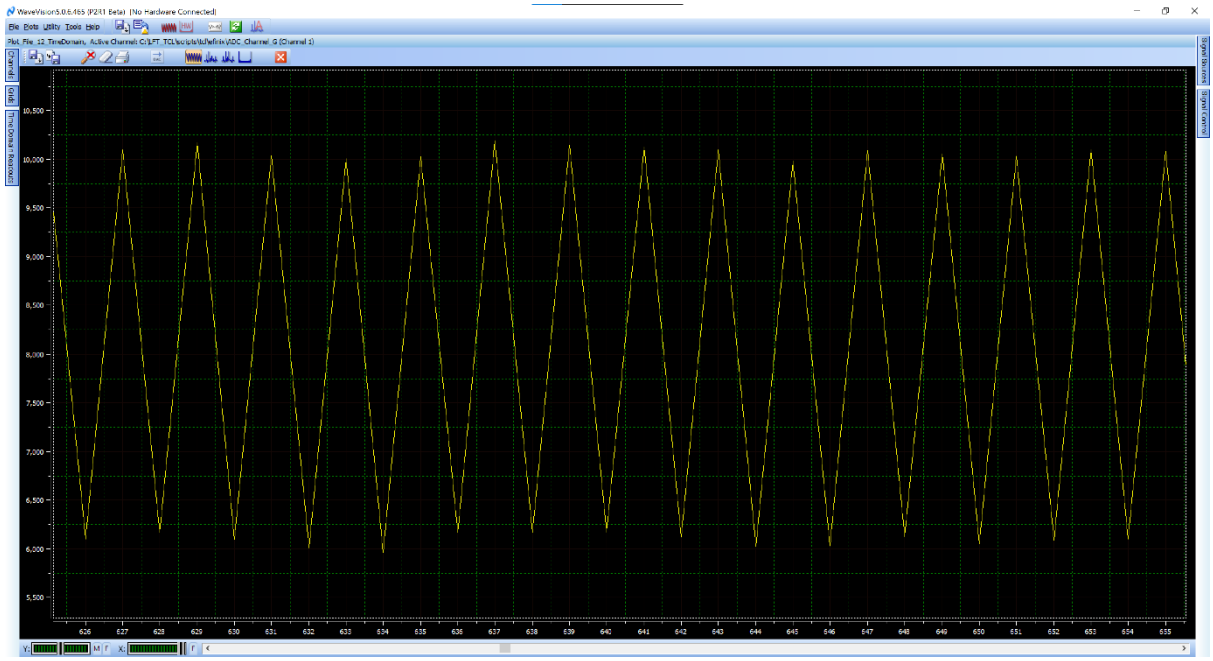


Figure 117.TC 0: Time domain plot for captured waveform for input frequency of 39.0625 MHz

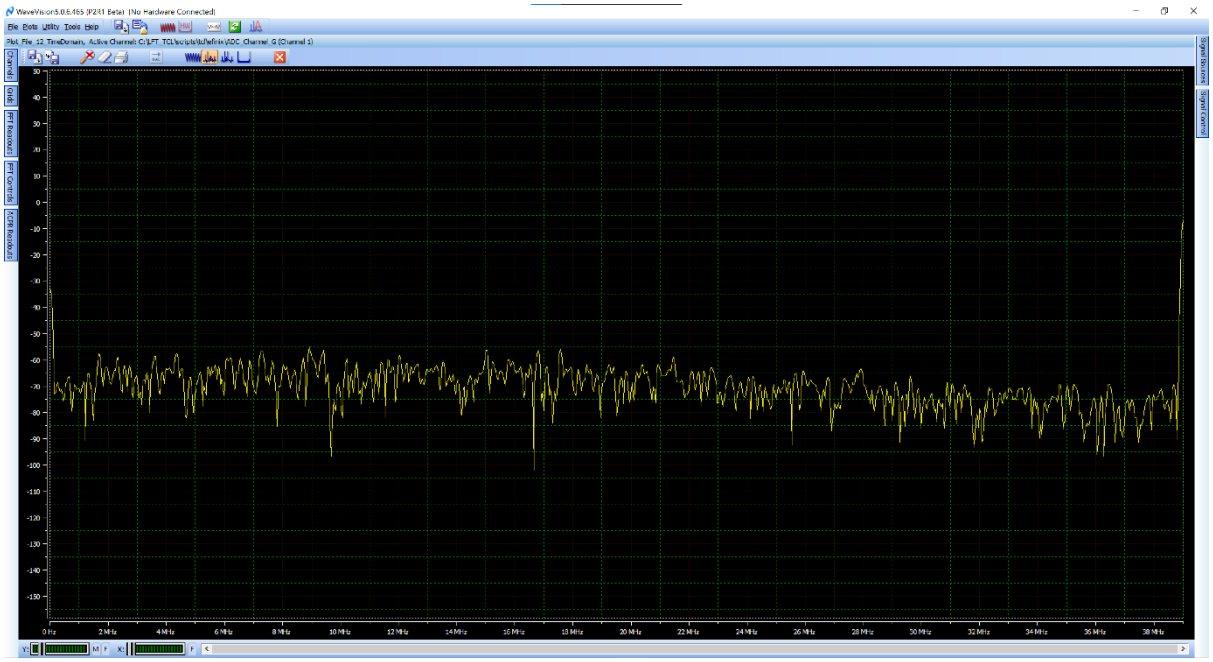


Figure 118.TC 0: frequency domain plot for captured waveform for input frequency of 39.0625 MHz

Note: For reference purpose, below is the waveform generated through the Octave Input frequency = 39.0625 MHz with fs = 78.125MHz

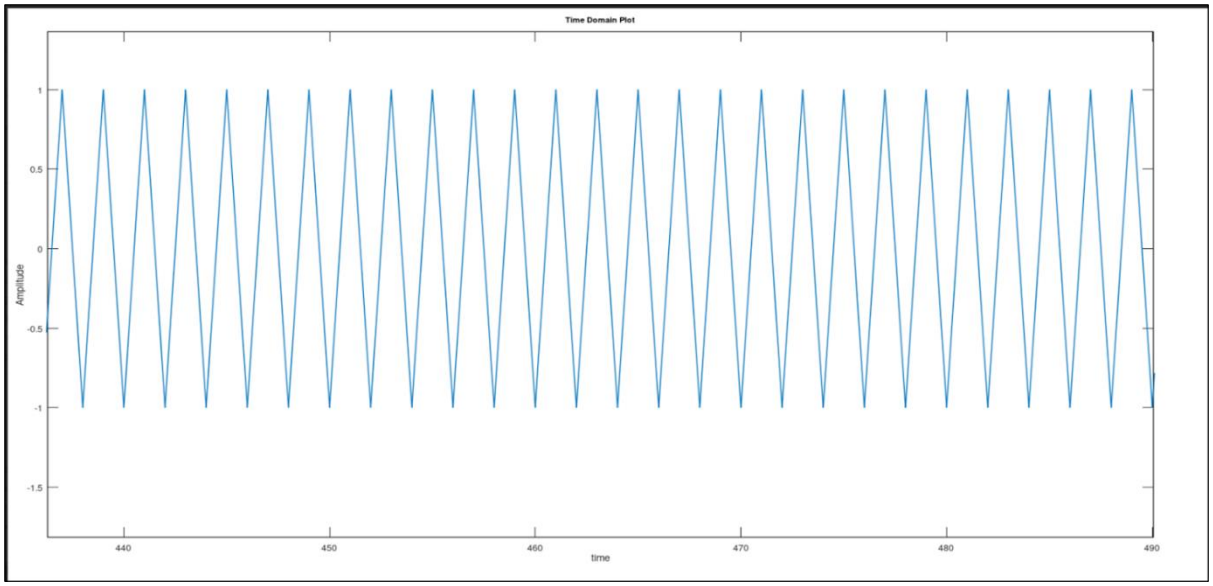


Figure 119. Waveform generated through octave code with Input frequency as 39.0625M

10 Deterministic Latency for JESD204B Receiver with ADC

10.1 Deterministic Latency for JESD204B Receiver with ADC at 5Gbps

10.1.1 Hardware Validation Block diagram for Deterministic Latency testing with ADC at 5Gbps

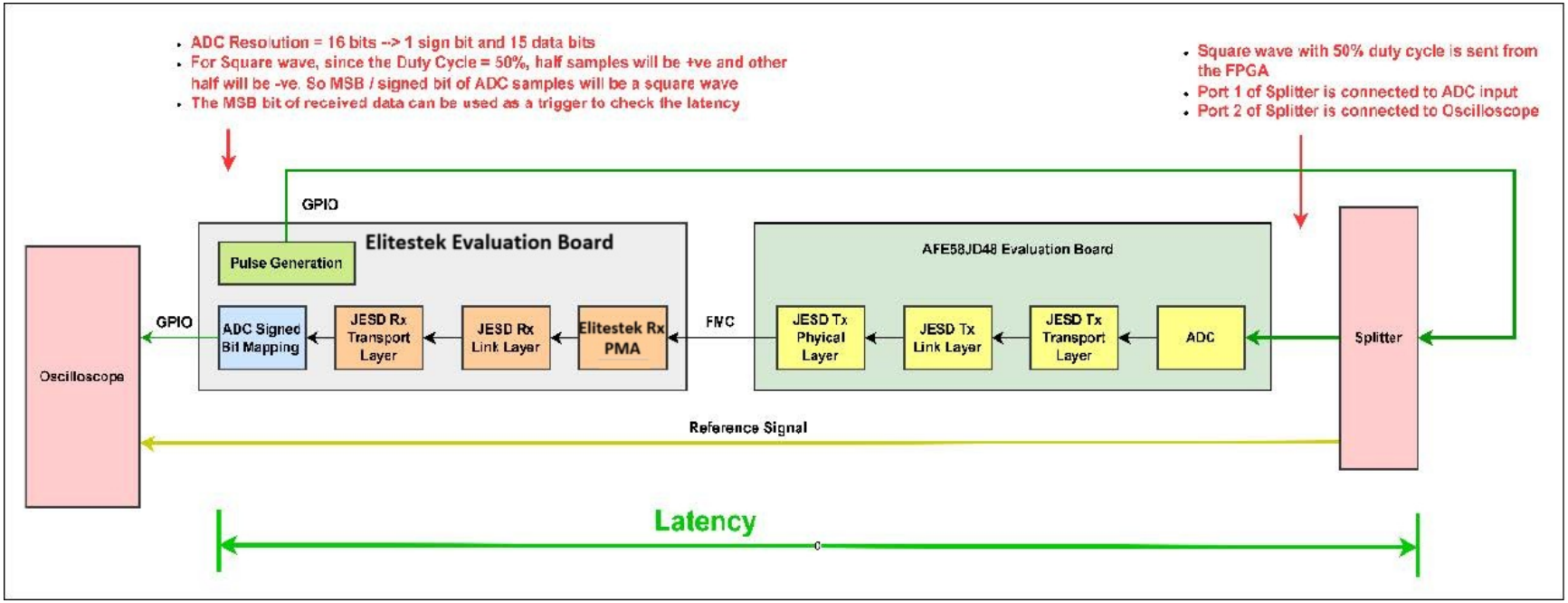


Figure 120. Deterministic Latency testing of JESD204B Receiver with ADC at 5Gbps

- The pulse generation block in the Elitestek FPGA will generate a square wave, which is fed to the splitter.
- The Port 1 of the splitter port will be connected to the Oscilloscope as a reference signal and the Port 2 is given as an input to the ADC.
- The MSB bit of the received data from the JESD204B RX Transport layer present in Elitestek FPGA is used as a trigger to check the latency.
- The deterministic latency is determined from the start of the reference signal to the start of the signed bit of the ADC sample.

10.1.2 Test Setup of Elitestek Evaluation Board with ADC for Deterministic Latency testing at 5Gbps.

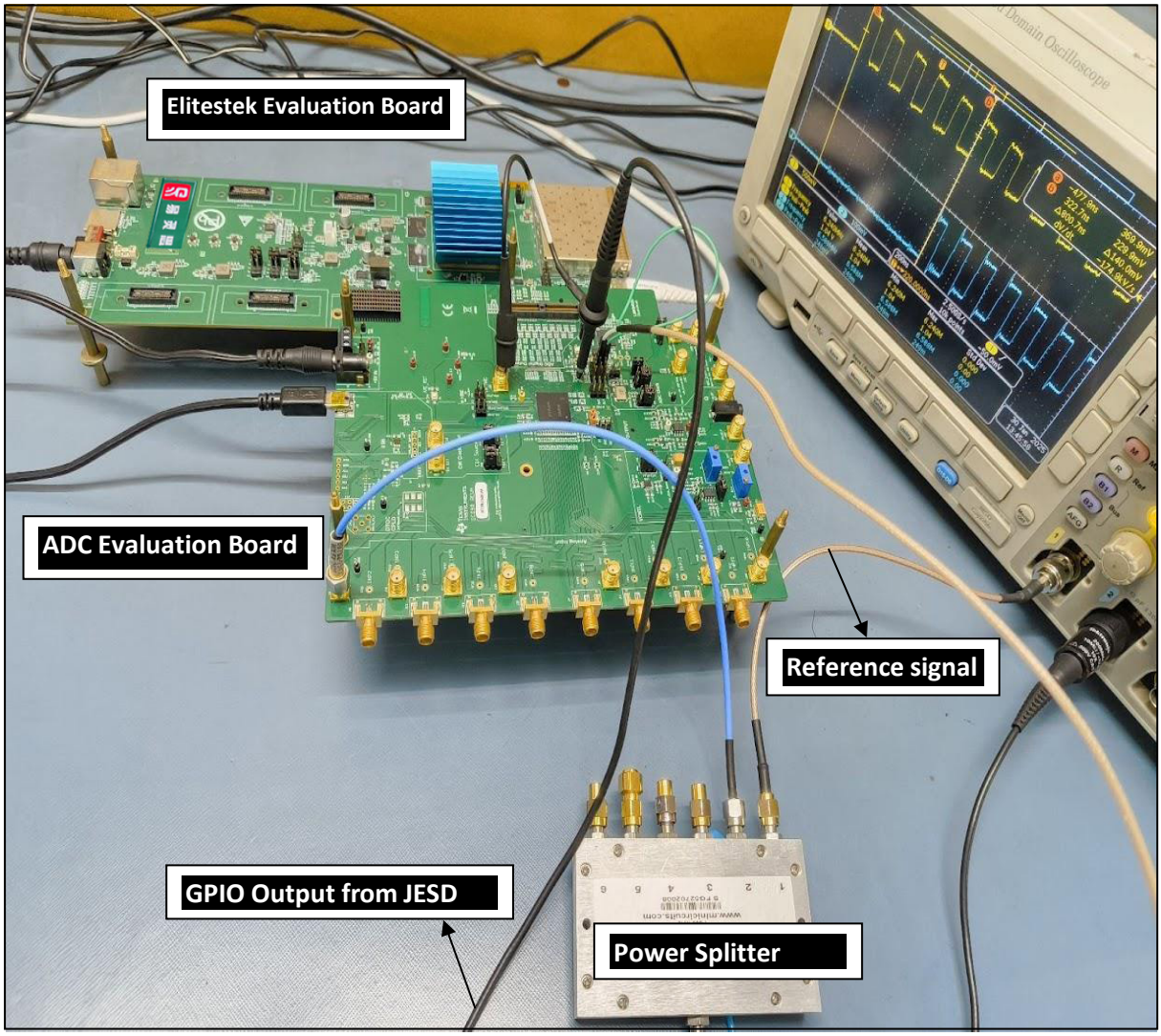


Figure 121.Test set up of Elitestek Evaluation Board with ADC for testing Deterministic Latency at 5Gbps

- One of the outputs from the Power splitter is connected to one channel of CRO, and the other is given to the ADC evaluation board.
- The MSB bit of the output data is mapped to the GPIO, which is connected to another channel of the CRO.

Note: Refer to sections 8.2.2 and 8.3.3 for the Hardware Test Equipment and Software used for the testing

10.1.3 Test Procedure

Note: The procedure to execute the test case for Deterministic Latency testing is the same as discussed in Section 8.3.

For Deterministic Latency testing, the trigger condition in the oscilloscope must be set up.

10.1.4 Test Cases

10.1.4.1 Test Case 0 : LMF = 484 (40X Mode)

10.1.4.1.1 Input Frequency = 6.25 MHz

Figure 122. Deterministic Latency capture between input square and ADC MSB bit at input frequency of 6.25MHz

The green colour waveform is the input square waveform, and the red colour waveform is the MSB bit of the received data.

Deterministic latency in the path is in range of 789.1ns with variation of 150ps on every power cycle

Below table shows the Minimum, Typical and Maximum deterministic latency values including variation on cold and warm reset.

Reset Type	Mode	Min Value (ns)	Typical Value (ns)	Max Value (ns)	No. of Iterations	Variation (ps)
Cold	40X	789.81	789.95	790.1	30	150
Warm	40X	789.81	789.91	790.03	30	100

Table 51. Deterministic latency variation table for JESD204B RX testing with ADC at 5Gbps

10.2 Deterministic Latency for JESD204B Receiver with ADC at 12.5 Gbps

10.2.1 Hardware Validation Block diagram for Deterministic Latency testing with ADC at 12.5Gbps

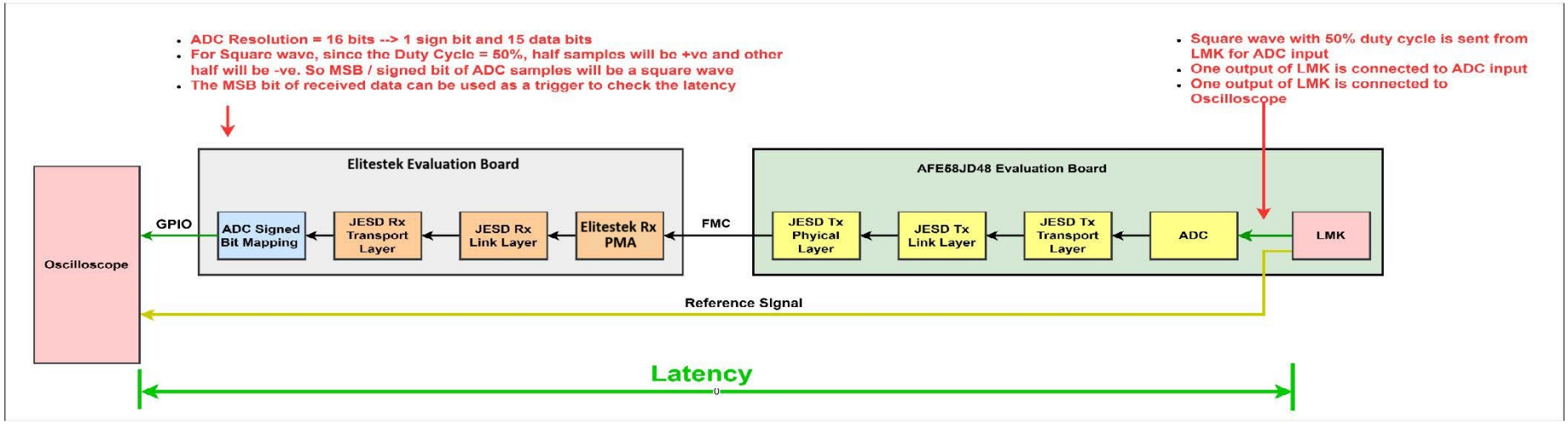


Figure 123. Deterministic Latency testing of JESD204B Receiver with ADC at 12.5Gbps

- One output of LMK is used for ADC input data generation and reference signal for checking deterministic latency .
- Another Output of LMK will be connected to the Oscilloscope as a reference signal and the output P is given as an input to the ADC.
- The MSB bit of the received data from the JESD204B RX Transport layer present in Elitestek FPGA is used as a trigger to check the latency.
- The deterministic latency is determined from the rising edge of reference input to the rising edge of ADC_MSB bit.

10.2.2 Test Setup of Elitestek Evaluation Board with ADC for Deterministic Latency testing at 12.5 Gbps.

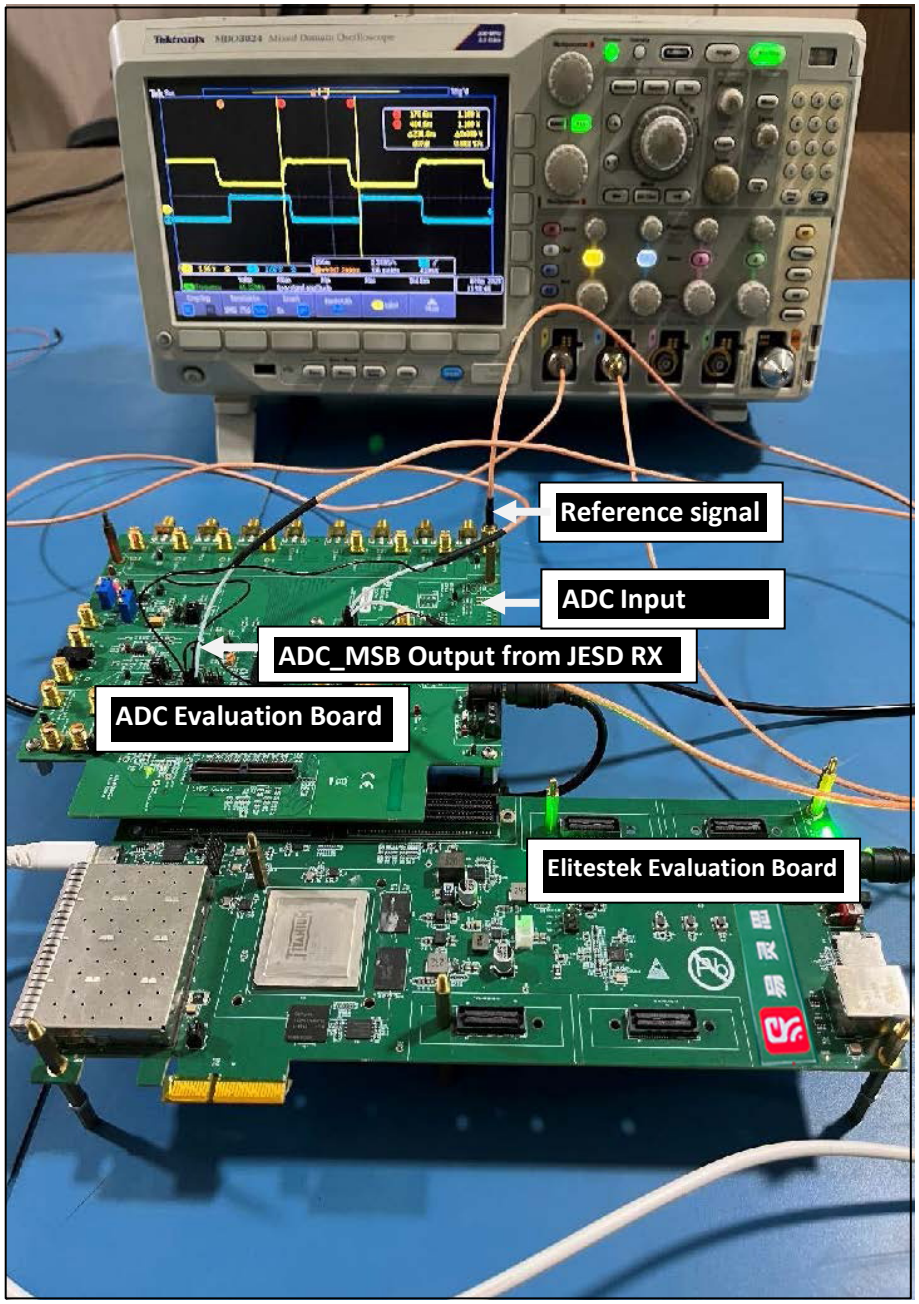


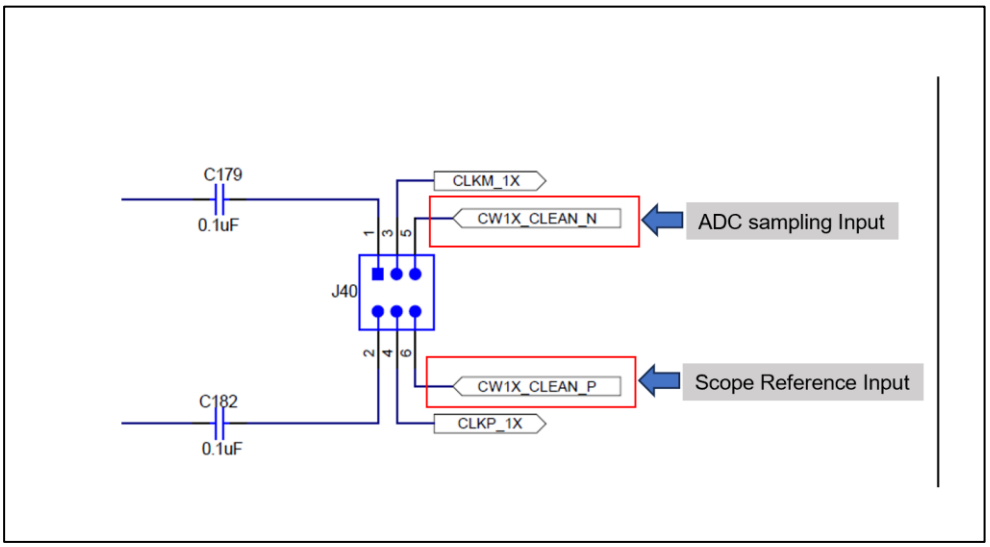
Figure 124.Test set up of Elitestek Evaluation Board with ADC for testing Deterministic Latency at 12.5Gbps

- One output of LMK is used for ADC input data generation which will be mapped on ADC0 input and other output is used as reference signal for checking deterministic latency on oscilloscope .

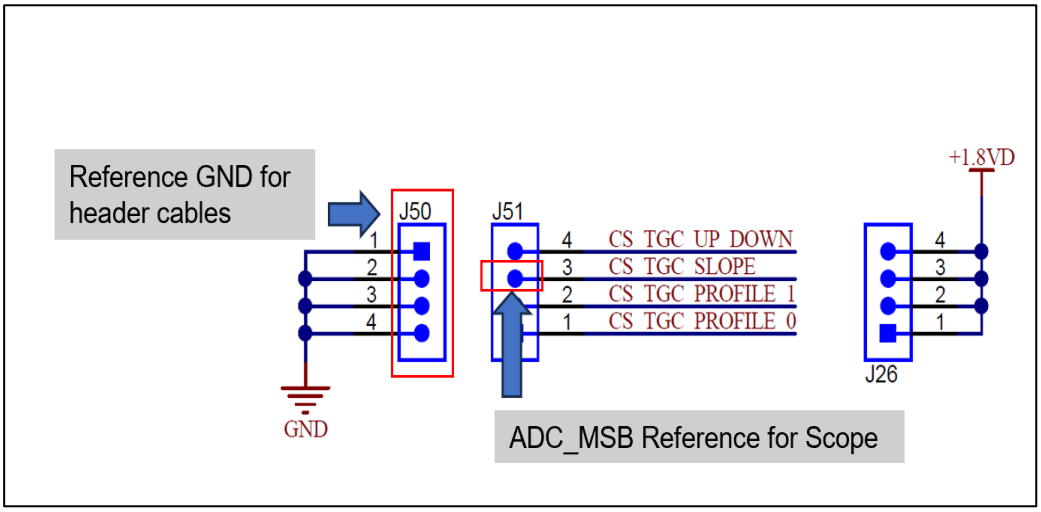
- The MSB bit of the output data is mapped to the GPIO, which is connected to another channel of the CRO.

10.2.2.1 Setup Details

- For reference input to ADC use J40 pin 5 as signal header of female header to SMA cable and pin 1 of connector J50 as GND header of female header to GPIO cable. SMA side of this cable will be mapped on the J6 connector on ADC Eval Board(this is ADC channel 0).



- For reference input to oscilloscope use J40 pin 6 as signal header of female header to SMA cable and pin 2 of connector J50 as GND (Enable 50ohm termination on the oscilloscope). This signal will be used as reference wave for the latency measurements.



- For ADC_MSB bit use J51 connector pin 3 as signal and pin 3 of connector J50 as GND(Enable 50ohm termination on the oscilloscope). This signal will be used as the captured data reference for latency measurements.

Note: The same setup can be used for 5 Gbps testing also, if we want to keep the setup for both 5 Gbps and 12.5 Gbps design the same. Just use the provided 5 Gbps MCS file on the FPGA and use the ADC config provided with the release 1.1.

10.2.3 Test Procedure

- Load the MCS provided 12.5 Gbps on the EVAL Board and then turn off the board.
- Configure the ADC board first with the given config file (JESD JESD 31.25MSPS_Subclass1.cfg) and then turn on the FPGA Eval board.
- Open tcl and run the script, once reset and configuration is done adjust cursors on the oscilloscope and check the rising edge to rising edge delay.

10.2.4 Test Cases

10.2.4.1 Test Case 0 : LMF = 148 (160X Mode)

10.2.4.1.1 Input Frequency = 2.44 MHz

Figure 125. Deterministic Latency capture between input square and ADC MSB bit at input frequency of 2.44 MHz

The green-colored waveform is the input square waveform, and the red-colored waveform is the MSB bit of the received data.

Deterministic latency in the path is in range of 233.4ns with variation of 150ps on every power cycle

Below table shows the Minimum, Typical and Maximum deterministic latency values including variation on cold and warm reset.

Reset Type	Mode	Min Value (ns)	Typical Value (ns)	Max Value (ns)	No. of Iterations	Variation (ps)
Cold	160X	233.32	233.4	233.47	30	150
Warm	160X	233.34	233.4	233.45	30	110

Table 52. Deterministic latency variation table for JESD204B RX testing with ADC at 12.5Gbps