CIS

Elitestek SLVS-EC RX Reference Design User Guide Ver.1.2

BOARD USED：TJ375N1156X DEVELOPMENT BOARD

CIS CORPORATION

Table of contents

Revision History

Rev.	Date of revision	Descriptions
1.0	12/20/2024	First Edition
1.1	1/27/2025	• Added Sensor Gain command to Table 2.4 • Corrected the description of the fmt command in Table 2.4 • Added "default" to the note in Table 2.4 • Added "Executing the command without parameters returns the current value." to section 2.4.
1.2	3/10/2025	• Changed Figure 1.1

1. Overview

In addition to the SLVS-EC Receiver IP (referred to as SLVS-EC RX), other components such as high-speed transceiver and sensor control logic are required to receive image data output from the image sensor in an FPGA. These functions are provided as a reference design and can be customized for your application. This document describes the evaluation system of SLVS-EC RX using the Elitestek evaluation board.

1.1. Evaluation system

As shown in Figure 1.1, the evaluation system consists of an evaluation board, a camera, a relay board that connects the camera and evaluation board, and a daughter card for HDMI output. The image signal output from the image sensor is input to the FPGA on the evaluation board via the relay board, processed by the reference design programmed in the FPGA, and then output to an external monitor via the HDMI connector. Some signals can be observed with an oscilloscope. The input and output signals of the SLVS-EC RX can also be observed using the Efinity Debugger. Table 1.1 shows the components of the evaluation system.

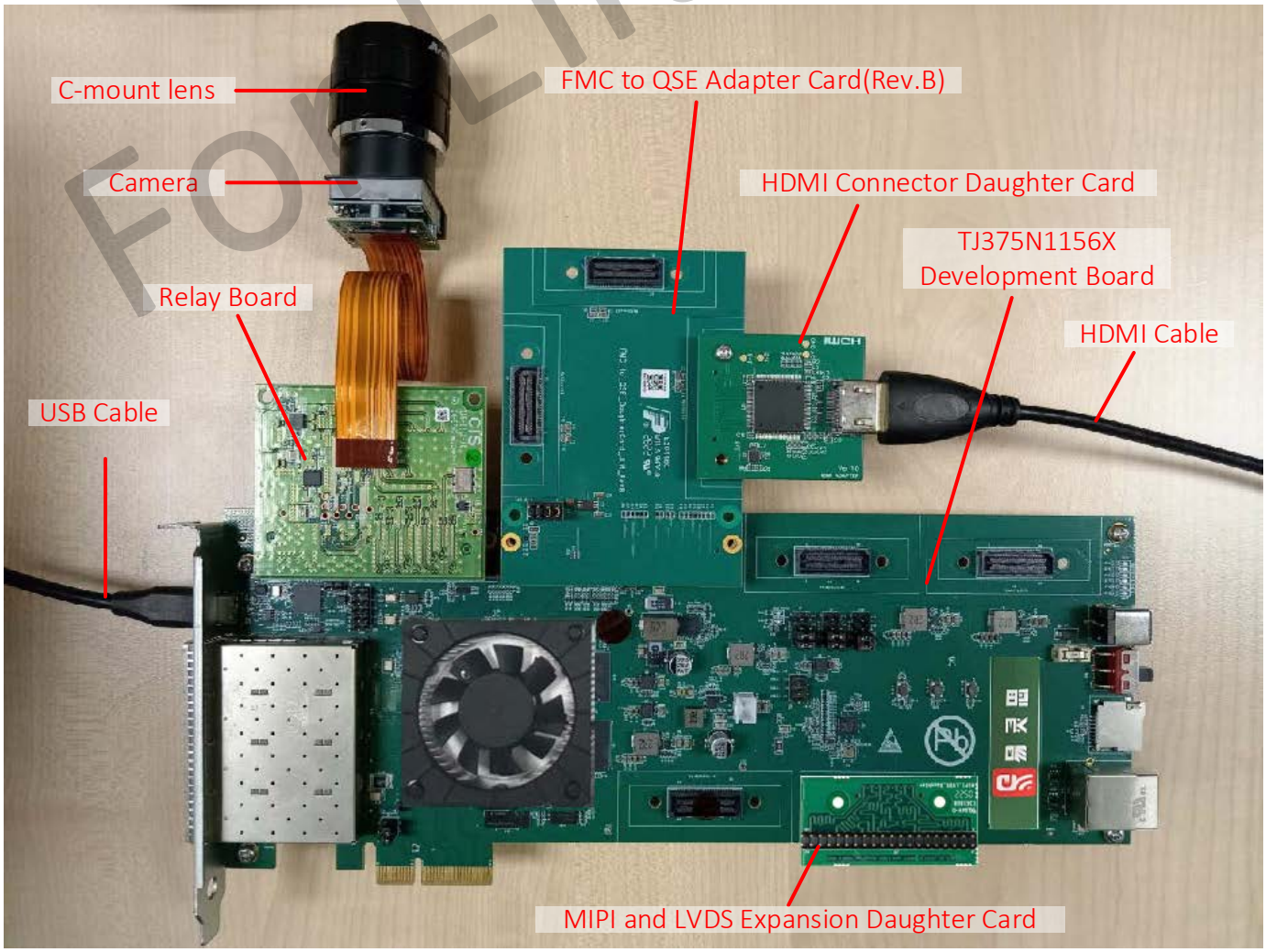

Figure 1.1 Evaluation system

Table 1.1 Components of the evaluation system[1]

No.	Components	Vendor	Note
1	DCC-5SLEC1R[2]	CIS	- SLVS-EC output camera - Image sensor is SONY IMX547 - Maximum number of lanes is 2 - Supported Bit depths are RAW8, 10, and 12 - Effective pixel count is 2472 x 2064 pixels - Lens mount is C-mount
2	Elitestek SLVS-EC Relay Board	CIS	- Relay board for connecting the camera and evaluation board - Connected to the FMC connector on the evaluation board
3	TJ375N1156X Development Board	Elitestek	- Evaluation board included in the TJ-Series TJ375N1156X development kit
4	FMC to QSE Adapter Card (Rev.B)	Elitestek	- Adapter to convert from FMC to QSE - Connect to the FMC connector on the evaluation board - Make sure to use Rev.B because Rev.C physically interferes with the relay board.
5	HDMI Connector Daughter Card	Elitestek	- Daughter card for HDMI output
6	MIPI and LVDS Expansion Daughter Card	Elitestek	- Daughter card for waveform observation
7	AC adaptor	Elitestek	- AC adaptor included with TJ-Series TJ375 N1156X development kit
8	USB Type-Cable	Elitestek	- USB cable included with TJ-Series TJ375 N1156X development kit
9	HDMI Cable	-	- HDMI cable which supports Full-HD and 60fps

[1] To purchase Component 1 and 2, please contact CIS Corporation. Component 3 to 9 must be prepared by the customer.

[2] Please prepare your own lenses.

1.2. Reference design

Figure 1.2 shows the block diagram of the reference design. Chapter 2 describes how to use the reference design, and Chapter 3 describes details of the design. Please refer to the documents provided by Elitestek for details of the high-speed transceiver and RISC-V included in this design. Table 1.2 shows the specifications of this reference design.

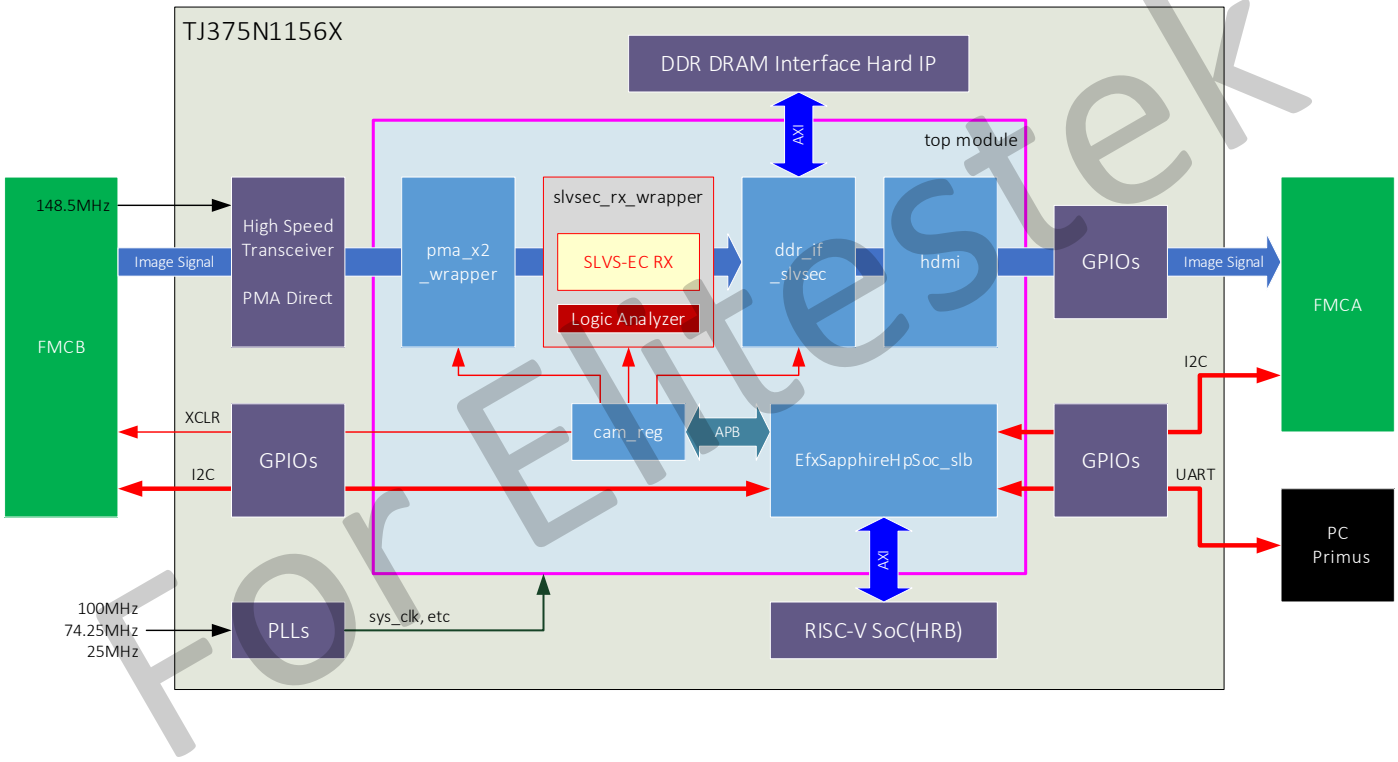

Figure 1.2 Block diagram of reference design

Table 1.2 Specifications for the reference design

Items	Descriptions	Notes
Developer	CIS Corporation	
IP to be evaluated	SLVS-EC RX	
Target board	TJ375N1156X Development Board	
Target device	TJ375N1156X	
FPGA Source code format	Verilog	
Firmware Format	bin	
Primus version	2024.2	
Transceiver Interface	PMA Direct Mode	
CPU	Hardened Sapphire RISC-V	
Hardware validation	Tested in the following modes: Number of lanes: 1, 2 Bit depth: 8, 10, 12 Sensor ROI: ON, OFF Error detection/correction: OFF, CRC, ECC	ECC has been checked for both 2-byte and 4-byte parity.

2. How to use the reference design

This chapter explains how to use the reference design.

2.1. Connecting hardware

The followings describe hardware connection procedure.

1. Connect the Elitestek SLVS-EC Relay Board to J15 (FMCB) of the TJ375N1156X Development Board.
2. Connect the DCC-5SLEC1R to CN2 of the Elitestek SLVS-EC Relay Board.
3. Connect the MIPI and LVDS Expansion Daughter Card to P1 of the TJ375N1156X Development Board (only if you want to observe the waveforms with an oscilloscope).
4. Connect USB1 of the Ti375N1156 Development Board to the PC with a USB Type-C cable.
5. Connect the AC adapter to J1 of the TJ375N1156X Development Board.
6. Set the jumpers according to Table 2.1. SD card slot is not used in this design.

Table 2.1 Jumper settings

Header	Connection	Description
J3	N.C.	VADJ=1.8V
J6	5 and 6 7 and 8	VCCIO_QSE=3.3V
J7	5 and 6 7 and 8	VCCIO_MIPI=1.2V
J18	5 and 6 7 and 8	VCCIO_BL0=3.3V

The following steps should be taken after programming the reference design in Section 2.2.

7. Connect the FMC to QSE Adapter Card (Rev.B) to J14 on the TJ375N1156X Development Board.
8. Connect the HDMI Connector Daughter Card to J1 on the FMC to QSE Adapter Card (Rev.B).
9. Connect the HDMI Connector Daughter Card to an external monitor with an HDMI cable.

Please note that the Efinity Programmer and Debugger cannot be used with the FMC to QSE Adapter Card inserted into the TJ375N1156X Development Board. Please remove the FMC to QSE Adapter Card to use the Programmer and Debugger.

2.2. Programming and starting the reference design

To use the TJ375N1156X Development Board, the USB driver must be installed in advance. For installation instructions, please refer to the TJ375N1156X Development Board User Guide. After installing the USB driver, follow the steps below to program and start the reference design.

1. Start Primus2024.2 and open the reference design project.
2. Turn on the power to the TJ375N1156X Development Board.
3. Make sure that nothing is connected to J14 and start the Efinity Programmer.
4. Set the Programming Mode to “SPI Active using JTAG Bridge(new)”.
5. Select the following Bitstream file.
   (project folder)¥Bitstream¥Combine¥slvsec_rx_rd_cmb_with_ECC.hex (with ECC)
   This is an image file that combines FPGA and FW.
6. Click the “Start Program” button to execute the program.
7. After completion of programming, turn off the power to the evaluation board.
8. If necessary, take steps 7 to 9 in section 2.1 and turn on the power to the external monitor.
9. Turn on the power to the evaluation board.
10. If the transceiver is successfully initialized, both red LEDs light up. If they do not light up, check the connections of the relay board and camera.
11. If you took step 8, check that an image is displayed on the external monitor. If not, check the connections of the FMC to QSE Adapter Card, HDMI Connector Daughter Card, and HDMI cable.
12. Open the serial communications software, press enter, and if the prompt $ is displayed, command control is enabled.

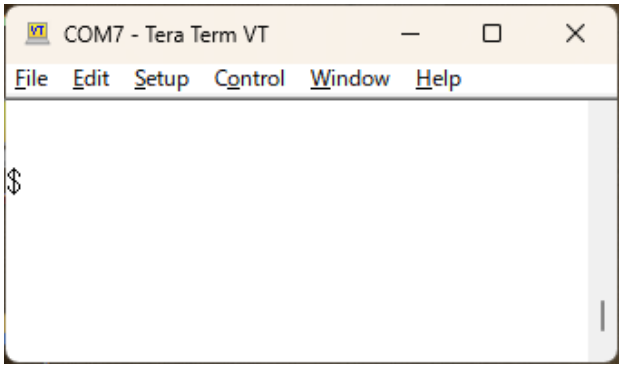

Figure 2.2 Step 12

2.3. Checking the operation of SLVS-EC RX using the Debugger

The waveforms of the input and output signals of SLVS-EC RX can be dumped using the Efinity Debugger. For further information on how to use the Debugger and how to display waveforms, please refer to the documents provided by Elitestek. Table 2.3 shows the signals input to the logic analyzer debug core.

Table 2.3 Logic Analyzer Debug Core Input Signals

Signal Name	Width	Description
i_rxdata0	20	Lane 0 Received Data
i_rxdata1	20	Lane 1 Received Data
rxdata0_pcs	16	Lane 0 PCS Output Data
rxdata1_pcs	16	Lane 1 PCS Output Data
rxcharisk0_pcs	2	Lane 0 PCS Output K Character
rxcharisk1_pcs	2	Lane 0 PCS Output K Character
o_data0	16	Output Pixel Data 0
o_data1	16	Output Pixel Data 1
o_data2	16	Output Pixel Data 2
o_data3	16	Output Pixel Data 3
o_lval	1	LVAL
o_dval	1	DVAL
o_frame_start	1	FRAME START
o_frame_end	1	FRAME END
o_line_valid	1	LINE VALID
o_line_number	13	LINE NUMBER
o_ebd_line	1	EBD LINE
o_data_id	4	DATA ID
o_info_type	3	INFO TYPE
o_info	24	INFO
o_hcrc_err	1	Packet header CRC error
o_pcrc_err	1	Payload CRC error
o_deskew_done	2	Deskew done flag
o_dbg_phy_sync	2	PHY SYNC detected (lanes 0-1)
o_dbg_phy_deskew	2	PHY DESKWEW detected (lanes 0-1)
o_dbg_phy_standby	2	PHY STANDBY detected (lanes 0-1)
o_dbg_phy_rxstart	2	PHY RXSTART detected (lanes 0-1)
o_dbg_phy_rxend	2	PHY RXEND detected (lanes 0-1)
o_dbg_phy_rxdval	2	PHY RXDVAL detected (lanes 0-1)

2.4. Control Commands

The reference design can be controlled using serial communications software. Set up the serial communications software as follows. Table 2.4 shows a list of commands.

Baud Rate : 115200
Data : 8bit
Parity : None
Stop Bit : 1bit
Flow Control : None

Table 2.4 Control Command List

Category	Command	Parameter 1	Parameter 2	Description	Note
Format	fmt	1	8	1lane 8bit	
			10	1lane 10bit	
			12	1lane 12bit	
		2	8	2lane 8bit	default
			10	2lane 10bit	
			12	2lane 12bit	
CRC/ECC	ecc	0		CRC=OFF, ECC=OFF	default
		1		CRC=ON, ECC=OFF	
		2		CRC=OFF, ECC=ON	2byte parity
		3		CRC=OFF, ECC=ON	4byte parity
Sensor ROI	roi	0		2472 x 2064	OFF (default)
		1		1920 x 1080	ON
Sensor Gain	gain	N		Gain=N[dB]	N=0 to 48 (default=18)
control register write	w	Address	Data	Write to the control register (cam_reg)	
control register read	r	Address		Read from the control register (cam_reg)	

[Example]

Switching format to 1lane10 bit : fmt 1 10
Switching to 4byte parity ECC : ecc 3
Turning on the sensor ROI : roi 1
Setting the sensor gain to 12dB : gain 12
Writing to the control register (cam_reg) : w 0x0004 0x0001

Executing the command without parameters returns the current value.

2.5. Control Register

Table 2.5 shows the address map of the control register (cam_reg) in the FPGA. In general, these registers are automatically set by the firmware when a control command is executed. As an exception, changing the trimming start position in the memory controller requires rewriting the DDR_XSTAT and DDR_YSTAT registers.

Table 2.5 Address map of control registers

Address	Register name	Width	Range	R/W	Init	Note
0x0000	IP_VERSION	8	[7:0]	R	0x00	Version of SLVS-EC RX
0x0004	PMA_STATE	8	[7:0]	R	0x00	PMA Status [2:0]: Lane0(0x5=Init Done) [6:4]: Lane1(0x5=Init Done)
0x0008	PHY_RSTN	2	[1:0]	RW	0x0	PHY Reset（Active Low） [0]: Lane0, [1]: Lane1
0x000c	PCS_RSTN	2	[1:0]	RW	0x0	PCS Reset（Active Low） [0]: Lane0, [1]: Lane1
0x0010	IMS_XCLR	1	[0]	RW	0x0	Sensor reset（Active Low）
0x0014	DESKEW_DONE	2	[1:0]	R	0x0	Deskew Done flag（Active High） [0]: Lane0, [1]: Lane1
0x0100	LANE_SEL	3	[2:0]	RW	0x0	Number of lanes 0: 1-lane, 1: 2-lane
0x0104	BIT_SEL	3	[2:0]	RW	0x0	Bit depth 0: 8-bit,　1: 10-bit,　2: 12-bit
0x0108	IMG_XSIZE	12	[11:0]	RW	0x908	Number of horizontal pixels
0x010c	IMG_YSIZE	12	[11:0]	RW	0x810	Number of vertical pixels
0x0110	ERR_HANDLING	2	[1:0]	RW	0x0	Error detection, correction ON/OFF 0: OFF 1: CRC ON 2: ECC ON (2byte parity), 3: ECC ON (4byte parity)
0x0114	ECC_TEST0	8	[7:0]	RW	0x00	ECC test register
0x0118	ECC_TEST1	8	[7:0]	RW	0x00	ECC test register
0x011c	ECC_DIS	1	[0]	RW	0x0	ECC test register
0x0200	DDR_XSTAT	12	[11:0]	RW	0x114	Horizontal start position of trimming
0x0204	DDR_YSTAT	12	[11:0]	RW	0x1ec	Vertical start position of trimming
0x0300	FMCA_PRSNT	1	[0]	R	-	FMCA PRSNT signal level

2.6. Combining FPGA and Firmware

Firmware is provided as a .bin file and cannot be changed. If the FPGA logic has been changed, combine the new FPGA bitstream with the FW and implement the program. The merging procedure is as follows.

1. Open “Combine Multiple Image Files” from Efinity Programmer.
2. Set Mode to “Generic Image Combination”.
3. Set Output File and Output Directory.
4. Click the “Add Image” button to add the FPGA bitstream and FW.
   FW: (project folder)¥Bitstream¥FW¥slvsec_rx.bin
5. Set the Flash Address as follows.
   FPGA : 0x00000000
   FW : 0x00800000
6. Click the “Apply” button to generate the combined bitstream.

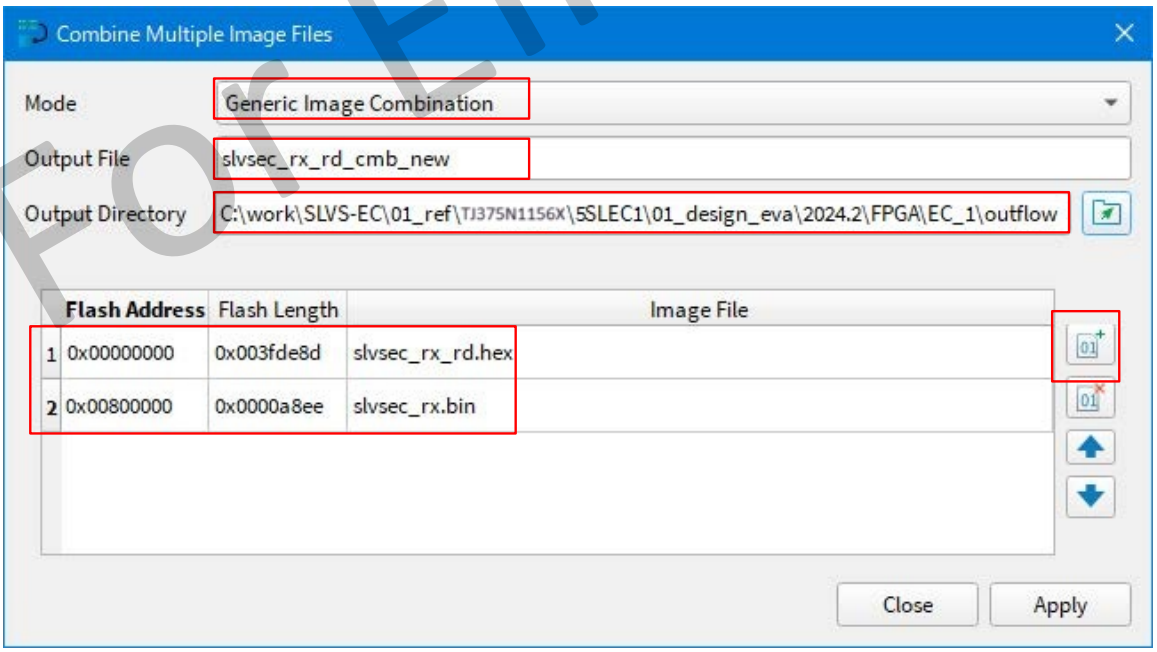

Figure 2.6 Combination of FPGA and FW

3. Reference Design Details

This chapter describes the details of the reference design.

3.1. Top-level Ports

Table 3.1 shows the list of top-level ports of the reference design.

Table 3.1 List of top-level ports (Part 1)

No.	Signal Name	Width	I/O	Description
High Speed Transceiver Interface				
1	IN_USER	1	I	User status
2	RAW_SERDES_TX_CLK	1	I	TX clock
3	RAW_SERDES_RX_CLK	1	I	RX clock
4	DP0_TXD	64	O	Lane 0 TX data (all 0)
5	DP0_RXD	64	I	Lane 0 RX data (lower 20 bits enabled)
6	DP0_PCS_RST_N_TX	1	O	Lane 0 PCS TX reset (Active Low)
7	DP0_PCS_RST_N_RX	1	O	Lane 0 PCS RX reset (Active Low)
8	DP0_PHY_RESET_N	1	O	Lane 0 PHY reset (Active Low)
9	DP0_PMA_TX_ELEC_IDLE	1	O	Lane 0 electrical idle
10	DP0_PMA_XCVR_PLLCLK_EN	1	O	Lane 0 PLL clock enable
11	DP0_PMA_XCVR_PLLCLK_EN_ACK	1	I	Lane 0 PLL clock enable ACK
12	DP0_PMA_XCVR_POWER_STATE_REQ	4	O	Lane 0 power state request
13	DP0_PMA_XCVR_POWER_STATE_ACK	4	I	Lane 0 power state request ACK
14	DP0_PMA_RX_SIGNAL_DETECT	1	I	Lane 0 receiver signal detected
15	DP0_PHY_INTERRUPT	1	I	Lane 0 PHY error & status
16	DP1_TXD	64	O	Lane 1 TX data (all 0)
17	DP1_RXD	64	I	Lane 1 RX data (lower 20 bits valid)
18	DP1_PCS_RST_N_TX	1	O	Lane 1 PCS TX reset (Active Low)
19	DP1_PCS_RST_N_RX	1	O	Lane 1 PCS RX reset (Active Low)
20	DP1_PHY_RESET_N	1	O	Lane 1 PHY reset (Active Low)
21	DP1_PMA_TX_ELEC_IDLE	1	O	Lane 1 electrical idle
22	DP1_PMA_XCVR_PLLCLK_EN	1	O	Lane 1 PLL clock enable
23	DP1_PMA_XCVR_PLLCLK_EN_ACK	1	I	Lane 1 PLL clock enable ACK
24	DP1_PMA_XCVR_POWER_STATE_REQ	4	O	Lane 1 power state request
25	DP1_PMA_XCVR_POWER_STATE_ACK	4	I	Lane 1 power state request ACK
26	DP1_PMA_RX_SIGNAL_DETECT	1	I	Lane 1 receiver signal detected
27	DP1_PHY_INTERRUPT	1	I	Lane 1 PHY error & status
28	Q2_PMA_CMN_READY	1	I	PHY ready status

Table 3.1 List of top-level ports (Part 2)

No.	Signal Name	Width	I/O	Description
Image Sensor Control Interface				
29	o_ims_xclr	1	O	Sensor reset (Active Low)
30	i_ims_xvs	1	I	Vertical sync signal
31	i_ims_xhs	1	I	Horizontal sync signal
32	o_ims_xce	1	O	4-wire serial I/F XCE (unused)
33	i_ims_sdo	1	I	4-wire serial I/F SDO (unused)
34	o_ims_xmaster	1	O	Master/Slave switch (Low: Master Mode)
35	o_ims_xtrig1	1	O	Trigger input 1 (unused)
36	o_ims_xtrig2	1	O	Trigger input 2 (unused)
37	i_ims_tout0	1	I	Pulse output 0 (unused)
38	i_ims_tout1	1	I	Pulse output 1 (unused)
39	i_ims_tout2	1	I	Pulse output 2 (unused)
40	o_ims_omode	1	O	SLVS-EC/SLVS switch (High: SLVS-EC)
41	o_ims_slamode0	1	O	I2C slave address selection 0
42	o_ims_slamode1	1	O	I2C slave address selection 1
43	o_ims_slamode2	1	O	I2C slave address selection 2
44	io_ims_i2c_scl_in	1	I	Sensor I2C SCL input
45	io_ims_i2c_scl_out	1	O	Sensor I2C SCL output
46	io_ims_i2c_scl_oe	1	O	Sensor I2C SCL output enable
47	io_ims_i2c_sda_in	1	I	Sensor I2C SDA input
48	io_ims_i2c_sda_out	1	O	Sensor I2C SDA output
49	io_ims_i2c_sda_oe	1	O	Sensor I2C SDA output enable
Memory Interface				
50	soc_ddr_inst1_ARSTN_0	1	O	ARSTN
51	soc_ddr_inst1_AWREADY_0	1	I	AWREADY
52	soc_ddr_inst1_AWADDR_0	33	O	AWADDR
53	soc_ddr_inst1_AWVALID_0	1	O	AWVALID
54	soc_ddr_inst1_AWBURST_0	2	O	AWBURST
55	soc_ddr_inst1_AWID_0	6	O	AWID
56	soc_ddr_inst1_AWLEN_0	8	O	AWLEN
57	soc_ddr_inst1_AWLOCK_0	1	O	AWLOCK
58	soc_ddr_inst1_AWSIZE_0	3	O	AWSIZE
59	soc_ddr_inst1_AWCACHE_0	4	O	AWCACHE
60	soc_ddr_inst1_AWQOS_0	1	O	AWQOS
61	soc_ddr_inst1_AWALLSTRB_0	1	O	AWALLSTRB
62	soc_ddr_inst1_AWAPCMD_0	1	O	AWAPCMD
63	soc_ddr_inst1_AWCOBUF_0	1	O	AWCOBUF
64	soc_ddr_inst1_ARREADY_0	1	I	ARREADY
65	soc_ddr_inst1_ARADDR_0	33	O	ARADDR

Table 3.1 List of top-level ports (Part 3)

No.	Signal Name	Width	I/O	Description
66	soc_ddr_inst1_ARVALID_0	1	O	ARVALID
67	soc_ddr_inst1_ARBURST_0	2	O	ARBURST
68	soc_ddr_inst1_ARID_0	6	O	ARID
69	soc_ddr_inst1_ARLEN_0	8	O	ARLEN
70	soc_ddr_inst1_ARLOCK_0	1	O	ARLOCK
71	soc_ddr_inst1_ARSIZE_0	3	O	ARSIZE
72	soc_ddr_inst1_ARQOS_0	1	O	ARQOS
73	soc_ddr_inst1_ARAPCMD_0	1	O	ARAPCMD
74	soc_ddr_inst1_WREADY_0	1	I	WREADY
75	soc_ddr_inst1_WLAST_0	1	O	WLAST
76	soc_ddr_inst1_WVALID_0	1	O	WVALID
77	soc_ddr_inst1_WDATA_0	512	O	WDATA
78	soc_ddr_inst1_WSTRB_0	64	O	WSTRB
79	soc_ddr_inst1_BID_0	6	I	BID
80	soc_ddr_inst1_BVALID_0	1	I	BVALID
81	soc_ddr_inst1_BRESP_0	2	I	BRESP
82	soc_ddr_inst1_BREADY_0	1	O	BREADY
83	soc_ddr_inst1_RDATA_0	512	I	RDATA
84	soc_ddr_inst1_RID_0	6	I	RID
85	soc_ddr_inst1_RVALID_0	1	I	RVALID
86	soc_ddr_inst1_RLAST_0	1	I	RLAST
87	soc_ddr_inst1_RRESP_0	2	I	RRESP
88	soc_ddr_inst1_RREADY_0	1	O	RREADY
HDMI Interface				
89	i_hdmi_locked	1	I	HDMI Clock PLL Lock
90	i_hdmi_clk	1	I	HDMI Clock
91	o_hdmi_vsync	1	O	HDMI Vertical Sync Signal
92	o_hdmi_hsync	1	O	HDMI Horizontal Sync Signal
93	o_hdmi_de	1	O	HDMI Data Enable
94	o_hdmi_data	16	O	HDMI Data
95	o_hdmi_spdif_clk	1	O	HDMI SPDIF Clock
96	o_hdmi_spdif	1	O	HDMI SPDIF
97	i_hdmi_int	1	I	HDMI Interrupt
98	io_hdmi_i2c_scl_in	1	I	Sensor I2C SCL Input
99	io_hdmi_i2c_scl_out	1	O	Sensor I2C SCL Output
100	io_hdmi_i2c_scl_oe	1	O	Sensor I2C SCL Output Enable
101	io_hdmi_i2c_sda_in	1	I	Sensor I2C SDA Input
102	io_hdmi_i2c_sda_out	1	O	Sensor I2C SDA Output
103	io_hdmi_i2c_sda_oe	1	O	Sensor I2C SDA Output Enable

Table 3.1 List of top-level ports (Part 4)

No.	Signal Name	Width	I/O	Description
CPU(RISC-V)				
104	io_jtag_tdi	1	O	Soft JTAG TDI (CPU)
105	io_jtag_tdo	1	I	Soft JTAG TDO (CPU)
106	io_jtag_tms	1	O	Soft JTAG TMS (CPU)
107	pin_io_jtag_tdi	1	I	Soft JTAG TDI (External pin)
108	pin_io_jtag_tdo	1	O	Soft JTAG TDO (External pin)
109	pin_io_jtag_tms	1	I	Soft JTAG TMS (External pin)
110	userInterruptA	1	O	Interrupt
111	userInterruptB	1	O	Interrupt
112	userInterruptC	1	O	Interrupt
113	userInterruptD	1	O	Interrupt
114	userInterruptE	1	O	Interrupt
115	userInterruptF	1	O	Interrupt
116	userInterruptG	1	O	Interrupt
117	userInterruptH	1	O	Interrupt
118	o_uart_txd	1	O	UART TXD
119	i_uart_rxd	1	I	UART RXD
120	o_system_spi_sclk	1	O	SPI Clock
121	o_system_spi_ss	1	O	SPI Chip Select
122	io_system_spi_data_0_in	1	I	SPI Data 0 Input
123	io_system_spi_data_0_out	1	O	SPI Data 0 Output
124	io_system_spi_data_0_oe	1	O	SPI Data 0 Output Enable
125	io_system_spi_data_1_in	1	I	SPI Data 1 Input
126	io_system_spi_data_1_out	1	O	SPI Data 1 Output
127	io_system_spi_data_1_oe	1	O	SPI Data 1 Output Enable
128	axiA_awaddr	I	32	AXI Slave AWADDR
129	axiA_awlen	I	8	AXI Slave AWLEN
130	axiA_awsize	I	3	AXI Slave AWSIZE
131	axiA_awburst	I	2	AXI Slave AWBURST
132	axiA_awlock	I	1	AXI Slave AWLOCK
133	axiA_awcache	I	4	AXI Slave AWCACHE
134	axiA_awprot	I	3	AXI Slave AWPROT
135	axiA_awqos	I	4	AXI Slave AWQOS
136	axiA_awregion	I	4	AXI Slave AWFREGION
137	axiA_awvalid	I	1	AXI Slave AWVALID
138	axiA_awready	O	1	AXI Slave AWREADY
139	axiA_wdata	I	32	AXI Slave WDATA
140	axiA_wstrb	I	4	AXI Slave WSTRT
141	axiA_wvalid	I	1	AXI Slave WVALID

Table 3.1 List of top-level ports (Part 5)

No.	Signal Name	Width	I/O	Description
142	axiA_wlast	I	1	AXI Slave WLAST
143	axiA_wready	O	1	AXI Slave WREADY
144	axiA_bresp	O	2	AXI Slave BRESP
145	axiA_bvalid	O	1	AXI Slave BVALID
146	axiA_bready	I	1	AXI Slave BREADY
147	axiA_araddr	I	32	AXI Slave ARADDR
148	axiA_arlen	I	8	AXI Slave ARLEN
149	axiA_arsize	I	3	AXI Slave ARSIZE
150	axiA_arburst	I	2	AXI Slave ARBURST
151	axiA_arlock	I	1	AXI Slave ARLOCK
152	axiA_arcache	I	4	AXI Slave ARCACHE
153	axiA_arprot	I	3	AXI Slave ARPROT
154	axiA_arqos	I	4	AXI Slave ARQOS
155	axiA_arregion	I	4	AXI Slave ARREGION
156	axiA_arvalid	I	1	AXI Slave ARVALID
157	axiA_arready	O	1	AXI Slave ARREADY
158	axiA_rdata	O	32	AXI Slave RDATA
159	axiA_rresp	O	2	AXI Slave RRESP
160	axiA_rlast	O	1	AXI Slave RLAST
161	axiA_rvalid	O	1	AXI Slave RVALID
162	axiA_rready	I	1	AXI Slave RREADY
163	axiAInterrupt	O	1	AXI Slave Interrupt
164	cfg_done	I	1	Config Done
165	cfg_start	O	1	Config Start
166	cfg_sel	O	1	Config Select
167	cfg_reset	O	1	Config Reset
168	io_peripheralClk	I	1	Peripheral clock
169	io_peripheralReset	I	1	Peripheral reset
170	io_asyncReset	O	1	Asynchronous reset
171	io_gpio_sw_n	I	1	GPIO SW
172	pll_peripheral_locked	I	1	Peripheral clock PLL lock
173	pll_system_locked	I	1	System clock PLL lock
Others				
174	i_fmca_prsnt	I	1	FMCA PRSNT Signal
175	o_led_g	O	4	LED (Green)
176	o_led_r	O	2	LED (Red)
177	o12_tp	O	10	Test Pads (1.2V)
178	o33_tp	O	6	Test Pads (3.3V)

3.2. High-Speed Transceiver Interface

Figure 3.2 shows the block diagram of the high-speed transceiver interface. This reference design uses PMA direct mode. The transceiver is initialized by the sequencer included in pma_x2_wrapper in this diagram. When initialization is complete, the receive clock and receive data output from the transceiver are enabled, and the lower 20 bits of each lane are passed to the downstream SLVS-EC RX.

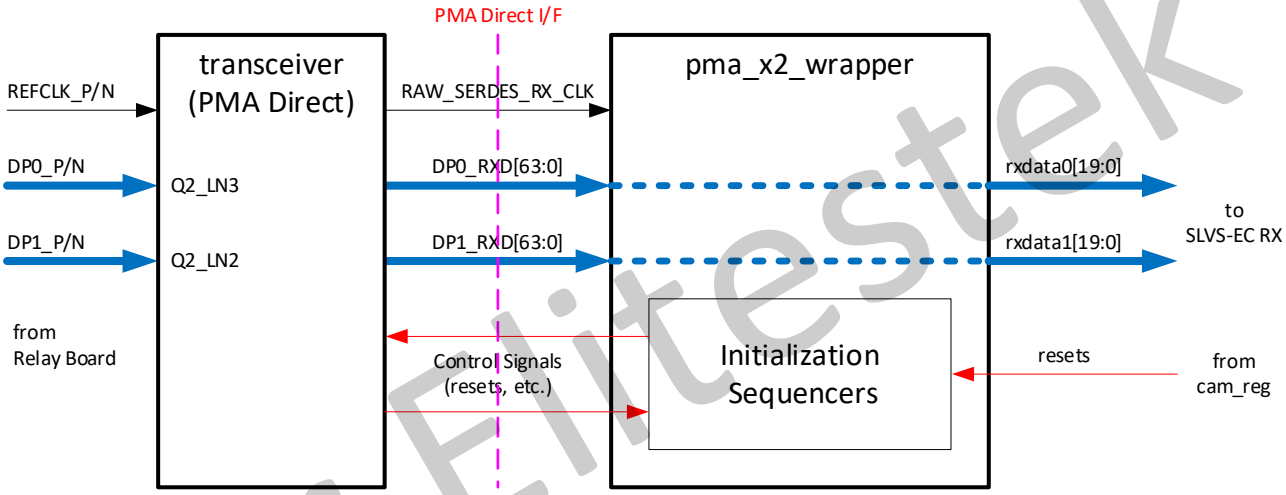

Figure 3.2 Block diagram of the high-speed transceiver interface

3.3. Image sensor control interface

Table 3.3 shows the control signals for the image sensor used in the reference design.

Table 3.3 Image sensor control signals

Signal Name	Control
o_ims_xclr	Controlled by control register
o_ims_xmaster	Low fixed
o_ims_omode	High fixed
o_ims_slamode0	Low fixed
o_ims_slamode1	Low fixed
o_ims_slamode2	Low fixed
io_ims_i2c_scl_in	Controlled by CPU
io_ims_i2c_scl_out	Controlled by CPU
io_ims_i2c_scl_oe	Controlled by CPU
io_ims_i2c_sda_in	Controlled by CPU
io_ims_i2c_sda_out	Controlled by CPU
io_ims_i2c_sda_oe	Controlled by CPU

3.4. SLVS-EC RX Wrapper

Figure 3.4 shows the block diagram of the SLVS-EC RX Wrapper, and Table 3.4 shows the parameter settings. SLVS-EC RX is controlled with the control register. In this design, the Efinity Debugger is also configured, and the SLVS-EC RX input/output signals are input to the logic analyzer debug core.

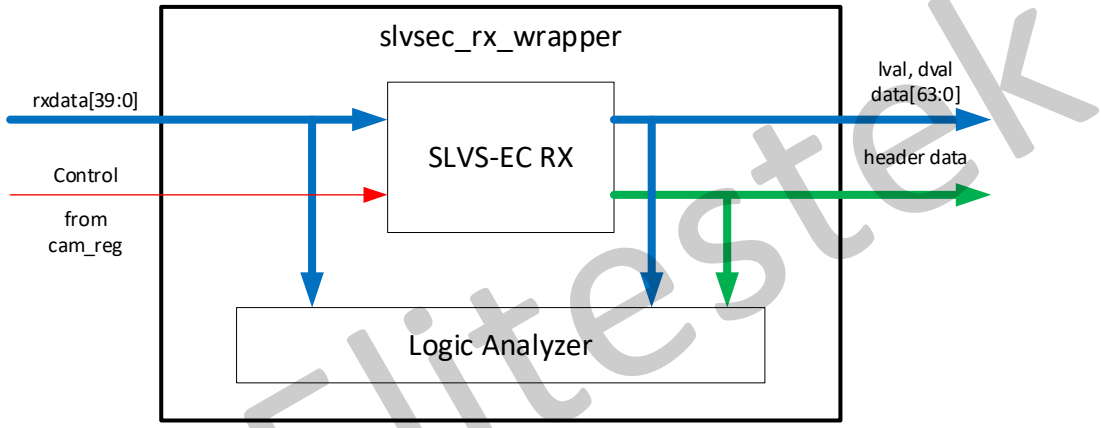

Figure 3.4 SLVS-EC RX Wrapper

Table 3.4 SLVS-EC RX Wrapper parameter settings

No.	Parameter	Setting	Description
1	MAX_LANE_NUM	2	Maximum number of transceiver lanes
2	MASTER_LANE	0	Master lane number
3	ERR_CORRECTION	0 or 1	0: without ECC, 1: with ECC
4	MAX_IMG_XSIZE	2472	Maximum image width

3.5. Memory Interface

Figure 3.5 shows the block diagram of the memory interface. The 2472x2064 pixel image data output from the SLVS-EC RX is trimmed to 1920x1080 in the memory controller. The start position of the trimming can be changed by the control register. The trimmed image data is written to the LPDDR4 memory via the DDR DRAM Interface Hard IP. In this design, 16 frames can be written to the LPDDR4. The data read from the LPDDR4 is connected to the HDMI interface. The interface between the memory controller and the DDR DRAM Interface Hard IP is AXI4.

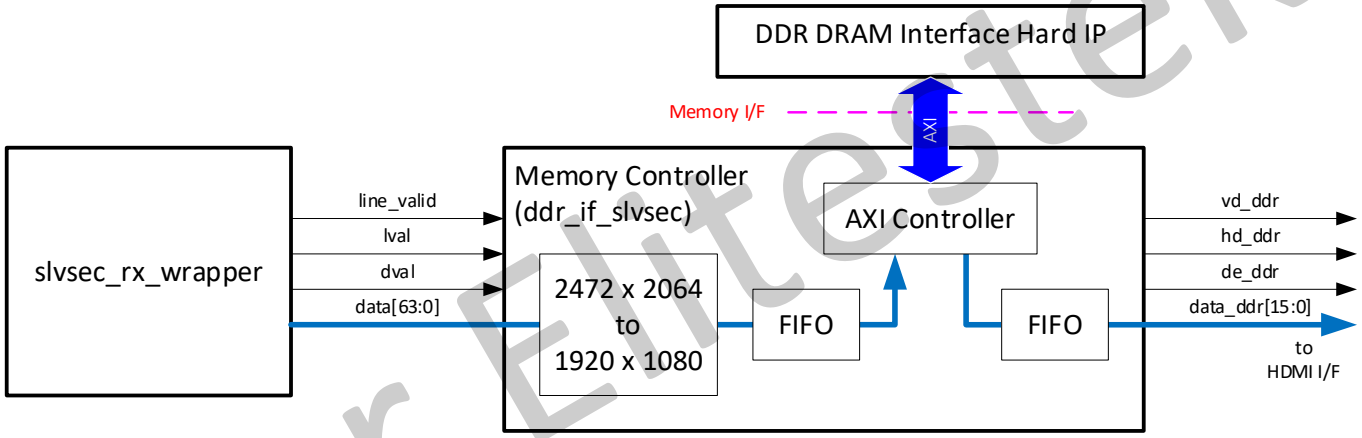

Figure 3.5 Memory Interface

Table 3.5 shows the write and read frame rates for each sensor operation mode. Normally, the write and read frame rates are matched, but this design writes at the maximum frame rate of the sensor and always reads at 60 fps, so that the write and read frame rates are different. Please note that this results in frame skipping or read of the same frame depending on the mode of operation.

Table 3.5 Frame rates for each operation mode

Lanes	Depth	Write Frame Rate [fps]	Read Frame Rate [fps]
1	8	80.3	60.0
1	10	64.8	
1	12	54.2	
2	8	122.9	
2	10	122.2	
2	12	82.4	

3.6. HDMI Interface

Figure 3.6 shows the HDMI interface. This reference design uses the FMC to QSE Adapter Card and the HDMI Connector Daughter Card to output images to an external monitor. The image output from the sensor is a Bayer pattern, but this design outputs it as a monochrome image. I2C is used to access the registers of the HDMI PHY chip.

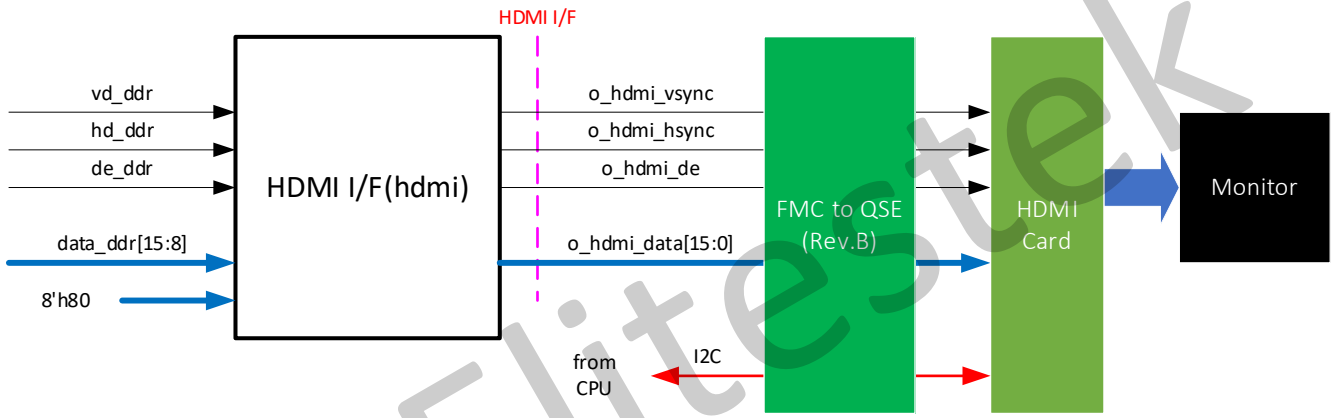

Figure 3.6 HDMI interface

3.7. CPU Block

Figure 3.7 shows a block diagram of the CPU block, and Table 3.7 shows an overview of each block. The CPU consists of a hardened RISC-V SoC block (HRB) and a soft logic block (SLB). The HRB and SLB are connected by an AXI bus. For further details on the CPU, please refer to the documents provided by Elitestek.

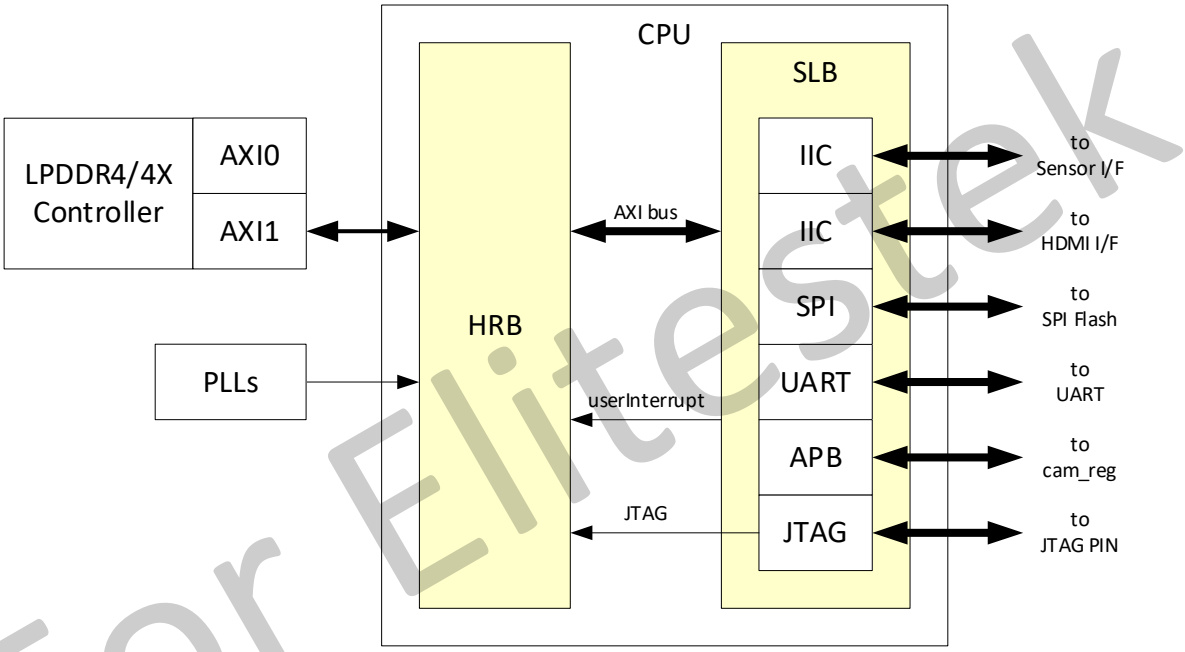

Figure 3.7 CPU block

Table 3.7 Overview of the CPU block

Block		Overview
HRB		Hardened RISC-V SoC block
SLB	IIC	To control the image sensor and HDMI PHY chip.
	SPI	To access the SPI flash memory.
	UART	To communicate with a PC.
	APB	To access the control register in the FPGA. For details on the control register, refer to Section 3.7.
	JTAG	For debugging firmware.
LPDDR4/4X Controller		External LPDDR4 memory controller. Connected to the AXI1 side from the HRB.
PLLs		PLL for the system clock and peripheral clock.

3.8. Debugging Signals

This reference design can output some signals to the LEDs on the evaluation board and the MIPI and LVDS Expansion Daughter Card. Connect the MIPI and LVDS Expansion Daughter Card to P1 (QSE3) on the evaluation board. Table 3.8.1 shows the LED pin assignments, and Table 3.8.2 shows the MIPI and LVDS Expansion Daughter Card pin assignments.

Table 3.8.1 LED pin assignments

LED	Signal Name	Assignment
LED1	o_led_g[0]	Number of Lanes
LED2	o_led_g[1]	00: 1-lane, 01: 2-lane
LED3	o_led_g[2]	Bit Depth
LED4	o_led_g[3]	00: 8-bit, 01: 10-bit, 10: 12-bit
LED5	o_led_r[0]	Lane 0 transceiver initialization done
LED6	o_led_r[1]	Lane 1 transceiver initialization done

Table 3.8.2 MIPI and LVDS Expansion Daughter Card pin assignment

Pin No.	Signal Name	Assignment	Description
2	o12_tp[0]	i_ims_xvs	Image sensor vertical sync signal
4	o12_tp[1]	i_ims_xhs	Image sensor horizontal sync signal
8	o12_tp[2]	frame_start	FRAME START
10	o12_tp[3]	ebd_line	EBD LINE
14	o12_tp[4]	line_valid	LINE VALID
16	o12_tp[5]	frame_end	FRAME END
20	o12_tp[6]	lval	LVAL
22	o12_tp[7]	dval	DVAL
26	o12_tp[8]	hcrc_err	Header CRC error
28	o12_tp[9]	pcrc_err	Payload CRC error
32	o33_tp[2]	dbg_phy_sync	PHY SYNC detected (lanes 0-1 OR)
34	o33_tp[3]	dbg_phy_standby	PHY STANDBY detected (lanes 0-1 OR)
37	o33_tp[0]	dbg_phy_deskew	PHY DESKEW detected (lanes 0-1 OR)
38	o33_tp[4]	dbg_phy_rxstart	PHY RXSTART detected (lanes 0-1 OR)
39	o33_tp[1]	dbg_phy_rxdval	PHY RXDVAL detected (lanes 0-1 OR)
40	o33_tp[5]	dbg_phy_rxend	PHY RXEND detected (lanes 0-1 OR)

3.9. FMC Pin assignment of Relay board

Table 3.9 shows the FMC pin assignment of the relay board. For details, refer to the relay board schematics.

Table 3.9 FPC Pin assignment of relay board (Part 1)

FMC Pin No.	Board Signal Name	FPGA Pin No.	Reference Design Signal Name
A1	GND		
A2	FMCB_DP1_M2C_P	A22	DP1_p
A3	FMCB_DP1_M2C_N	B22	DP1_n
A4	GND		
A5	GND		
A6	FMCB_DP2_M2C_P	A20	
A7	FMCB_DP2_M2C_N	B20	
A8	GND		
A9	GND		
A10	FMCB_DP3_M2C_P	A18	
A11	FMCB_DP3_M2C_N	B18	
A12	GND		
A13	GND		
A14	N.C.		
A15	N.C.		
A16	GND		
A17	GND		
A18	N.C.		
A19	N.C.		
A20	GND		
A21	GND		
A22	FMCB_DP1_C2M_P	C21	
A23	FMCB_DP1_C2M_N	D21	
A24	GND		
A25	GND		
A26	FMCB_DP2_C2M_P	C19	
A27	FMCB_DP2_C2M_N	D19	
A28	GND		
A29	GND		
A30	FMCB_DP3_C2M_P	C17	
A31	FMCB_DP3_C2M_N	D17	
A32	GND		
A33	GND		
A34	N.C.		
A35	N.C.		

Table 3.9 FPC Pin assignment of relay board (Part 2)

FMC Pin No.	Board Signal Name	FPGA Pin No.	Reference Design Signal Name
A36	GND		
A37	GND		
A38	N.C.		
A39	N.C.		
A40	GND		
C1	GND		
C2	FMCB_DP0_C2M_P	C23	
C3	FMCB_DP0_C2M_N	D23	
C4	GND		
C5	GND		
C6	FMCB_DP0_M2C_P	A24	DP0_p
C7	FMCB_DP0_M2C_N	B24	DP0_n
C8	GND		
C9	GND		
C10	FMCB_LA6_P	T29	
C11	FMCB_LA6_N	U30	
C12	GND		
C13	GND		
C14	FMCB_LA10_P	Y28	
C15	FMCB_LA10_N	Y27	
C16	GND		
C17	GND		
C18	FMCB_LA14_P	W26	
C19	FMCB_LA14_N	W25	
C20	GND		
C21	GND		
C22	FMCB_LA18_CC_P	R28	
C23	FMCB_LA18_CC_N	R27	
C24	GND		
C25	GND		
C26	FMCB_LA27_P	R23	
C27	FMCB_LA27_N	R22	
C28	GND		
C29	GND		
C30	FMCB_SCL	L24	
C31	FMCB_SDA	L22	
C32	GND		
C33	GND		
C34	FMCB_GA0	L23	

Table 3.9 FPC Pin assignment of relay board (Part 3)

FMC Pin No.	Board Signal Name	FPGA Pin No.	Reference Design Signal Name
C35	VCC_12V		
C36	GND		
C37	VCC_12V		
C38	GND		
C39	VCC_3V3		
C40	GND		
D1	FMCB_C2M_PG	N25	
D2	GND		
D3	GND		
D4	FMCB_GBTCLK_M2C_P	G18	REFCLK_p
D5	FMCB_GBTCLK_M2C_N	F18	REFCLK_n
D6	GND		
D7	GND		
D8	FMCB_LA1_CC_P	M32	
D9	FMCB_LA1_CC_N	N32	
D10	GND		
D11	FMCB_LA5_P	T32	
D12	FMCB_LA5_N	U32	
D13	GND		
D14	FMCB_LA9_P	U28	
D15	FMCB_LA9_N	V28	
D16	GND		
D17	FMCB_LA13_P	V27	
D18	FMCB_LA13_N	V26	
D19	GND		
D20	FMCB_LA17_P	AB28	
D21	FMCB_LA17_N	AC28	
D22	GND		
D23	FMCB_LA23_P	R24	
D24	FMCB_LA23_N	T24	
D25	GND		
D26	FMCB_LA26_P	P24	
D27	FMCB_LA26_N	P23	
D28	GND		
D29	TCK_FMCB		
D30	TDO_FMCA		
D31	TDO_FT		
D32	VCC_3V3		
D33	TMS_FMCB		

Table 3.9 FPC Pin assignment of relay board (Part 4)

FMC Pin No.	Board Signal Name	FPGA Pin No.	Reference Design Signal Name
D34	VCC_3V3(PU)		
D35	FMCB_GA1	K26	
D36	VCC_3V3		
D37	GND		
D38	VCC_3V3		
D39	GND		
D40	VCC_3V3		
G1	GND		
G2	FMCB_CLK1_M2C_P	Y26	
G3	FMCB_CLK1_M2C_N	AA27	
G4	GND		
G5	GND		
G6	FMCB_LA0_CC_P	L31	
G7	FMCB_LA0_CC_N	M30	
G8	GND		
G9	FMCB_LA3_P	R34	o_ims_xclr
G10	FMCB_LA3_N	R33	
G11	GND		
G12	FMCB_LA8_P	P34	io_ims_i2c_sda
G13	FMCB_LA8_N	P33	
G14	GND		
G15	FMCB_LA12_P	M33	i_ims_sdo
G16	FMCB_LA12_N	N33	
G17	GND		
G18	FMCB_LA16_P	T31	o_ims_xmaster
G19	FMCB_LA16_N	T30	
G20	GND		
G21	FMCB_LA20_P	T27	o_ims_omode
G22	FMCB_LA20_N	U27	
G23	GND		
G24	FMCB_LA22_P	P26	i_ims_tout0
G25	FMCB_LA22_N	P25	
G26	GND		
G27	FMCB_LA25_P	J29	i_ims_tout1
G28	FMCB_LA25_N	K29	
G29	GND		
G30	FMCB_LA29_P	N31	i_ims_tout2
G31	FMCB_LA29_N	N30	
G32	GND		

Table 3.9 FPC Pin assignment of relay board (Part 5)

FMC Pin No.	Board Signal Name	FPGA Pin No.	Reference Design Signal Name
G33	N.C.		
G34	N.C.		
G35	GND		
G36	N.C.		
G37	N.C.		
G38	GND		
G39	FMC_VADJ		
G40	GND		
H1	N.C.		
H2	FMCB_PRSNT	K24	
H3	GND		
H4	FMCB_CLK0_M2C_P	R26	
H5	FMCB_CLK0_M2C_N	T26	
H6	GND		
H7	FMCB_LA2_P	T34	i_ims_xvs
H8	FMCB_LA2_N	U34	
H9	GND		
H10	FMCB_LA4_P	U33	i_ims_xhs
H11	FMCB_LA4_N	V33	
H12	GND		
H13	FMCB_LA7_P	R32	io_ims_i2c_scl
H14	FMCB_LA7_N	R31	
H15	GND		
H16	FMCB_LA11_P	P31	o_ims_xce
H17	FMCB_LA11_N	P30	
H18	GND		
H19	FMCB_LA15_P	P29	o_ims_xtrig1
H20	FMCB_LA15_N	R29	
H21	GND		
H22	FMCB_LA19_P	T25	o_ims_xtrig2
H23	FMCB_LA19_N	U25	
H24	GND		
H25	FMCB_LA21_P	L34	o_ims_slamode0
H26	FMCB_LA21_N	M34	
H27	GND		
H28	FMCB_LA24_P	J31	o_ims_slamode1
H29	FMCB_LA24_N	J30	
H30	GND		
H31	FMCB_LA28_P	L30	o_ims_slamode2

Table 3.9 FPC Pin assignment of relay board (Part 6)

FMC Pin No.	Board Signal Name	FPGA Pin No.	Reference Design Signal Name
H32	FMCB_LA28_N	L29	
H33	GND		
H34	N.C.		
H35	N.C.		
H36	GND		
H37	N.C.		
H38	N.C.		
H39	GND		
H40	FMC_VADJ		