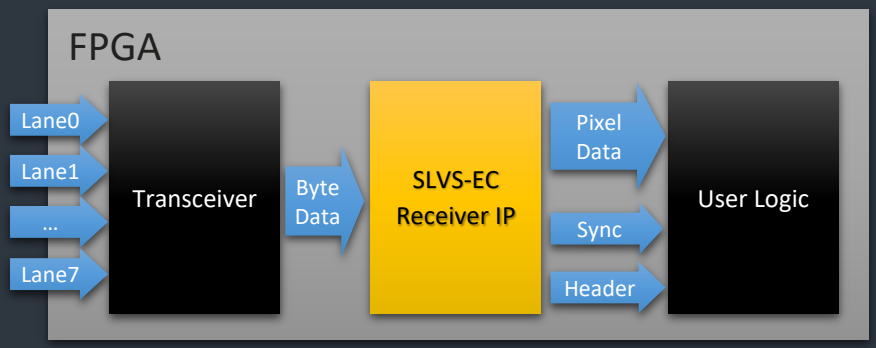
Introduction to CIS SLVS-EC Receiver IP for Elitestek

SLVS-EC Overview

SLVS-EC (Scalable Low Voltage Signaling with Embedded Clock) is a high speed, high performance interface for Sony CMOS image sensors. SLVS-EC differs from conventional LVDS interface in that the clock is embedded in the data, allowing circuit design without considering the pesky skew between serial buses. In a nutshell, SLVS-EC enables faster, lower power design made easy.

SLVS-EC Receiver IP Overview

CIS has concentrated on extracting pixel data from the byte data received via FPGA's high speed transceiver, enabling an IP with low FPGA resource usage , and also supports payload error detection and error correction (optional).



Specifications

Item	Compatibility
SLVS-EC Version	2.0 compliant
Lane	1,2,4,6,8
Raw Format	8,10,12,14,16
Line Length	4-∞ (default:65532)
CRC	Available
ECC	Available(optional)
Baud Rate	Grade1～3
Multi Stream	N.A.
Output Signals	Pixel Data, Sync. Signals, Packet Header etc.
Devices	Elitestek TJ-Series, Elitestek TP-Series

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Resource Usage

One of the advantages of CIS's SLVS-EC Receiver IP is its low resource usage. Although this IP allows you to dynamically change the number of SLVS-EC lanes, which affects resource usage, you can further reduce resources by limiting the maximum number of lanes used or by using a fixed lane configuration. The resource usage in TJ-Series (Primus 2024.2) is as follows:

ECC	Lane	FFs	SRLs	ADDs	LUTs	RAMs
w/o	1	959(904)	0(0)	281(281)	1961(1678)	2(2)
	2	1267(1245)	0(0)	288(288)	2625(2656)	4(4)
	4	2107 (2067)	0(0)	315(315)	4977(4614)	8(8)
	6	3171(3113)	0(0)	341(327)	8708(7695)	12(12)
	8	3785(3781)	0(0)	355(341)	10120(8867)	16(16)
w/	1	2477(2422)	32(32)	426(422)	3831(3528)	16(16)
	2	2785(2762)	32(32)	433(433)	4472(4417)	18(18)
	4	3998(3958)	30(30)	433(421)	7551(7156)	26(26)
	6	5774(5716)	28(28)	445(421)	12972(12180)	41(41)
	8	6388(6384)	28(28)	459(435)	14739(13104)	45(45)

Fixed lane configuration in parentheses

Demonstration Environment

CIS provides a camera with SLVS-EC output, relay board for connecting the camera and Elitestek's TJ375N1156X development board,
as well as reference design of FPGA. With this system, you can demonstrate Raw8, Raw10, and Raw12 using up to 2 lanes. Customers can freely customize and use the reference design.

Support

CIS has many experienced engineers in the fields of RTL design related to various high-speed interfaces and image processing, board design including high-speed signals, and embedded software development, etc. Please feel free to contact us for IP customization, etc.

Contact

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