Ti180 Data Sheet

DSTi180-v3.7
March 2026
www.elitestek.com



Copyright © 2026. All rights reserved. Elitestek and the Elitestek logo are trademarks of Elitestek Co., Ltd.. All other trademarks and service marks are the property of their respective owners. All specifications subject to change without notice.

Contents

Introduction **4**

Features **4**
- Package-Dependent Resources 5
- Available Package Options 5

Device Core Functional Description **6**
- XLR Cell 7
- Embedded Memory 8
  - True Dual-Port Mode 8
  - Simple Dual-Port Mode 8
- DSP Block 9
- Clock and Control Network 10
  - Clock Sources that Drive the Global and Regional Networks 11
  - Driving the Global Network 11
  - Driving the Regional Network 17
  - Driving the Local Network 18

Device Interface Functional Description **21**
- Interface Block Connectivity 21
- GPIO 22
  - Features for HVIO and HSIO Configured as GPIO 24
  - HVIO 27
  - HSIO 28
  - I/O Banks 43
- DDR DRAM Interface 44
- MIPI D-PHY 50
  - MIPI RX D-PHY 50
  - MIPI TX D-PHY 53
- Oscillator 55
- PLL 56
  - Dynamic Phase Shift 60
- Spread-Spectrum Clocking PLL 60
- Single-Event Upset Detection 62
- Internal Reconfiguration Block 62

Security Feature **63**

Power Sequence **65**
- Power-Up Sequence 66
- Power-Down Sequence 68
- Power Supply Current Transient 68
- Unused Resources and Features 68

Configuration **69**
- Supported Configuration Modes 70

Characteristics and Timing **71**
- DC and Switching Characteristics 71
- HSIO Electrical and Timing Specifications 79
- MIPI Electrical Specifications and Timing 82
  - MIPI Reset Timing 83
- PLL Timing and AC Characteristics 84
- Configuration Timing 85
  - JTAG Mode 86
  - SPI Active Mode 87
  - SPI Passive Mode 88

Pinout Description **89**
Configuration Pins 91
Dedicated DDR Pinout 93
Dedicated MIPI D-PHY Pinout 94
Pin States 95

Ti180 Interface Floorplan **97**

Efinity Software Support **100**

Ordering Codes **100**

Revision History **101**

Introduction

The TJ-Series Ti180 FPGA features the high-density, low-power Elitestek® Quantum® compute fabric wrapped with an I/O interface in a small footprint package for easy integration. Ti180 FPGAs include hardened MIPI D-PHY that you can use with Elitestek® MIPI CSI-2 and DSI controller IP cores to create multi-camera, high definition vision systems, edge computing, and hardware acceleration systems. Additionally, these FPGAs have a hardened DDR DRAM controller block that supports a LPDDR4 DRAM interface. With ultra-low power Ti180 FPGAs, designers can build products that are always on, providing enhanced capabilities for applications such as vision systems, edge computing, hardware acceleration, and machine learning.

The Ti180 is also available as a SIP that combines the Ti180 FPGA with an LPDDR4x SDRAM device in the same package. Because the memory chip connects directly to the FPGA in the package, you save space on your board and simplify your overall board design.

Features

- High-density, low-power Quantum® compute fabric
- 10-kbit high-speed, embedded SRAM, configurable as single-port RAM, simple dual-port RAM, true dual-port RAM, or ROM
- High-performance DSP blocks for multiplication, addition, subtraction, accumulation, and up to 15-bit variable-right-shifting
- Versatile on-chip clocking
  - Low-skew global network supporting 32 clock or control signals
  - Regional and local clock networks
  - PLL support
- FPGA interface blocks
  - LPDDR4/4x PHY (supporting x16 or x32 DQ widths) with memory controller hard IP
  - MIPI D-PHY hard IP with speeds up to 2.5 Gbps
  - Two varieties of general-purpose I/O (GPIO) pins:
    - High-voltage I/O (HVIO) pins support 1.8, 2.5, and 3.3 V
    - Configurable high-speed I/O (HSIO) pins support
      - Single-ended and differential I/O
      - LVDS, subLVDS, Mini-LVDS, and RSDS (RX, TX, and bidirectional), up to 1.5 Gbps
      - MIPI lane (DSI and CSI) in high-speed and low-power modes, up to 1.5 Gbps
  - PLL
  - Oscillator
  - Spread-Spectrum Clocking (SSC) PLL
- Flexible device configuration
  - Standard SPI interface (active, passive, and daisy chain)
  - JTAG interface
  - Supports internal reconfiguration
- Single-event upset (SEU) detection feature
- J484 packages are available in an automotive (Q3) speed grade with
  - AEC-Q100 qualification
  - Production Part Approval Process (PPAP) documentation
- Fully supported by the Efinity® software, an RTL-to-bitstream compiler

Table 1: Ti180 FPGA Resources

Logic Elements (LEs)	eXchangeable Logic and Routing (XLR) Cells		Global Clock and Control Signals	Embedded Memory (Mbits)	Embedded Memory Blocks (10 Kbits)	Embedded DSP Blocks
	Total	SRL8[1]				
176,256	172,800	32,000	Up to 32	13.11	1,280	640

Package-Dependent Resources

Table 2: Ti180 Package-Dependent Resources

Resource		J361	G400	J484	L484	G529
Single-ended GPIO (Maximum)	HVIO LVCMOS: 1.8, 2.5, 3.0, 3.3 V LVTTL: 3.0, 3.3 V	20	74	27	27	48
	HSIO LVCMOS, HSTL: 1.2, 1.5, 1.8 V SSTL: 1.2, 1.35, 1.5, 1.8 V	110	200	116	116	210
Differential GPIO (Maximum)	HSIO (LVDS, Differential HSTL, and SSTL)	54	100	57	57	105
	HSIO (MIPI D-PHY Data Lanes)	45	82	47	47	88
	HSIO (MIPI D-PHY Clock Lanes)	9	17	10	10	17
LPDDR4/4x PHY with memory controller		1 x16	–	1 x32	–	1 x32
MIPI D-PHY Hard Blocks	RX	2	–	4	4	–
	TX or SSC PLL	2	–	4	4	–
Global clock or control signals from GPIO pins		20	32	32	32	32
PLLs		8	8	8	8	8

Note: The x32 LPDDR4/4x PHY with memory controller can be configured as x16 or x32 widths.

Available Package Options

Table 3: Available Packages

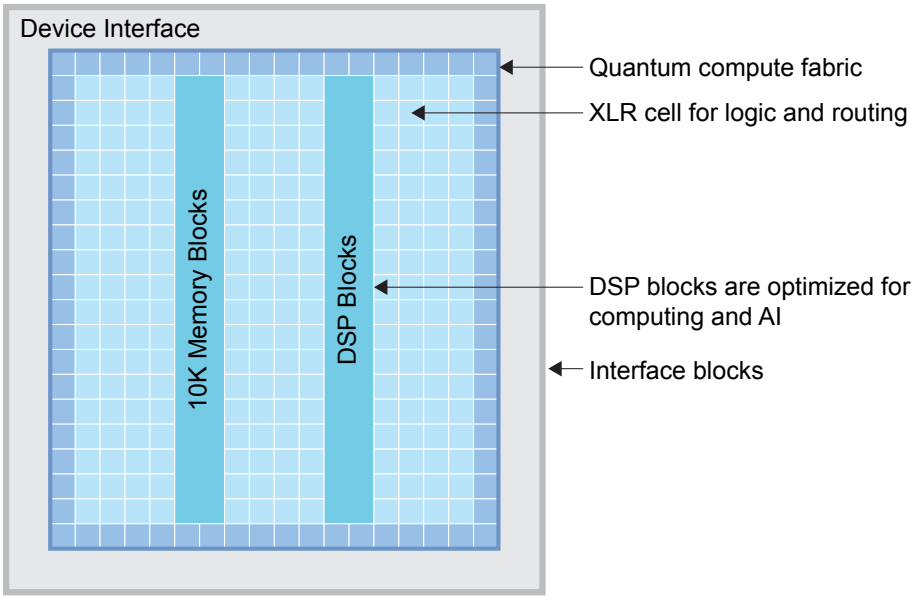
Package	Dimensions (mm x mm)	Pitch (mm)
361-ball FBGA	13 x 13	0.65
400-ball FBGA	16 x 16	0.8
484-ball FBGA	18 x 18	0.8
529-ball FBGA	19 x 19	0.8

[1] Number of XLR that can be configured as shift register with 8 maximum taps.

Device Core Functional Description

Ti180 FPGAs feature an eXchangeable Logic and Routing (XLR) cell that Elitestek® has optimized for a variety of applications. TJ-Series FPGAs contain LEs that are constructed from XLR cells. Each FPGA in the TJ-Series family has a custom number of building blocks to fit specific application needs. As shown in the following figure, the FPGA includes I/O ports on all four sides, as well as columns of LEs, memory, and DSP blocks. A control block within the FPGA handles configuration.

Figure 1: Ti180 FPGA Block Diagram



Interface blocks include GPIO, LVDS, PLL, MIPI lane I/O, MIPI D-PHY, and DDR DRAM.

XLR Cell

The eXchangeable Logic and Routing (XLR) cell is the basic building block of the Quantum® architecture. The Elitestek® XLR cell combines logic and routing and supports both functions. This unique innovation greatly enhances the transistor flexibility and utilization rate, thereby reducing transistor counts and silicon area significantly.

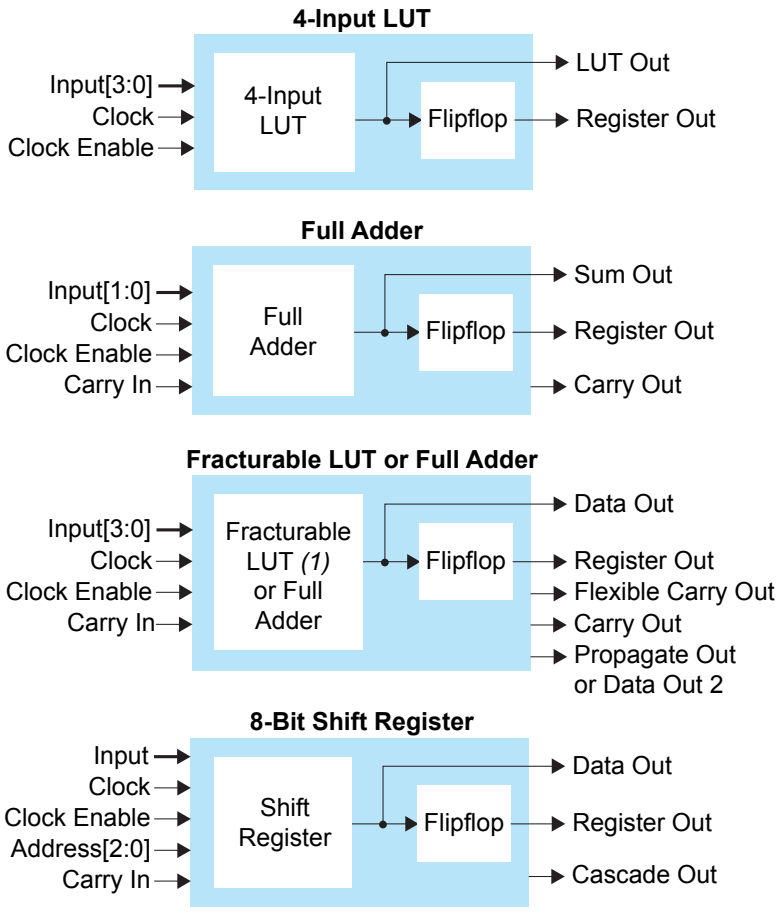
Learn more: For more detailed on the advantages the XLR cell brings to TJ-Series FPGAs, read the **Why the XLR Cell is a Big Deal White Paper**.

The XLR cell functions as:

- A 4-input LUT that supports any combinational logic function with four inputs.
- A simple full adder.
- An 8-bit shift register that can be cascaded.
- A fracturable LUT or full adder.

The logic cell includes an optional flipflop. You can configure multiple logic cells to implement arithmetic functions such as adders, subtractors, and counters.

Figure 2: Logic Cell Functions



1. The fracturable LUT is a combination of a 3-input LUT and a 2-input LUT. They share 2 of the same inputs.

Learn more: Refer to the **Quantum® TJ-Series Primitives User Guide** for details on the TJ-Series logic cell primitives.

Embedded Memory

The core has 10-kbit high-speed, synchronous, embedded SRAM memory blocks. Memory blocks can operate as single-port RAM, simple dual-port RAM, true dual-port RAM, or ROM. You can initialize the memory content during configuration. The Efinity® software includes a memory cascading feature to connect multiple blocks automatically to form a larger array. This feature enables you to instantiate deeper or wider memory modules.

Note: The block RAM content is random and undefined if it is not initialized.

The read and write ports support independently configured data widths, an address enable, and an output register reset. The simple dual-port mode also supports a write byte enable.

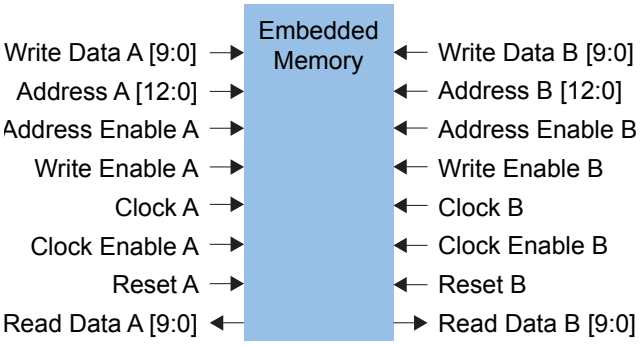
Learn more: Refer to the **Quantum® TJ-Series Primitives User Guide** for details on the TJ-Series RAM configuration.

True Dual-Port Mode

The memory read and write ports have the following modes for addressing the memory (depth × width):

1024 × 8	2048 × 4	4096 × 2
8192 × 1	1024 × 10	2048 × 5

Figure 3: RAM Block Diagram (True Dual-Port Mode)

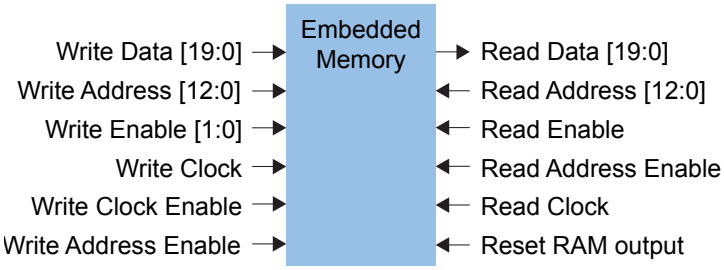


Simple Dual-Port Mode

The memory read and write ports have the following modes for addressing the memory (depth × width):

512 × 16	1024 × 8	2048 × 4	4096 × 2
8192 × 1	512 × 20	1024 × 10	2048 × 5

Figure 4: Simple Dual-Port Mode RAM Block Diagram (512 × 20 Configuration)



DSP Block

The FPGA has high-performance, complex DSP blocks that can perform multiplication, addition, subtraction, accumulation, and 4-bit variable right shifting. The 4-bit variable right shift supports one lane in normal mode, two lanes in dual mode and four lanes in quad mode. Each DSP block has four modes, which support the following multiplication operations:

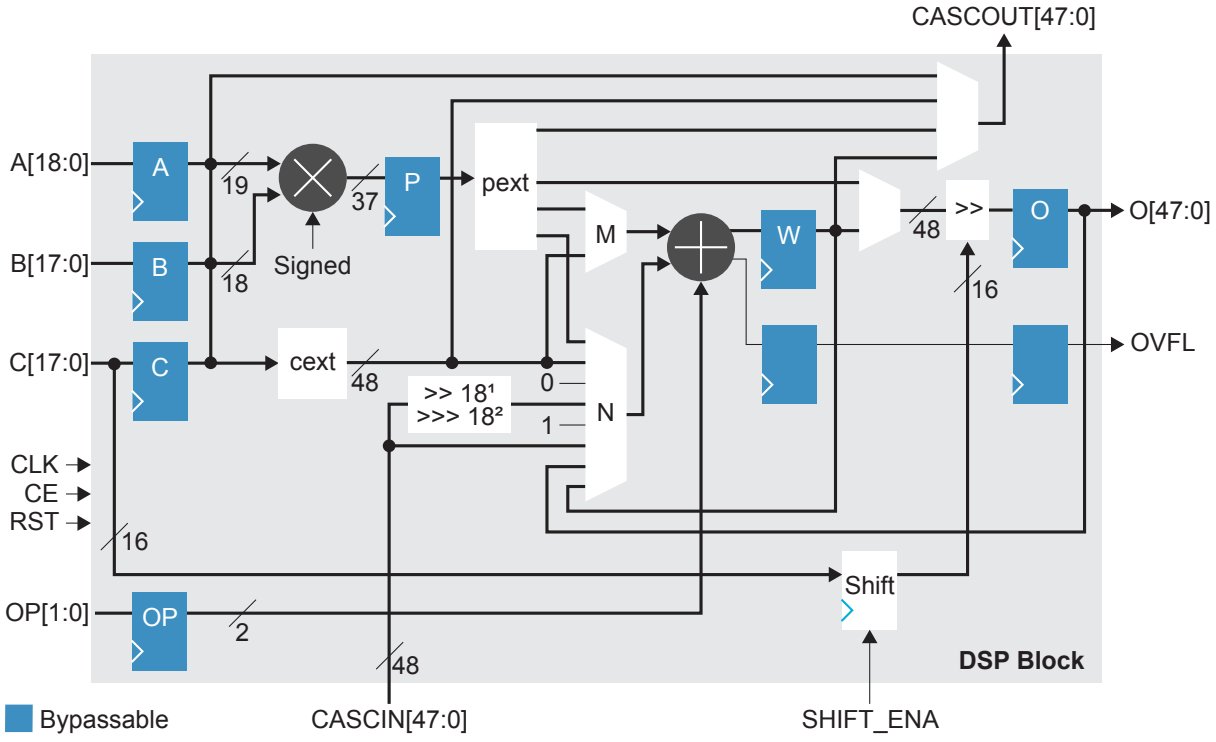
- *Normal*—One 19 × 18 integer multiplication with 48-bit addition/subtraction.
- *Dual*—One 11 × 10 integer multiplication and one 8 × 8 integer multiplication with two 24-bit additions/subtractions.
- *Quad*—One 7 × 6 integer multiplication and three 4 × 4 integer multiplications with four 12-bit additions/subtractions.

  Important: The 7 × 6 Quad mode output is truncated to 12-bit.

- *Float*—One fused-multiply-add/subtract/accumulate (FMA) BFLOAT16 multiplication.

The integer multipliers can represent signed or unsigned values based on the `SIGNED` parameter. When multiple EFX_DSP12 or EFX_DSP24 primitives are mapped to the same DSP block, they must have the same `SIGNED` value. The inputs to the multiplier are the A and B data inputs. Optionally, you can use the result of the multiplier in an addition or subtraction operation.

Figure 5: DSP Block Diagram



1. Logical right-shift-by-18.
2. Arithmetic right-shift-by-18.

Learn more: Refer to the **Quantum® TJ-Series Primitives User Guide** for details on the TJ-Series DSP block primitives.

Clock and Control Network

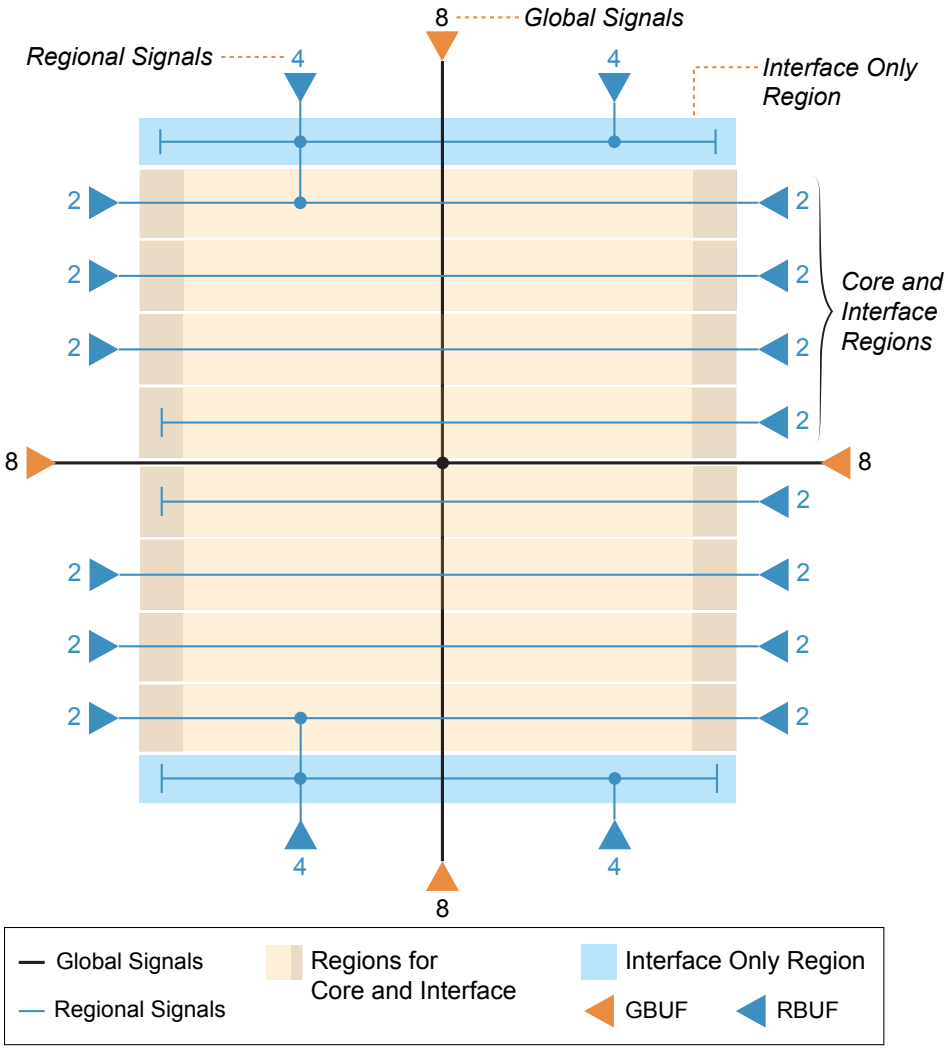
The clock and control network is distributed through the FPGA to provide clocking for the core's LEs, memory, DSP blocks, I/O blocks, and control signals. The FPGA has 32 global signals that can be used as either clocks or control signals. The global signals are balanced trees that feed the whole FPGA.

The FPGA also has regional signals that can only reach certain FPGA regions, including the top or bottom edges. The FPGA has 8 regional networks for the core, right interface, and left interface blocks. The top and bottom interface blocks have one regional clock network each. You can drive the right and left sides of each region independently. Each region also has a local network of clock signals that can only be used in that region.

The core's global buffer (GBUF) blocks drive the global and regional networks. Signals from the core and interface can drive the GBUF blocks.

Each network has dedicated enable logic to save power by disabling the clock tree. The logic dynamically enables/disables the network and guarantees no glitches at the output.

Figure 6: Global and Regional Clock Network Overview



Clock Sources that Drive the Global and Regional Networks

The Ti180 global and regional networks are highly flexible and configurable. Clock sources can come from interface blocks, such as GPIO or PLLs, or from the core fabric.

Table 4: Clock Sources that Drive the Global and Regional Networks

Source	Description
GPIO	Supports GCLK and RCLK. (Only the P resources support this connection type).
LVDS RX	Supports GCLK and RCLK.
MIPI D-PHY RX, TX, and SSC PLL	Can drive the word clock onto the global and regional clock networks.
MIPI RX Lane (configured as clock lane)	Supports GCLK (default) and RCLK. You can only use resources that are identified as clocks.
PLL	All output clocks connect to the global network. Refer to **Driving the Regional Network** on page 17 for the PLL clocks that drive the regional network.
Oscillator	Connects to global buffer.
Core	Signals from the core logic can drive the global or regional network.

Driving the Global Network

You can access the global clock network using the global clock GPIO pins, PLL outputs, oscillator output, MIPI word clocks, and core-generated clocks.

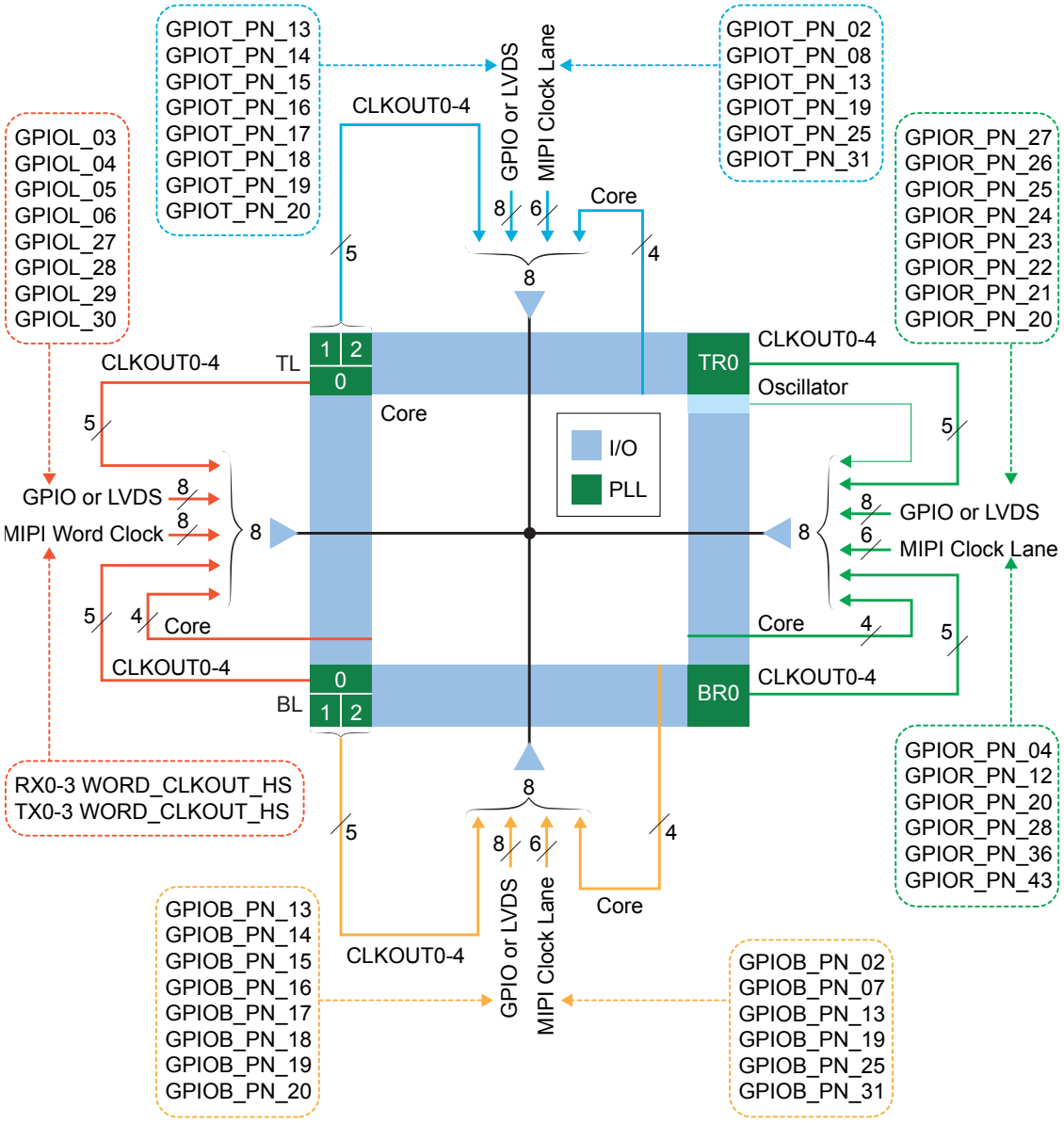
A clock multiplexing network controls which interface blocks can drive the global and regional networks. Eight of the clock multiplexers are dynamic (two on each side of the FPGA), allowing you to change which clock drives the global signal in user mode.



Learn more: Refer to the **Quantum® TJ-Series Primitives User Guide** for information on how to configure the global and regional clock networks.

The following figure shows the global network clock sources graphically.

Figure 7: Clock Sources that Drive the Global Network



Numerous clock sources feed the global network. These signals are multiplexed together with static and dynamic clock multiplexers.

The dynamic multiplexers are configurable by the user at run-time. You can choose which clock source drives which input to the dynamic multiplexer. When you enable the dynamic multiplexer, you specify a select bus to choose which clock source is active.

When dynamically switching between the clock inputs of a dynamic multiplexer, both the currently active input and the input you intend to switch to must have toggling clocks during the switching period. Additionally, upon configuration completion and when the device transitions into user mode, input 0 of the dynamic multiplexer becomes the default active input. Therefore, you must feed a toggling clock to input 0 before switching to other inputs.

The following figures show the resources that drive each multiplexer.

Figure 8: Clock Sources that Drive the Multiplexers: Top

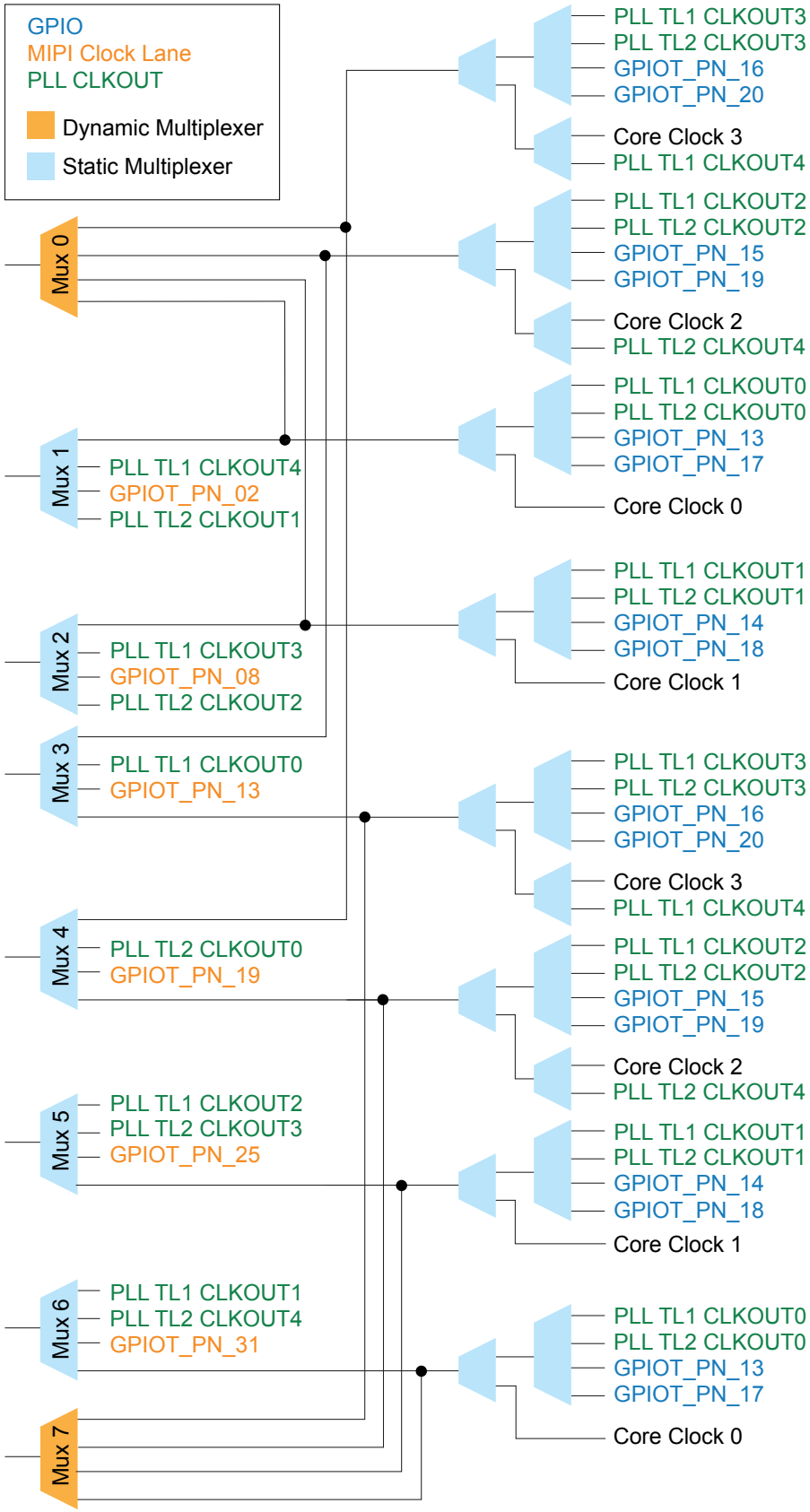


Figure 9: Clock Sources that Drive the Multiplexers: Bottom

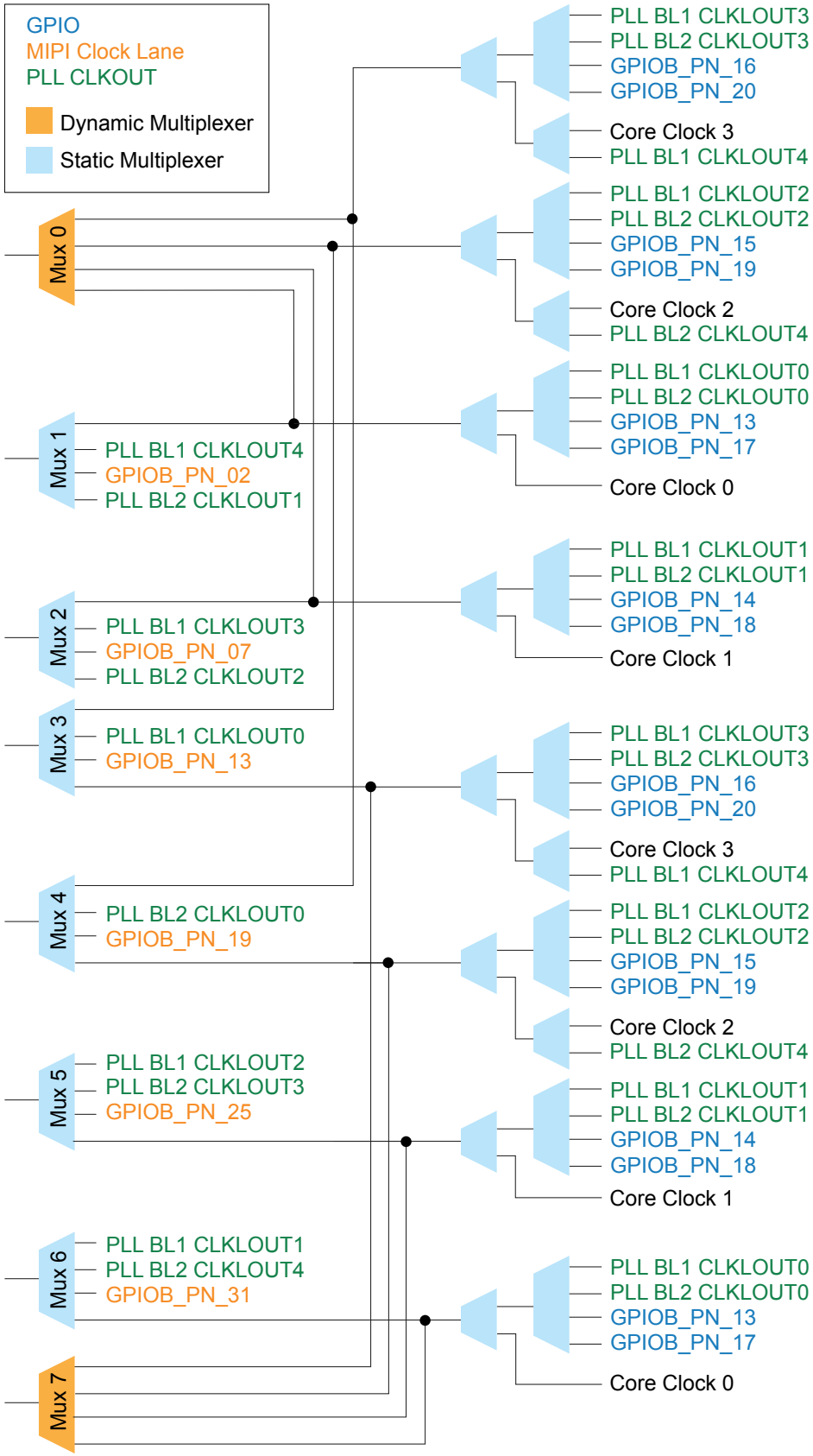


Figure 10: Clock Sources that Drive the Multiplexers: Left

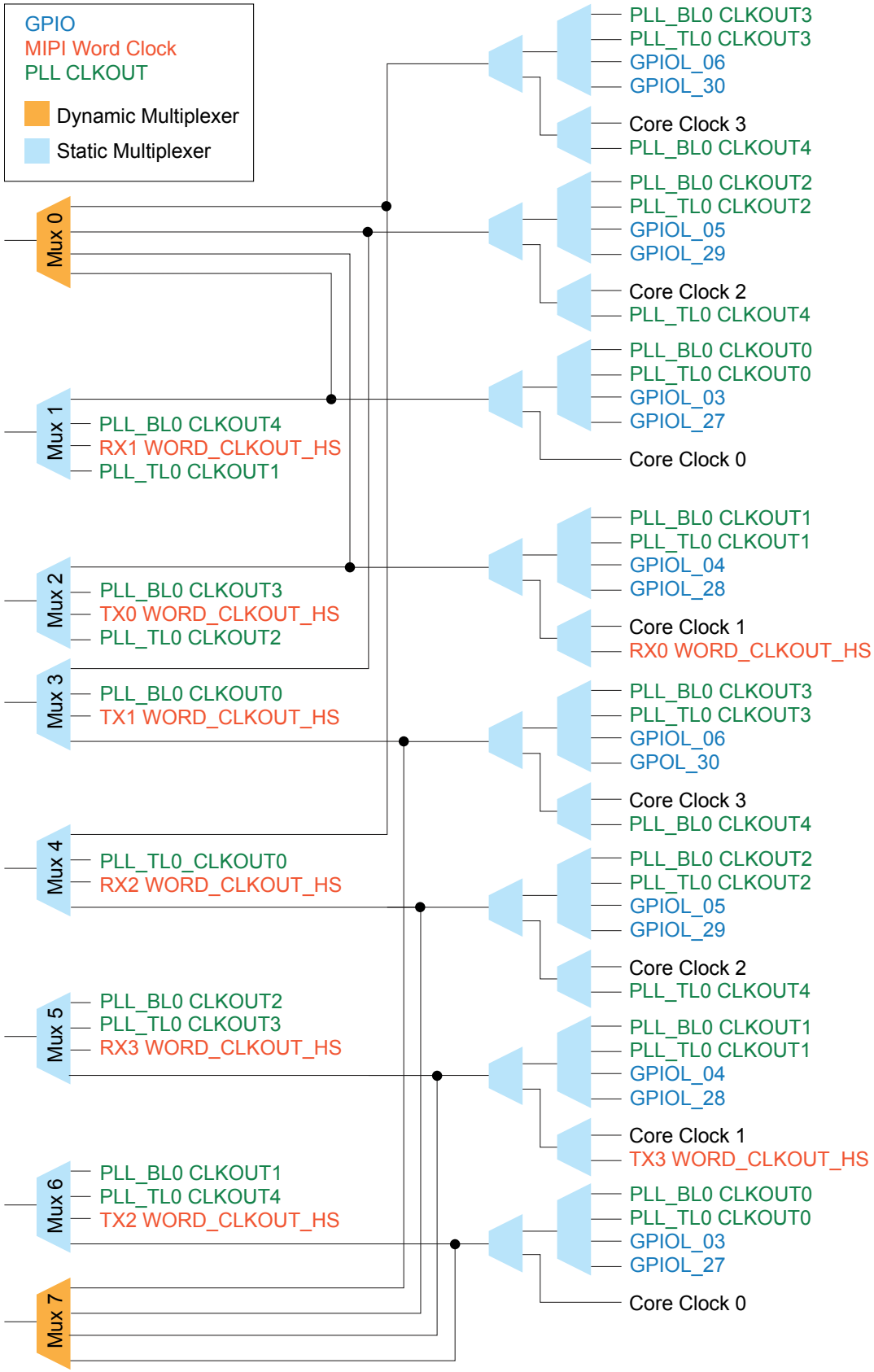
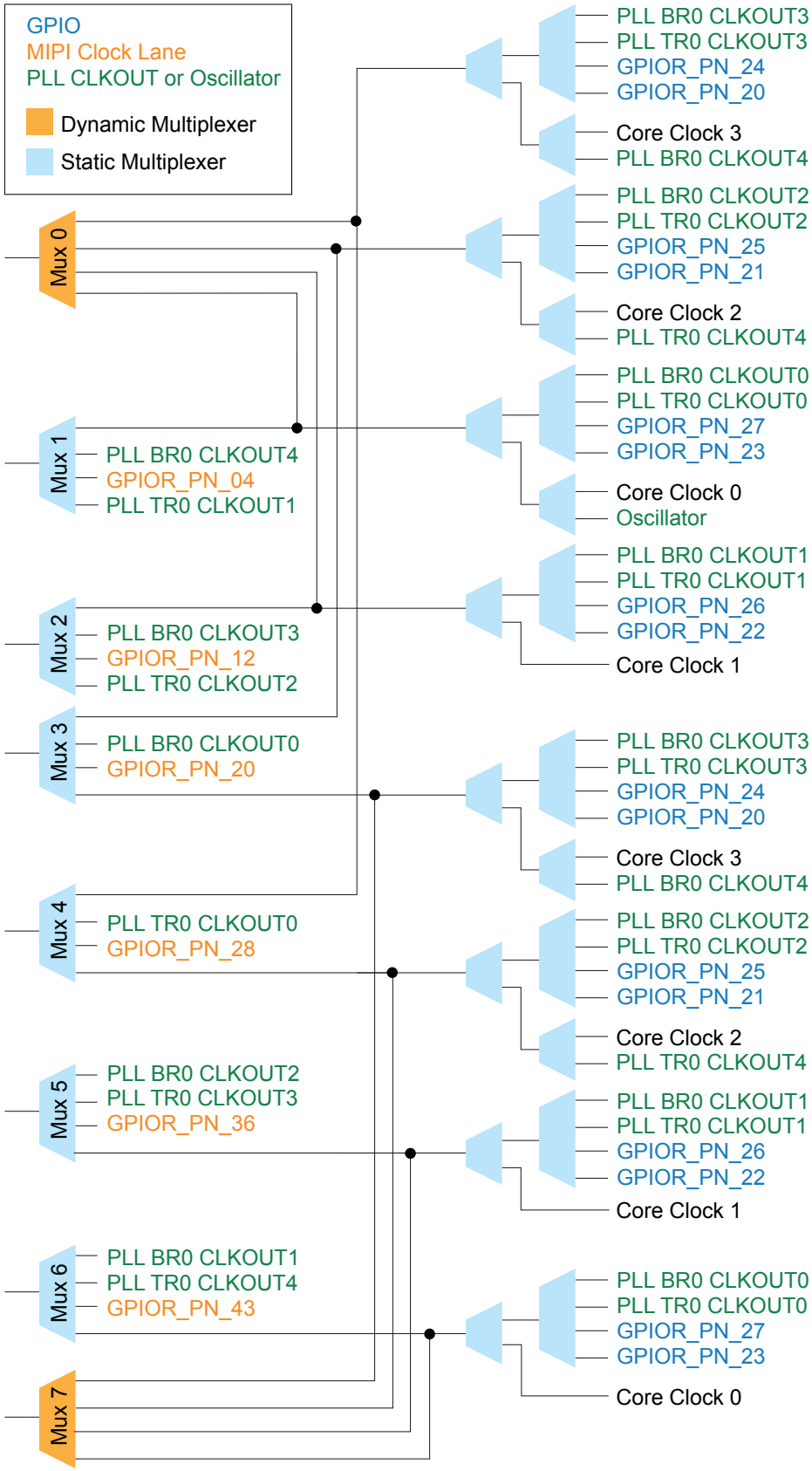


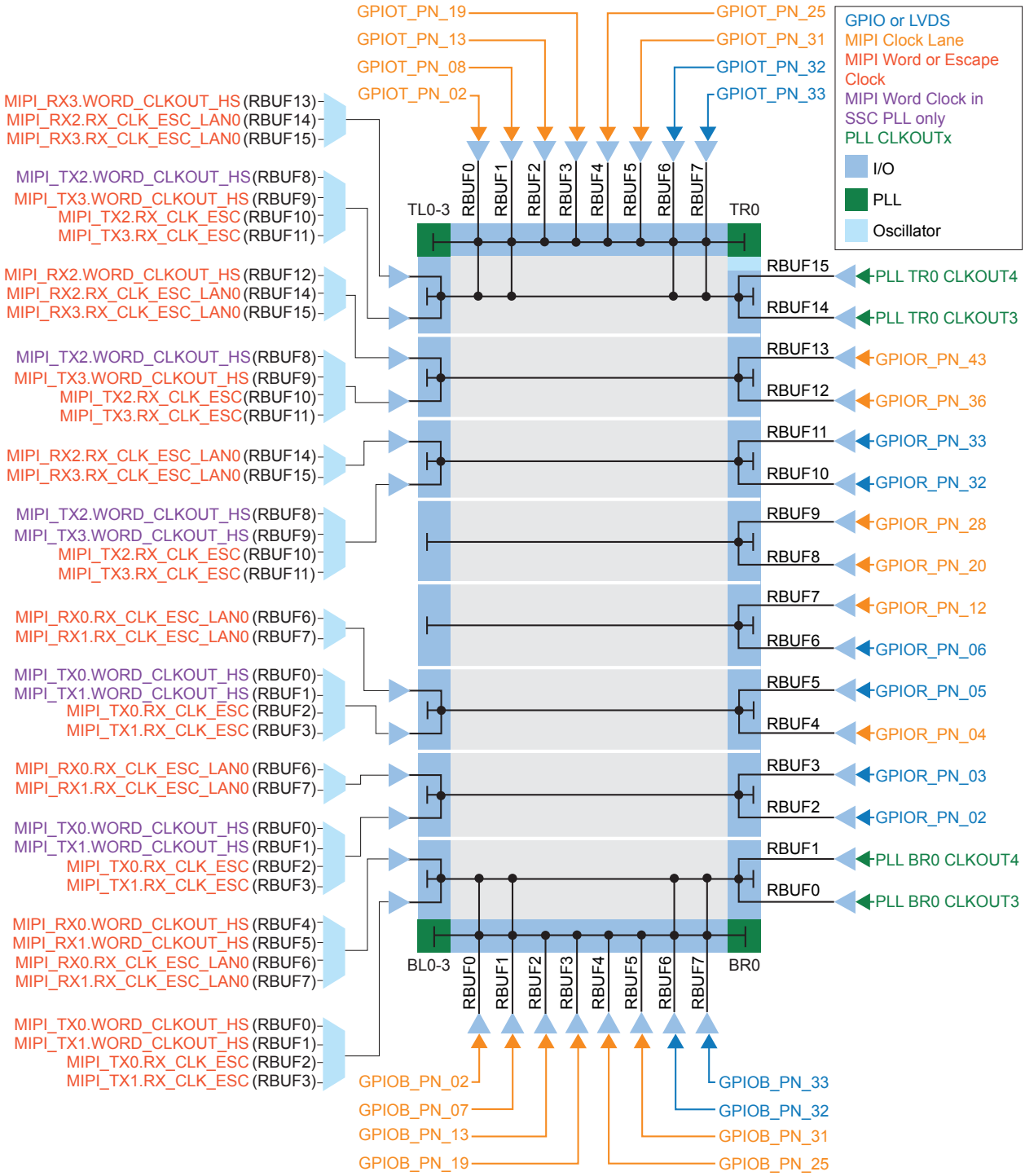
Figure 11: Clock Sources that Drive the Multiplexers: Right



Driving the Regional Network

The following figure shows the regional network clock sources graphically.

Figure 12: Clock Sources that Drive the Regional Network



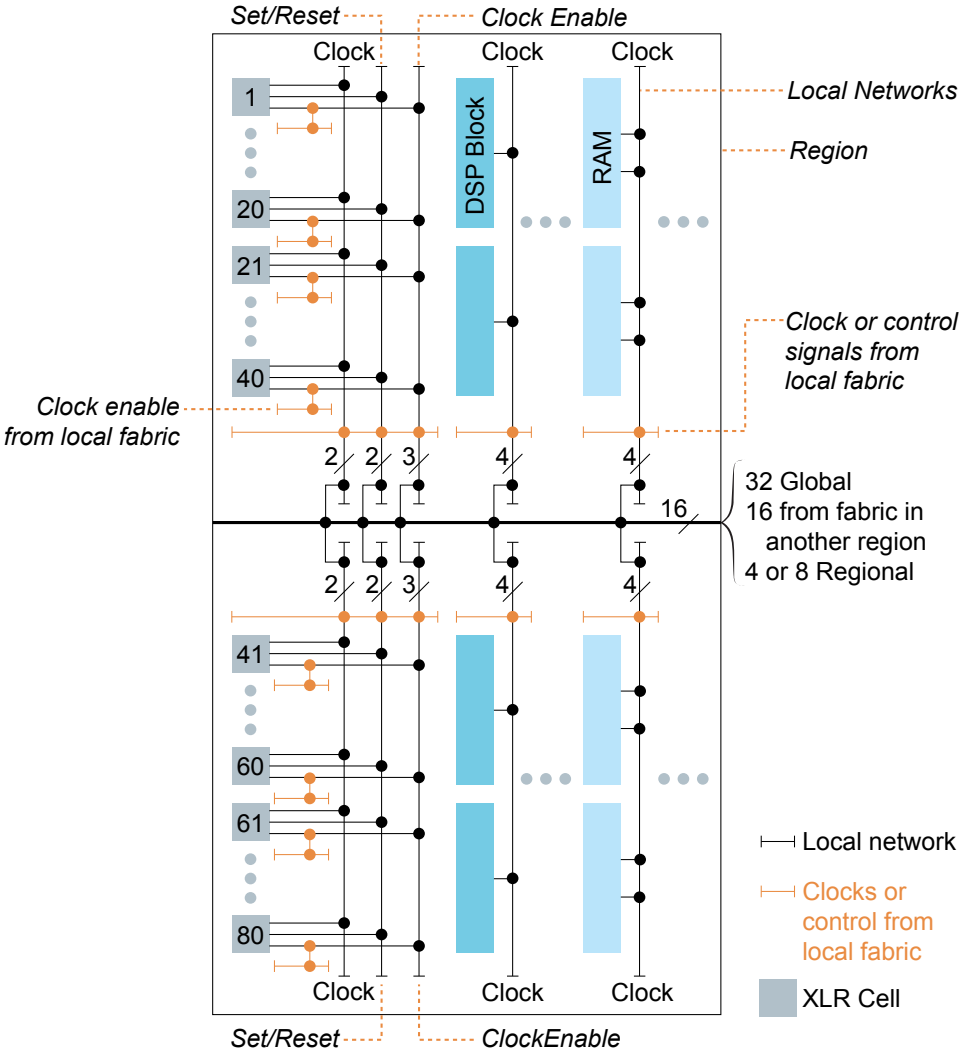
Driving the Local Network

As described previously, the FPGA has horizontal clock regions. The top and bottom regions are **only** for the top and bottom interfaces. The other regions are for the core logic (XLR cells, DSP Blocks, and RAM) and the interfaces on the sides.

Local Network for Core Logic

As shown in the following figure, the regions that contain the core logic are 80 XLR cells tall, and the local network connects an area that is 40 XLR cells tall. Additionally, each column has its own local network. For example, in the first column, XLR cells 1 - 40 are in the same local network and XLR cells 41 - 80 are in another local network. DSP Blocks and RAM also have their own local networks. This pattern of block/local network is repeated for each column in the die.

Figure 13: Clock Sources for Logic, DSP Blocks, and RAM



There are 16 signals that can feed the local networks. These signals can come from several sources:

- The global network (32 possible signals)
- The core fabric in another region (16 possible signals)
- The regional network (four or eight possible signals):
  - For the top and bottom regions eight signals can come from the regional network.
  - For the other regions, four signals can come from the regional network. (Refer back to **Clock and Control Network** on page 10.)

Additionally, the local fabric can generate clock and control signals for the local network. The fabric can also drive the clock enable for the XLR cell directly, allowing each XLR cell to have a unique clock enable.

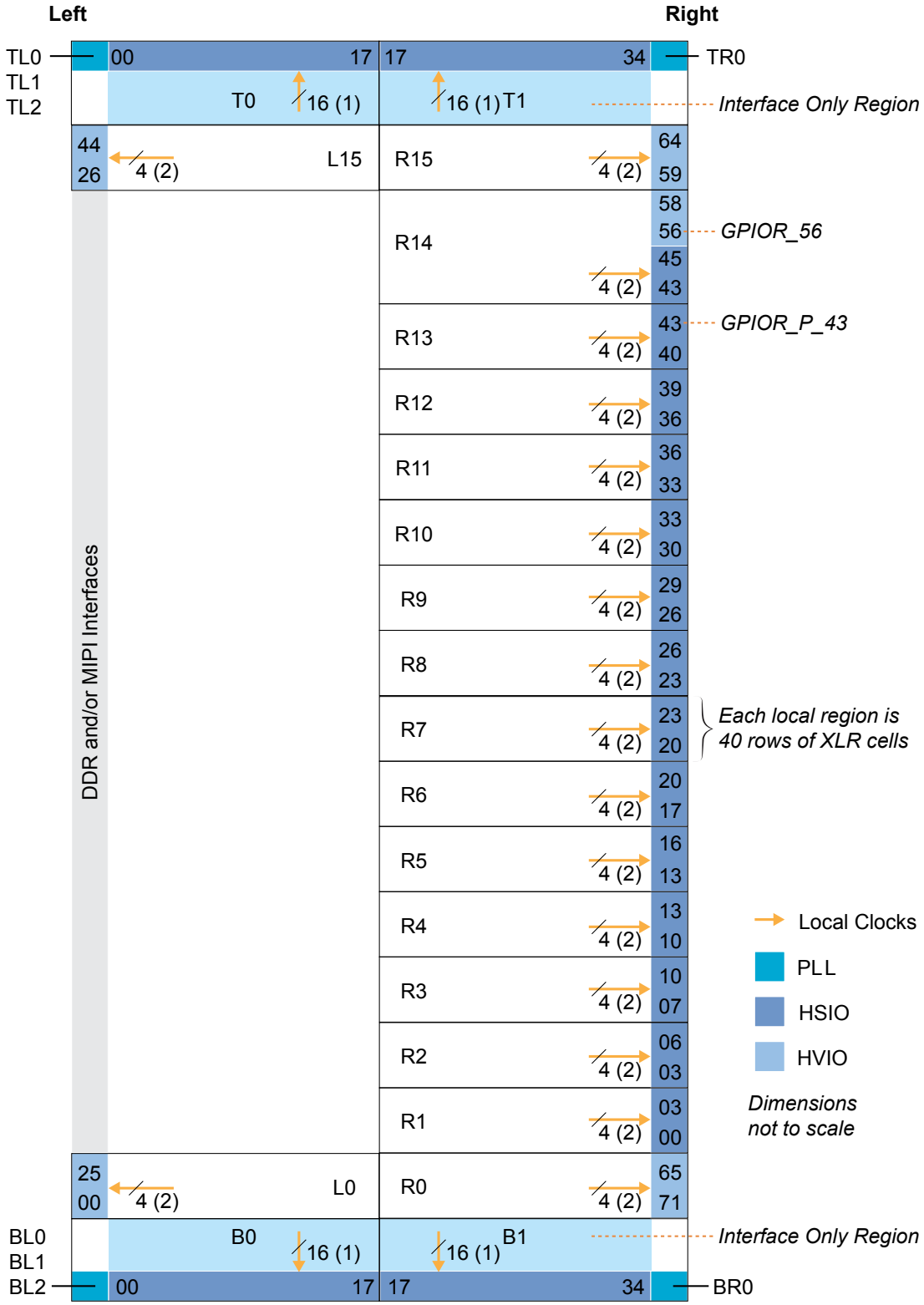
Local Network for Interface Regions

The following figure shows the local clock networks for the interface blocks. There are a limited number of unique clocks per local clock region.

- The top and bottom regions can each support up to 16 unique clock signals; 14 from the global network and two from the fabric.

- The left and right regions can each support up to four unique clock signals. Up to two can come from the routing fabric, the rest come from the global or regional buffers. These regions are the same height as the core local regions (that is, 40 rows).

Figure 14: Clock Sources that Drive the Interfaces



Note:
1. 14 signals come from the global network; 2 come from the routing fabric.
2. Up to 2 signals can come from the routing fabric. The rest come from the regional/global buffer.

Device Interface Functional Description

The device interface wraps the core and routes signals between the core and the device I/O pads through a signal interface. Because they use the flexible Quantum® architecture, devices in the TJ-Series family support a variety of interfaces to meet the needs of different applications.

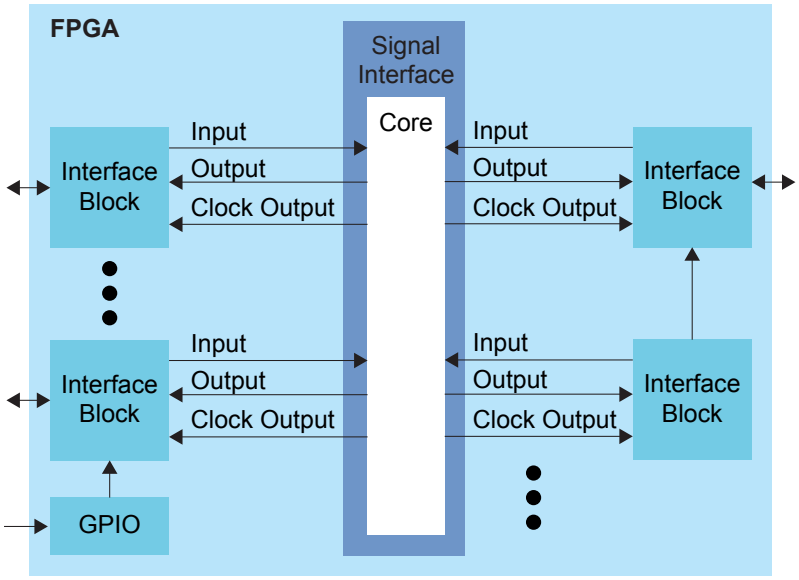
Learn more: The following sections describe the available device interface features in Ti180 FPGAs. Refer to the **TJ-Series Interfaces User Guide** for details on the Efinity® Interface Designer settings.

Interface Block Connectivity

The FPGA core fabric connects to the interface blocks through a signal interface. The interface blocks then connect to the package pins. The core connects to the interface blocks using three types of signals:

- *Input*—Input data or clock to the FPGA core
- *Output*—Output from the FPGA core
- *Clock output*—Clock signal from the core clock tree

Figure 15: Interface Block and Core Connectivity



GPIO blocks are a special case because they can operate in several modes. For example, in alternate mode the GPIO signal can bypass the signal interface and directly feed another interface block. So a GPIO configured as an alternate input can be used as a PLL reference clock without going through the signal interface to the core.

When designing for TJ-Series FPGAs, you create an RTL design for the core and also configure the interface blocks. From the perspective of the core, outputs from the core are inputs to the interface block and inputs to the core are outputs from the interface block.

The Efinity netlist always shows signals from the perspective of the core, so some signals do not appear in the netlist:

- GPIO used as reference clocks are not present in the RTL design, they are only visible in the interface block configuration of the Efinity® Interface Designer.
- The FPGA clock tree is connected to the interface blocks directly. Therefore, clock outputs from the core to the interface are not present in the RTL design, they are only part of the interface configuration (this includes GPIO configured as output clocks).

The following sections describe the different types of interface blocks. Signals and block diagrams are shown from the perspective of the interface, not the core.

GPIO

The Ti180 FPGA supports the following types of GPIO:

- *High-voltage I/O (HVIO)*—Simple I/O blocks that can support single-ended I/O standards.
- *High-speed I/O (HSIO)*—Complex I/O blocks that can support single-ended and differential I/O functionality.

The I/O logic comprises three register types:

- *Input*—Capture interface signals from the I/O before being transferred to the core logic
- *Output*—Register signals from the core logic before being transferred to the I/O buffers
- *Output enable*—Enable and disable the I/O buffers when I/O used as output

The HVIO supports the following I/O standards.

Table 5: HVIO Supported Standards

Standard	VCCIO33 (V)	When Configured As
LVTTL 3.3 V	3.3	GPIO
LVTTL 3.0 V	3.0	GPIO
LVCMOS 3.3 V	3.3	GPIO
LVCMOS 3.0 V	3.0	GPIO
LVCMOS 2.5 V	2.5	GPIO
LVCMOS 1.8 V	1.8	GPIO

Important: Elitestek recommends that you limit the number of 3.0/3.3 V HVIO as bidirectional or output to 6 per bank to avoid switching noise. The Efinity® software issues a warning if you exceed the recommended limit.

The HSIO pins support the following I/O standards.

Table 6: HSIO Supported I/O Standards

Standard	VCCIO (V)		VCCAUX (V)	VREF (V)	When Configured As
	TX	RX			
LVCMOS 1.8 V	1.8	1.8	1.8	–	GPIO
LVCMOS 1.5 V	1.5	1.5	1.8	–	GPIO
LVCMOS 1.2 V	1.2	1.2	1.8	–	GPIO
HSTL/Differential HSTL 1.8 V SSTL/Differential SSTL 1.8 V	1.8	1.8	1.8	0.5 * VCCIO	GPIO
HSTL/Differential HSTL 1.5 V SSTL/Differential SSTL 1.5 V	1.5	1.5, 1.8[(2)]	1.8	0.5 * VCCIO	GPIO
SSTL/Differential SSTL 1.35 V	1.35	1.35, 1.5, 1.8[(2)]	1.8	0.5 * VCCIO	GPIO
HSTL/Differential HSTL 1.2 V SSTL/Differential SSTL 1.2 V	1.2	1.2, 1.35, 1.5, 1.8[(2)]	1.8	0.5 * VCCIO	GPIO
LVDS/RSDS/mini-LVDS	1.8	1.5, 1.8[(2)]	1.8	–	LVDS
Sub-LVDS	1.8	1.5, 1.8[(2)]	1.8	–	Sub-LVDS
MIPI	1.2	1.2	1.8	–	MIPI Lane
SLVS	1.2	1.2	1.8	–	SLVS

[(2)] To prevent pin leakage, you must ensure that the voltage at the pin does not exceed VCCIO.

The differential receivers are powered by VCCAUX, which gives you the flexibility to choose the VCCIO you want to use. However, you must comply to the requirements stated in the previous table.

Features for HVIO and HSIO Configured as GPIO

The following table describes the features for HVIO and HSIO configured as GPIO.

Table 7: Features for HVIO and HSIO Configured as GPIO

Feature	HVIO	HSIO Configured as GPIO
Double-data I/O (DDIO)	✓	✓
Dynamic pull-up	–	✓
Pull-up/Pull-down	✓	✓
Slew-Rate Control	–	✓
Variable Drive Strength	✓	✓
Schmitt Trigger	✓	✓
1:4 Serializer/Deserializer (Full rate mode only)	–	✓
Programmable Bus Hold	–	✓
Static Programmable Delay Chains	✓	✓
Dynamic Programmable Delay Chains	–	✓

Table 8: GPIO Modes

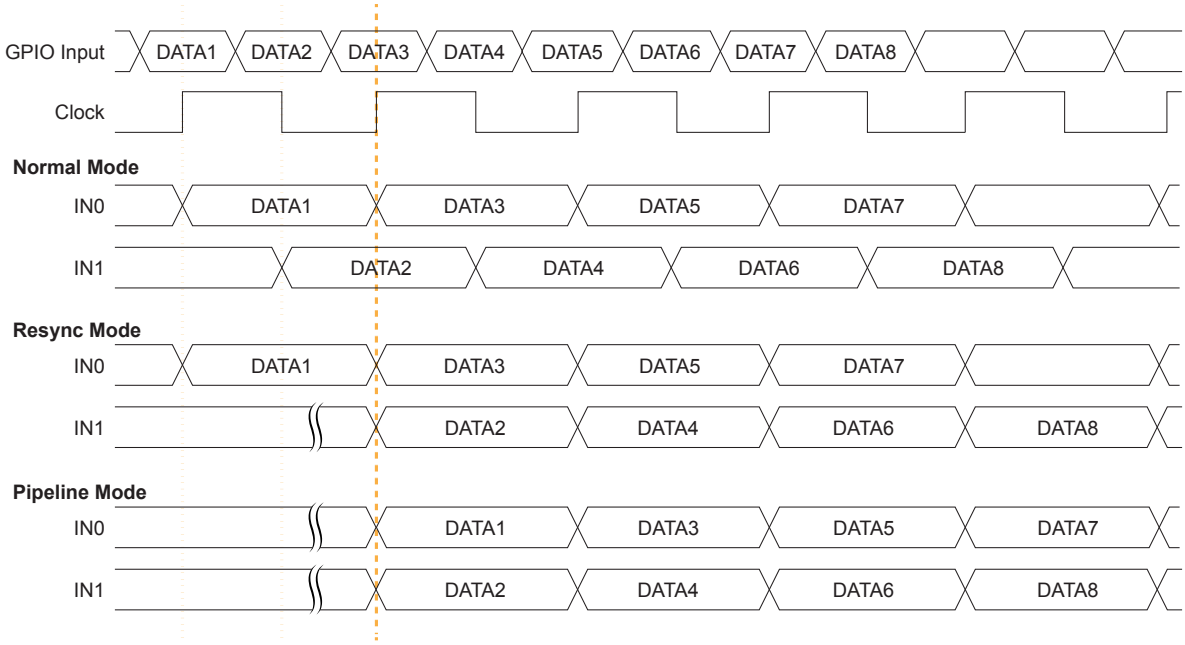
GPIO Mode	Description
Input	Only the input path is enabled; optionally registered. If registered, the input path uses the input clock to control the registers (positively or negatively triggered). Select the alternate input path to drive the alternate function of the GPIO. The alternate path cannot be registered. In DDIO mode, two registers sample the data on the positive and negative edges of the input clock, creating two data streams.
Output	Only the output path is enabled; optionally registered. If registered, the output path uses the output clock to control the registers (positively or negatively triggered). The output register can be inverted. In DDIO mode, two registers capture the data on the positive and negative edges of the output clock, multiplexing them into one data stream.
Bidirectional	The input, output, and OE paths are enabled; optionally registered. If registered, the input clock controls the input register, the output clock controls the output and OE registers. All registers can be positively or negatively triggered. Additionally, the input and output paths can be registered independently. The output register can be inverted.
Clock output	Clock output path is enabled.

Double-Data I/O

Ti180 FPGAs support double data I/O (DDIO) on input and output registers. In this mode, the DDIO register captures data on both positive and negative clock edges. The core receives 2 bit wide data from the interface.

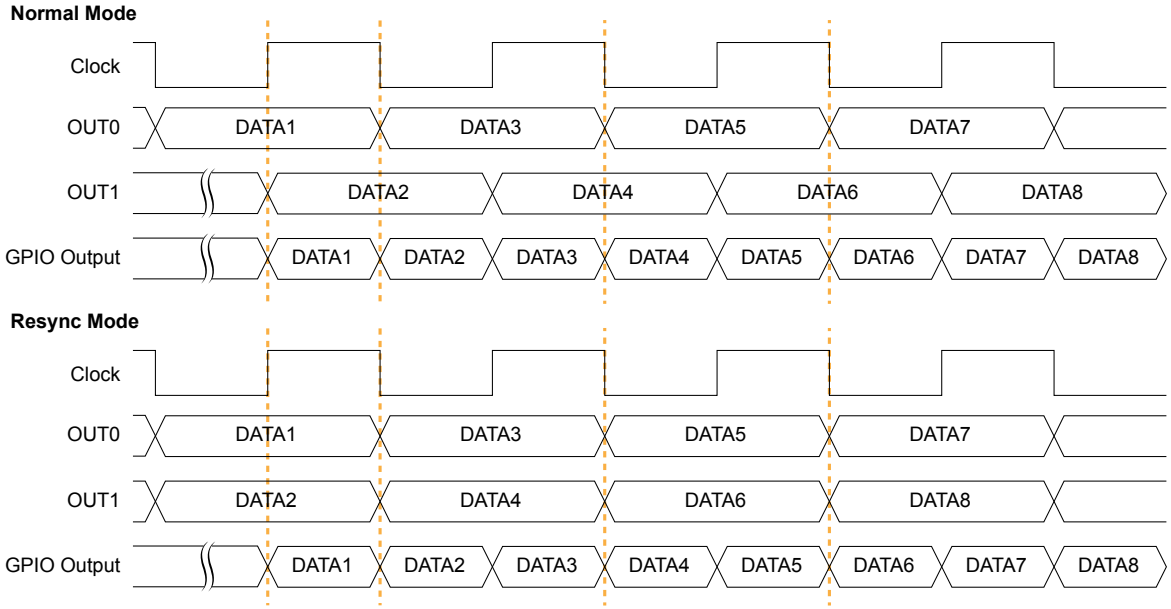
In normal mode, the interface receives or sends data directly to or from the core on the positive and negative clock edges. In resync and pipeline mode, the interface resynchronizes the data to pass both signals on the positive clock edge only.

Figure 16: DDIO Input Timing Waveform



In resync mode, the IN1 data captured on the falling clock edge is delayed one half clock cycle.
In the Interface Designer, IN0 is the HI pin name and IN1 is the LO pin name.

Figure 17: DDIO Output Timing Waveform



In the Interface Designer, OUT0 is the HI pin name and OUT1 is the LO pin name.

Programmable Delay Chains

The HVIO and HSIO configured as GPIO support programmable delay chain. In some cases you can use static and dynamic delays at the same time.

Table 9: Programmable Delay Support

GPIO Type	Delay Steps	
	Static Delay	Dynamic Delay
Single-Ended		
HVIO input	16	N/A
HVIO output	16	N/A
HSIO P pin input	16	64
HSIO P pin output	16	N/A
HSIO N pin input	16	N/A
HSIO N pin output	16	N/A
Differential		
HSIO TX	64	N/A
HSIO RX	64[3]	64[3]

Learn more: Refer to the following tables for the delay step size:

Table 73: Single-Ended I/O Programmable Delay Chain Step Size: Static on page 77

Table 74: Single-Ended I/O Programmable Delay Chain Step Size: Dynamic on page 77

Table 75: Differential I/O Programmable Delay Chain Step Size: Static and Dynamic on page 77

[3] You cannot use the static delay and dynamic delay simultaneously.

HVIO

The HVIOs are grouped into banks. Each bank has its own VCCIO33 that sets the bank voltage for the I/O standard. Each HVIO consists of I/O logic and an I/O buffer. I/O logic connects the core logic to the I/O buffers. I/O buffers are located at the periphery of the device.

Figure 18: HVIO Interface Block

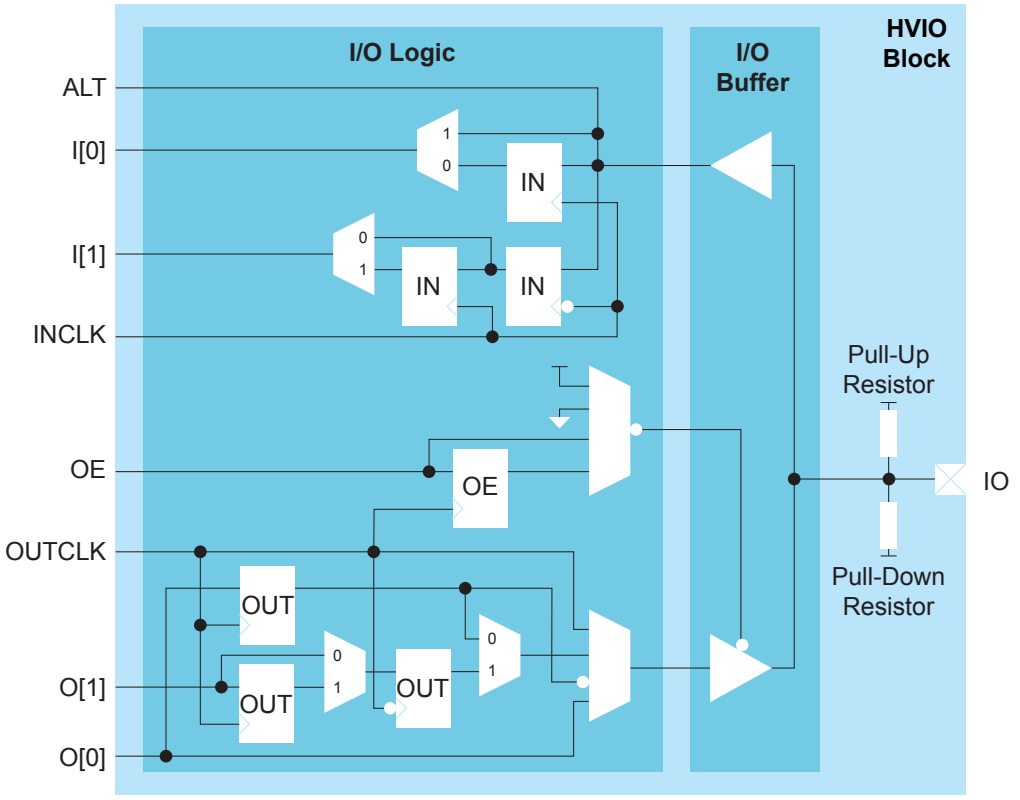


Table 10: HVIO Signals (Interface to FPGA Fabric)

Signal	Direction	Description
I[1:0]	Output	Input data from the HVIO pad to the core fabric. I[0] is the normal input to the core. In DDIO mode, I[0] is the data captured on the positive clock edge (HI pin name in the Interface Designer) and I[1] is the data captured on the negative clock edge (LO pin name in the Interface Designer).
ALT	Output	Alternative input connection (in the Interface Designer, **Register Option** is **none**). HVIO only support pll_clkin as the alternative connection.
O[1:0]	Input	Output data to HVIO pad from the core fabric. O[0] is the normal output from the core. In DDIO mode, O[0] is the data captured on the positive clock edge (HI pin name in the Interface Designer) and O[1] is the data captured on the negative clock edge (LO pin name in the Interface Designer).
OE	Input	Output enable from core fabric to the I/O block. Can be registered.
OUTCLK	Input	Core clock that controls the output and OE registers. This clock is not visible in the user netlist.
INCLK	Input	Core clock that controls the input registers. This clock is not visible in the user netlist.

Table 11: HVIO Pads

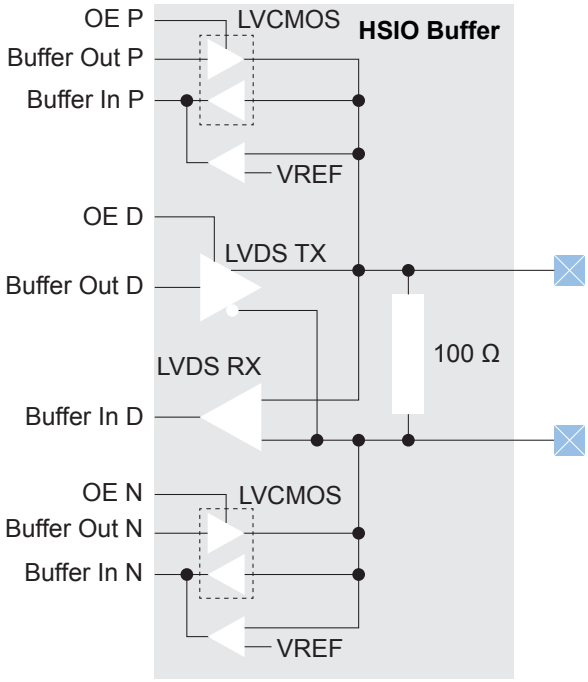
Signal	Direction	Description
IO	Bidirectional	HVIO pad.

HSIO

Each HSIO block uses a pair of I/O pins as one of the following:

- *Single-ended HSIO*—Two single-ended I/O pins (LVCMOS, SSTL, HSTL)
- *Differential HSIO*—One differential I/O pins:
  - Differential SSTL and HSTL
  - LVDS—Receiver (RX), transmitter (TX), or bidirectional (RX/TX)
  - MIPI lane I/O—Receiver (RX) or transmitter (TX)

Figure 19: HSIO Buffer Block Diagram



Important: When you are using an HSIO pin as a GPIO, make sure to leave at least one pair of unassigned HSIO pins between any GPIO and LVDS or MIPI lane pins. This rule applies for pins on each side of the device (top, bottom, left, right). This separation reduces noise. The Efinity software issues a warning if you do not leave this separation.

HSIO Configured as GPIO

You can configure each HSIO block as two GPIO (single-ended) or one GPIO (differential).

Figure 20: I/O Interface Block

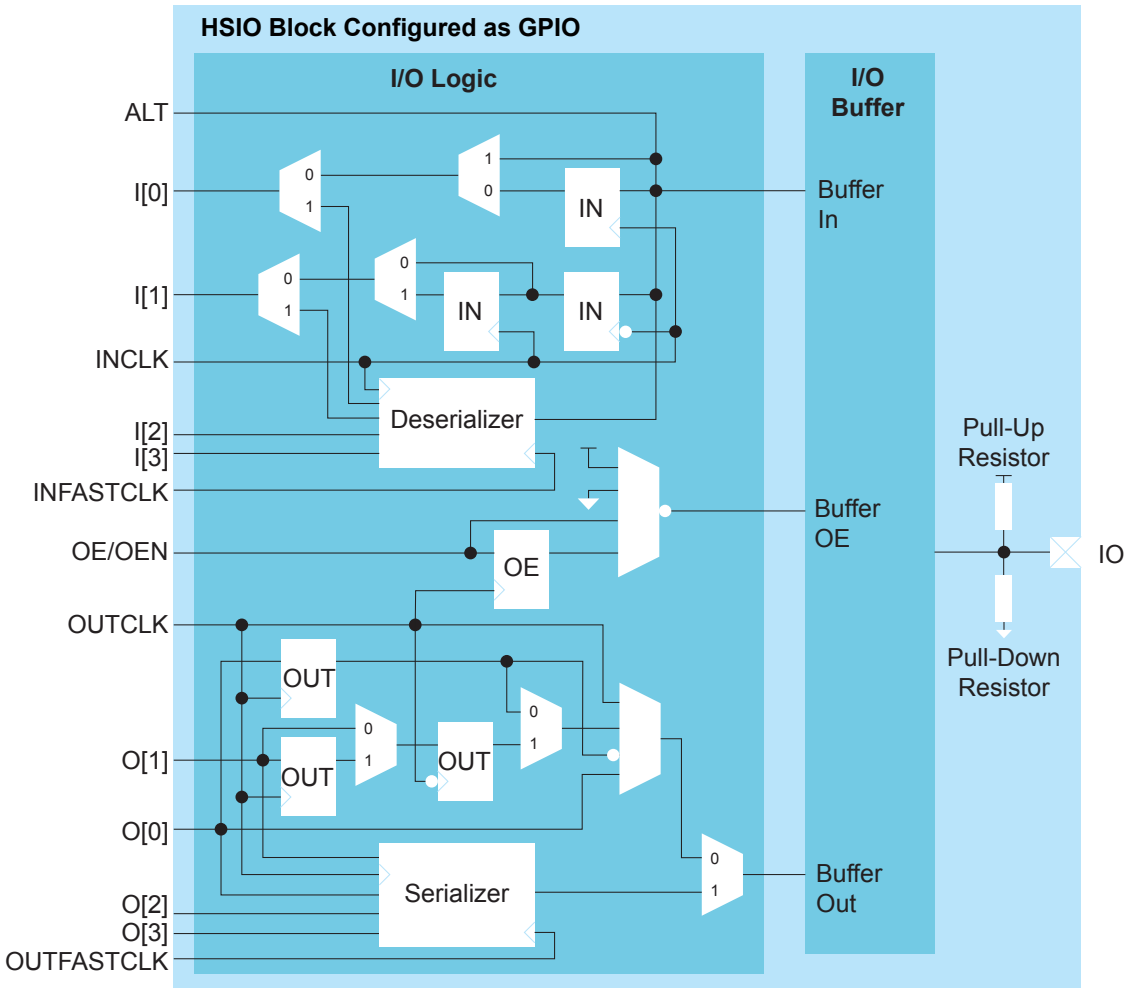


Table 12: HSIO Block Configured as GPIO Signals (Interface to FPGA Fabric)

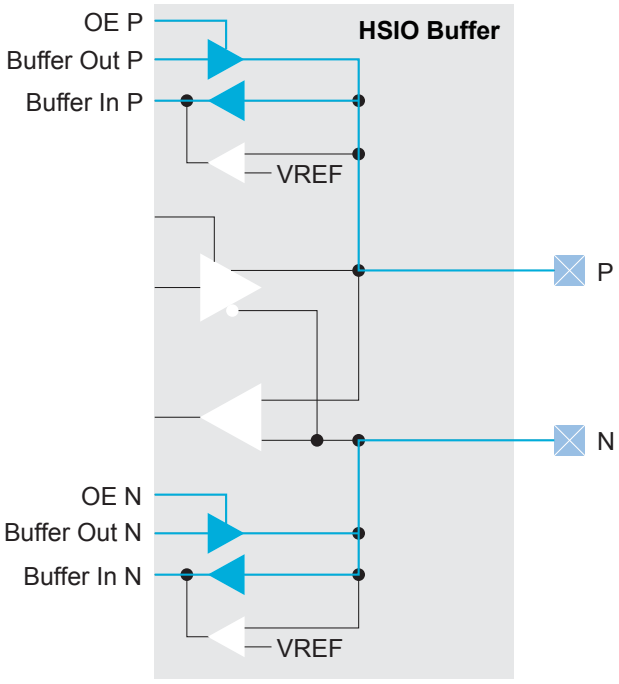
Signal	Direction	Description
I[3:0]	Output	Input data from the pad to the core fabric. I[0] is the normal input to the core. In DDIO mode, I[0] is the data captured on the positive clock edge (HI pin name in the Interface Designer) and I[1] is the data captured on the negative clock edge (LO pin name in the Interface Designer). When using the deserializer, the first bit is on I[0] and the last bit is on I[3].
ALT	Output	Alternative input connection for GCLK, PLL_CLKIN, RCLK, PLL_EXTFB, and VREF. (In the Interface Designer, **Register Option** is **none**).
O[3:0]	Input	Output data to GPIO pad from the core fabric. O[0] is the normal output from the core. In DDIO mode, O[0] is the data output on the positive clock edge (HI pin name in the Interface Designer) and O[1] is the data output on the negative clock edge (LO pin name in the Interface Designer). When using the serializer, the first bit is on O[0] and the last bit is on O[3].
OE/OEN	Input	Output enable from core fabric to the I/O block. Can be registered. OEN is used in differential mode. Drive it with the same signal as OE.
DLYCLK	Input	Delay clock for dynamic delay, sampled on the negative edge. In serializer mode, this clock must be the same clock as INCLK.
DLY_ENA	Input	(Optional) Enable the dynamic delay control.
DLY_INC	Input	(Optional) Dynamic delay control. When DLY_ENA = 1, 1: Increments 0: Decrements The updated delay count takes effect approximately 5 ns after the rising edge of the clock.
DLY_RST	Input	(Optional) Reset the delay counter.
OUTCLK	Input	Core clock that controls the output and OE registers. This clock is not visible in the user netlist.
OUTFASTCLK	Input	Core clock that controls the output serializer.
INCLK	Input	Core clock that controls the input registers. This clock is not visible in the user netlist.
INFASTCLK	Input	Core clock that controls the input serializer.

Table 13: GPIO Pads

Signal	Direction	Description
IO (P and N)	Bidirectional	GPIO pad.

The signal path from the pad through the I/O buffer changes depending on the I/O standard you are using. The following figures show the paths for the supported standards. The blue highlight indicates the path.

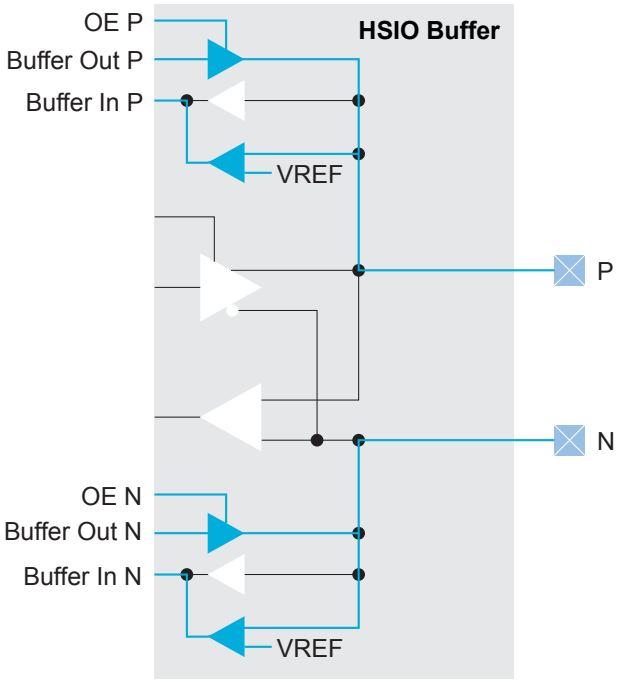
Figure 21: I/O Buffer Path for LVCMOS



When using an HSIO with the HSTL or SSTL I/O standards, you must configure an I/O pad of the standard's input path as a `VREF` pin. There is one programmable `VREF` per I/O bank.

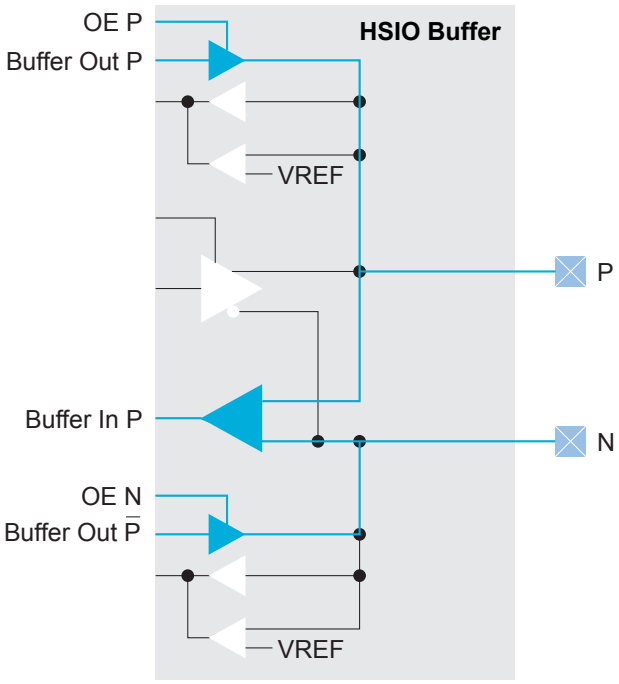
Important: When configuring an I/O pad of the standard's input path as a `VREF` pin, you must use the `VREF` from the same physical I/O bank even when the I/O banks are merged to share a common VCCIO pin.

Figure 22: I/O Buffer Path for HSTL and SSTL



When using an HSIO with the differential HSTL or differential SSTL standard, you must use both GPIO resources in the HSIO. You use the core interface pins associated with the P resource.

Figure 23: I/O Buffer Path for Differential HSTL and SSTL



HSIO Configured as LVDS

You can configure each HSIO block in RX, TX, or bidirectional LVDS mode. As LVDS, the HSIO has these features:

- Programmable V_{OD}, depending on the I/O standard used.
- Programmable pre-emphasis.
- Up to 1.5 Gbps.
- Programmable 100 Ω termination to save power (you can enable or disable it at runtime).
- LVDS input enable to dynamically enable/disable the LVDS input.
- Support for full rate or half rate serialization.
- Up to 10-bit serialization to support protocols such as 8b10b encoding.
- Programmable delay chains.
- Optional 8-word FIFO for crossing from the parallel (slow) clock to the user's core clock to help close timing (RX only).
- Dynamic phase alignment (DPA) that automatically eliminates skew for clock to data channels and data to data channels by adjusting a delay chain setting so that data is sampled at the center of the bit period. The DPA supports full-rate serialization mode only.

Table 14: Full and Half Rate Serialization

Mode	Description	Example
Full rate clock	In full rate mode, the fast clock runs at the same frequency as the data and captures data on the positive clock edge.	Data rate: 800 Mbps Serialization/Deserialization factor: 8 Slow clock frequency: 100 Mhz (800 Mbps / 8) Fast clock frequency: 800 Mhz
Half rate clock	In half rate mode, the fast clock runs at half the speed of the data and captures data on both clock edges.	Data rate: 800 Mbps Serialization / Deserialization factor: 8 Slow clock frequency: 100 Mhz (800 Mbps / 8) Fast clock frequency: 400 Mhz (800 / 2)

You use a PLL to generate the serial (fast) and parallel (slow) clocks for the LVDS pins. The slow clock runs at the data rate divided by the serialization factor.

LVDS RX

You can configure an HSIO block as one LVDS RX signal.

Figure 24: LVDS RX Interface Block Diagram

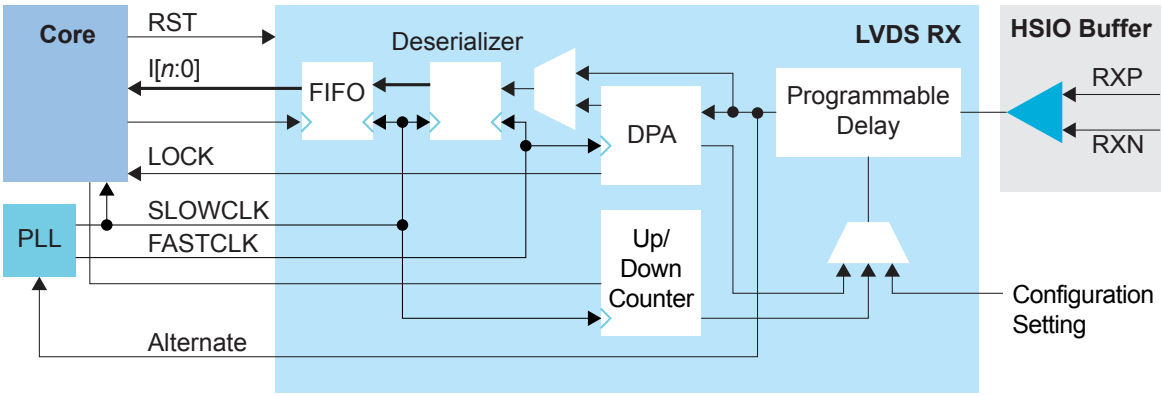
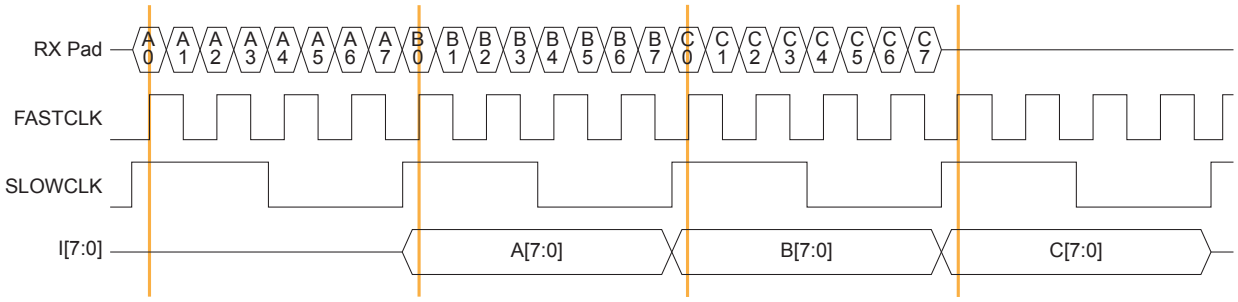


Table 15: LVDS RX Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Description
I[9:0]	Output	SLOWCLK	Parallel input data to the core. The width is programmable.
ALT	Output	–	Alternate input, only available for an LVDS RX resource in bypass mode (deserialization width is 1; alternate connection type). Alternate connections are PLL_CLKIN, PLL_EXTFB, GCLK, and RCLK.
SLOWCLK	Input	–	Parallel (slow) clock.
FASTCLK	Input	–	Serial (fast) clock.
FIFO_EMPTY	Output	FIFOCLK	This signal is required when you turn on the **Enable Clock Crossing FIFO** option. Indicates that the FIFO is empty.
FIFOCLK	Input	–	This signal is required when you turn on the **Enable Clock Crossing FIFO** option. Core clock to read from the FIFO.
FIFO_RD	Input	FIFOCLK	This signal is required when you turn on the **Enable Clock Crossing FIFO** option. Enables FIFO to read.
RST	Input	FIFOCLK SLOWCLK	(Optional) This signal is available when deserialization is enabled. Asynchronous. Resets the FIFO and deserializer. If the FIFO is enabled, it is relative to FIFOCLK; otherwise it is relative to SLOWCLK.
ENA	Input	–	Dynamically enable or disable the LVDS input buffer. Can save power when disabled. 1: Enabled 0: Disabled
TERM	Input	–	The signal is available when dynamic termination is enabled. Enables or disables termination in dynamic termination mode. 1: Enabled 0: Disabled
LOCK	Output	–	(Optional) This signal is available when you set **Delay Mode** to **dpa**. Indicates that the DPA has achieved training lock and data can be passed.
DLY_ENA	Input	SLOWCLK	This signal is required when you set **Delay Mode** to **dynamic** or **dpa**. Enable the dynamic delay control or the DPA circuit, depending on the LVDS RX delay settings.
DLY_INC	Input	SLOWCLK	This signal is required when you set **Delay Mode** to **dynamic**. Dynamic delay control. Cannot be used with DPA enabled. When DLY_ENA is 1: 1: Increments 0: Decrements
DLY_RST	Input	SLOWCLK	(Optional) This signal is available when you set **Delay Mode** to **dpa** or **dynamic**. Reset the delay counter or the DPA circuit, depending on the LVDS RX delay settings.
DBG[5:0]	Output	SLOWCLK	DPA debug pin. Outputs the final delay chain settings when DPA achieved lock.

The following waveform shows the relationship between the fast clock, slow clock, RX data coming in from the pad, and byte-aligned data to the core.

Figure 25: LVDS RX Timing Example Serialization Width of 8 (Half Rate)



I is byte-aligned data passed to the core on the rising edge of SLOWCLK.

Note: For LVDS RX interfaces with multiple LVDS RX lanes and an LVDS RX clock input, use the LVDS RX blocks from the same side of the FPGA to minimize skew between data lanes and RX clock input.

LVDS TX

You can configure an HSIO block as one LVDS TX signal. LVDS TX can be used in the serial data output mode or reference clock output mode.

Figure 26: LVDS TX Interface Block Diagram

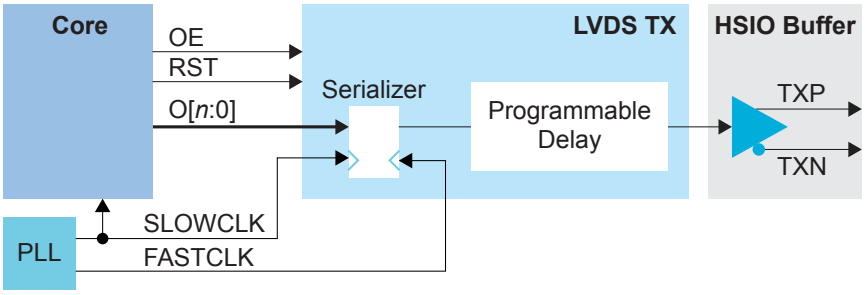
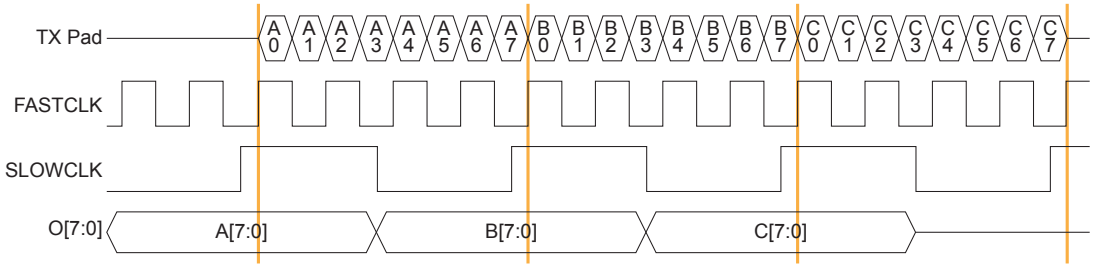


Table 16: LVDS TX Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Description
O[9:0]	Input	SLOWCLK	Parallel output data from the core. The width is programmable.
SLOWCLK	Input	–	Parallel (slow) clock.
FASTCLK	Input	–	Serial (fast) clock.
RST	Input	SLOWCLK	(Optional) This signal is available when serialization is enabled. Resets the serializer.
OE	Input	–	(Optional) Output enable signal.

The following waveform shows the relationship between the fast clock, slow clock, TX data going to the pad, and byte-aligned data from the core.

Figure 27: LVDS Timing Example Serialization Width of 8 (Half Rate)



OUT is byte-aligned data passed from the core on the rising edge of SLOWCLK.

Note: For LVDS TX interfaces with multiple LVDS TX lanes and an LVDS TX reference clock output, use the LVDS TX blocks from the same side of the FPGA to minimize skew between data lanes and TX reference clock output.

LVDS Bidirectional

You can configure an HSIO block as one LVDS bidirectional signal. You must use the same serialization for the RX and TX.

Figure 28: LVDS Bidirectional Interface Block Diagram

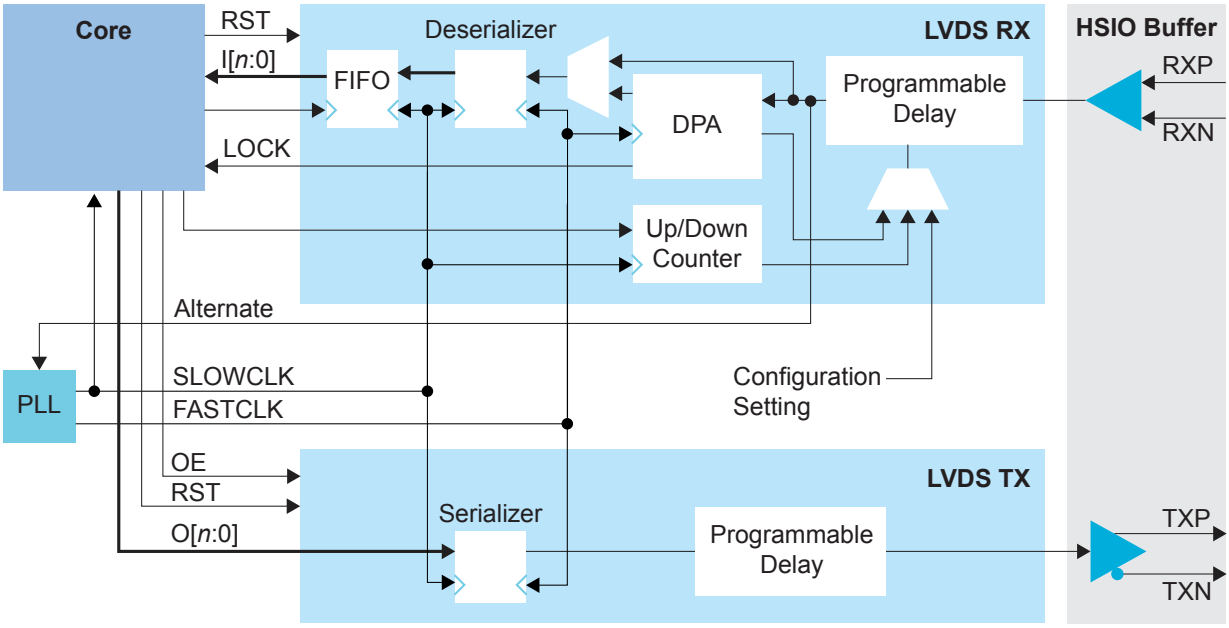


Table 17: LVDS Bidirectional Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Description
I[9:0]	Output	SLOWCLK	Parallel input data to the core. The width is programmable.
INSLOWCLK	Input	–	Parallel (slow) clock for RX.
INFASTCLK	Input	–	Serial (fast) clock for RX.
FIFO_EMPTY	Output	FIFOCLK	This signal is required when you turn on the **Enable Clock Crossing FIFO** option. Indicates that the FIFO is empty.
FIFOCLK	Input	–	This signal is required when you turn on the **Enable Clock Crossing FIFO** option. Core clock to read from the FIFO.
FIFO_RD	Input	FIFOCLK	This signal is required when you turn on the **Enable Clock Crossing FIFO** option. Enables FIFO to read.
INRST	Input	FIFOCLK SLOWCLK	This signal is available when deserialization is enabled. Asynchronous. Resets the FIFO and RX deserializer. If the FIFO is enabled, it is relative to FIFOCLK; otherwise it is relative to SLOWCLK.
ENA	Input	–	Dynamically enable or disable the LVDS input buffer. Can save power when disabled. 1: Enabled 0: Disabled
TERM	Input	–	The signal is available when dynamic termination is enabled. Enables or disables termination in dynamic termination mode. 1: Enabled 0: Disabled
LOCK	Output	–	(Optional) This signal is available when you set **Delay Mode** to **dpa**. Indicates that the DPA has achieved training lock and data can be passed.
DLY_ENA	Input	SLOWCLK	This signal is required when you set **Delay Mode** to **dynamic** or **dpa**. Enable the dynamic delay control or the DPA circuit, depending on the bidirectional LVDS delay settings.
DLY_INC	Input	SLOWCLK	This signal is required when you set **Delay Mode** to **dynamic**. Dynamic delay control. Cannot be used with DPA enabled. When DLY_ENA is 1, 1: Increments 0: Decrements

Signal	Direction	Clock Domain	Description
DLY_RST	Input	SLOWCLK	(Optional) This signal is available when you set **Delay Mode** to **dpa** or **dynamic**. Reset the delay counter or the DPA circuit, depending on the bidirectional LVDS delay settings.
DBG[5:0]	Output	SLOWCLK	DPA debug pin. Outputs the final delay chain settings when DPA achieved lock.
O[9:0]	Input	SLOWCLK	Parallel output data from the core. The width is programmable.
OUTSLOWCLK	Input	–	Parallel (slow) clock for TX.
OUTFASTCLK	Input	–	Serial (fast) clock for TX.
OUTRST	Input	SLOWCLK	This signal is available when serialization is enabled. Resets the TX serializer.
OE	Input	–	Output enable signal.

LVDS Pads

Table 18: LVDS Pads

Signal	Direction	Description
P	Output	Differential pad P.
N	Output	Differential pad N.

HSIO Configured as MIPI Lane

You can configure the HSIO block as a MIPI RX or TX lane. The block supports bidirectional data lane, unidirectional data lane, and unidirectional clock lane which can run at speeds up to 1.5 Gbps. The MIPI lane operates in high-speed (HS) and low-power (LP) modes. In HS mode, the HSIO block transmits or receives data with x8 serializer/deserializer. In LP mode, it transmits or receives data without deserializer/serializer.

The MIPI lane block does not include the MIPI D-PHY core logic. A full MIPI D-PHY solution requires:

- Multiple MIPI RX or TX lanes (at least a clock lane and a data lane)
- Soft MIPI D-PHY IP core programmed into the FPGA fabric

The MIPI D-PHY standard is a point-to-point protocol with one endpoint (TX) responsible for initiating and controlling communication. Often, the standard is unidirectional, but when implementing the MIPI DSI protocol, you can use one TX data lane for LP bidirectional communication.

The protocol is source synchronous with one clock lane and 1, 2, 4, or 8 data lanes. The number of lanes available depends on which package you are using. A dedicated HSIO block is assigned on the RX interface as a clock lane while the clock lane for TX interface can use any of the HSIO block in the group.

MIPI RX Lane

In RX mode, the HS (fast) clock comes in on the MIPI clock lane and is divided down to generate the slow clock. The fast and slow clocks are then passed to neighboring HSIO blocks to be used for the MIPI data lanes.

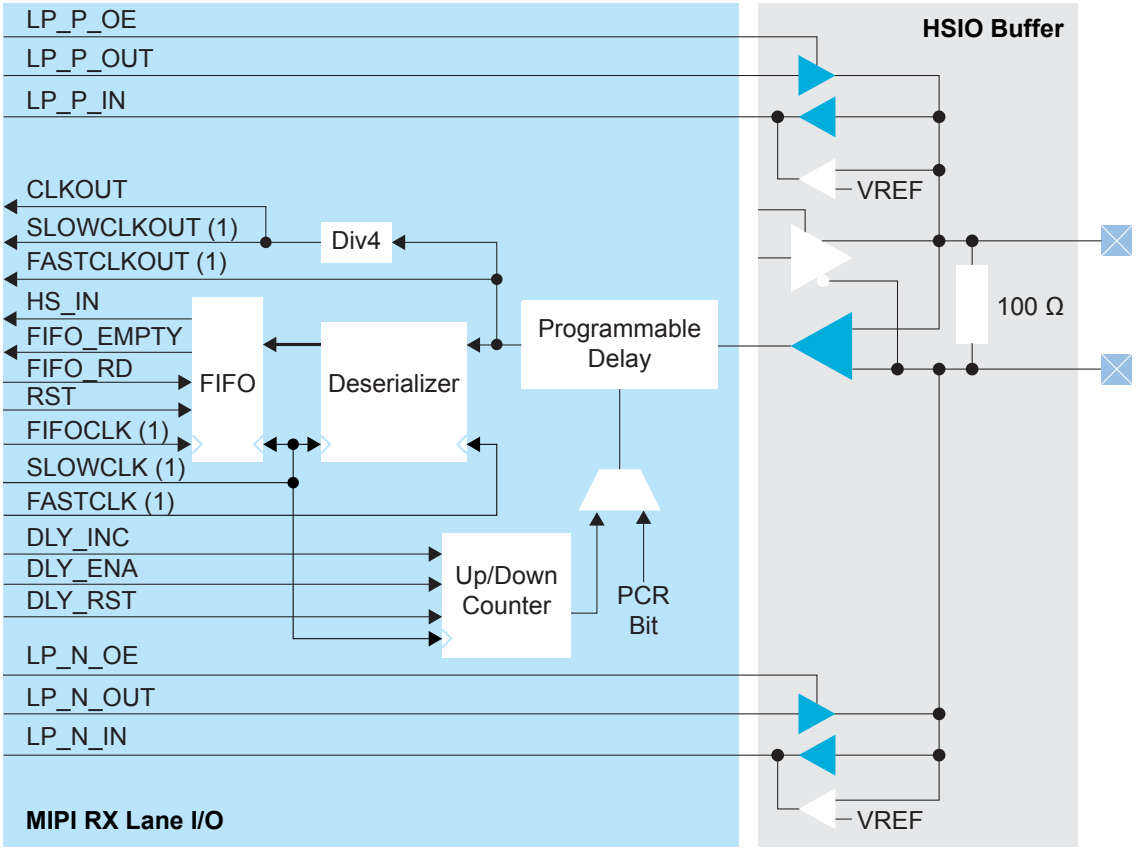
The data lane fast and slow clocks must be driven by a clock lane in the same MIPI group (dedicated buses drive from the clock lane to the neighboring data lanes).

The MIPI RX function is defined as:

Table 19: MIPI RX Function

MIPI RX Function	Description
RX_DATA_*xy_zz*	MIPI RX Data Lane. You can use any data lanes within the same group to form multiple lanes of MIPI RX channel. *x* = P or N *y* = 0 to 7 data lanes (Up to 8 data lanes per channel) *zz* = I0 to I17 MIPI RX channel (Up to 18 MIPI RX channels)
RX_CLK_*x_zz*	MIPI RX Clock Lane. One clock lane is required for each MIPI RX channel. *x* = P or N *zz* = I0 to I17 MIPI RX channel (Up to 18 MIPI RX channels)

Figure 29: MIPI RX Lane Block Diagram



Note:
1. These signals are in the primitive, but the software automatically connects them for you.

Table 20: MIPI RX Lane Signals

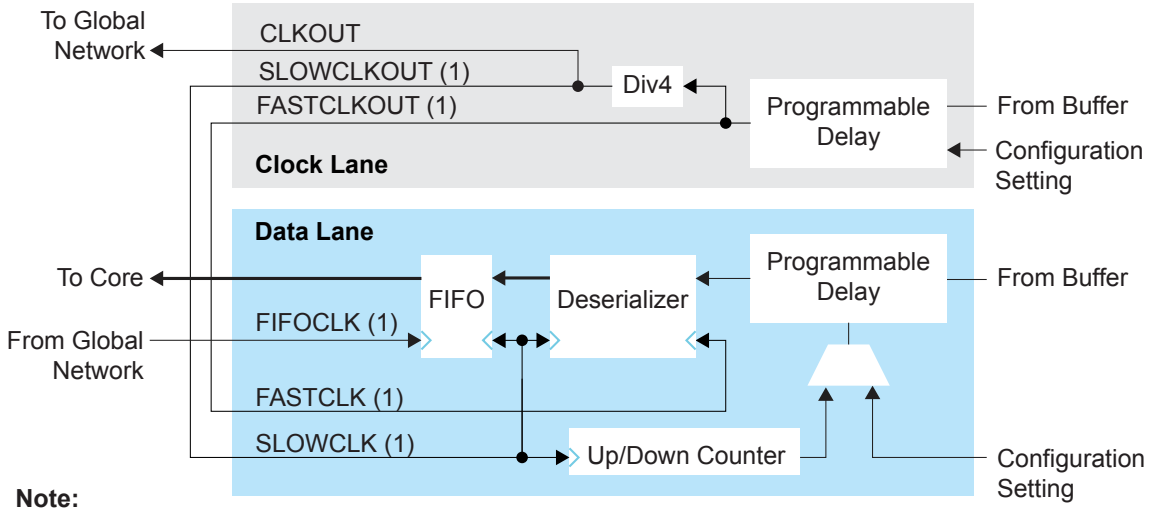
Interface to MIPI soft CSI/DSI controller with D-PHY in FPGA Fabric

Signal	Direction	Clock Domain	Description
LP_P_OE	Input	–	(Optional) LP output enable signal for P pad.
LP_P_OUT	Input	–	(Optional) LP output data from the core for the P pad. Used if the data lane is reversible.
LP_P_IN	Output	–	LP input data from the P pad.
CLKOUT	Output	–	Divided down parallel (slow) clock from the pads that can drive the core clock tree. Used to drive the core logic implementing the rest of the D-PHY protocol. It should also connect to the FIFOCLK of the data lanes.
SLOWCLKOUT[4]	Output	–	Divided down parallel (slow) clock from the pads. Can only drive RX DATA lanes.
FASTCLKOUT[4]	Output	–	Serial (fast) clock from the pads. Can only drive RX DATA lanes.
HS_IN[7:0]	Output	SLOWCLK	High-speed parallel data input.
FIFO_EMPTY	Output	FIFOCLK	(Optional) When the FIFO is enabled, this signal indicates that the FIFO is empty.
FIFO_RD	Input	FIFOCLK	(Optional) Enables FIFO to read.
RST	Input	FIFOCLK SLOWCLK	(Optional) Asynchronous. Resets the FIFO and serializer. If the FIFO is enabled, it is relative to FIFOCLK; otherwise it is relative to SLOWCLK.
FIFOCLK[4]	Input	–	(Optional) Core clock to read from the FIFO.
SLOWCLK[4]	Input	–	Parallel (slow) clock.
FASTCLK[4]	Input	–	Serial (fast) clock.
DLY_INC	Input	SLOWCLK	(Optional) Dynamic delay control. When DLY_ENA is 1, 1: Increments 0: Decrements
DLY_ENA	Input	SLOWCLK	(Optional) Enable the dynamic delay control.
DLY_RST	Input	SLOWCLK	(Optional) Reset the delay counter.
LP_N_OE	Input	–	(Optional) LP output enable signal for N pad.
LP_N_OUT	Input	–	(Optional) LP output data from the core for the N pad. Used if the data lane is reversible.
LP_N_IN	Output	–	LP input data from the N pad.
HS_ENA	Input	–	Dynamically enable the differential input buffer when in high-speed mode.
HS_TERM	Input	–	Dynamically enables input termination high-speed mode.

[4] These signals are in the primitive, but the software automatically connects them for you.

The clock lane generates the fast clock and slow clock for the RX data lanes within the interface group. It also generates a clock which is divided by 4 that feeds the global network. The following figure shows the clock connections between the clock and data lanes.

Figure 30: Connections for Clock and RX Data Lane in the Same MIPI RX Channel



Note:
1. The software automatically connects this signal for you.

MIPI TX Lane

In TX mode, a PLL generates the parallel and serial clocks and passes them to the clock and data lanes.

Figure 31: MIPI TX Lane Block Diagram

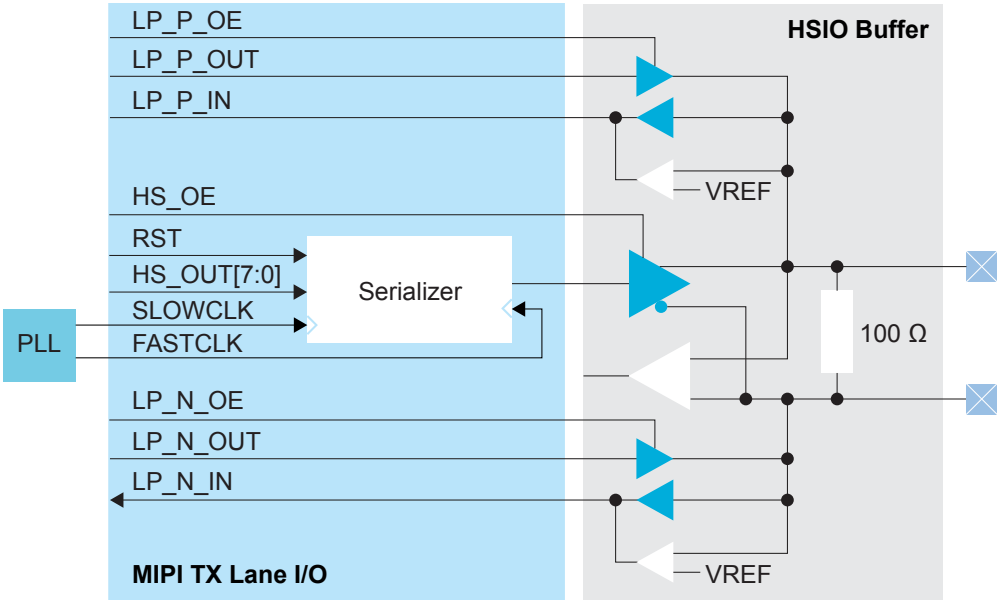


Table 21: MIPI TX Lane Signals

Interface to MIPI soft CSI/DSI controller with D-PHY in FPGA fabric

Signal	Direction	Clock Domain	Description
LP_P_OE	Input	–	LP output enable signal for P pad.
LP_P_OUT	Input	–	LP output data from the core for the P pad.
LP_P_IN	Output	–	(Optional) LP input data from the P pad. Used if data lane is reversible.
HS_OE	Input	–	High-speed output enable signal.
RST	Input	SLOWCLK	(Optional) Resets the serializer.
HS_OUT[7:0]	Input	SLOWCLK	High-speed output data from the core. Always 8-bits wide.
SLOWCLK	Input	–	Parallel (slow) clock.
FASTCLK	Input	–	Serial (fast) clock.
LP_N_OE	Input	–	LP output enable signal for N pad.
LP_N_OUT	Input	–	LP output data from the core for the N pad.
LP_N_IN	Output	–	(Optional) LP input data from the N pad. Used if data lane is reversible.

MIPI Lane Pads

Table 22: MIPI Lane Pads

Signal	Direction	Description
P	Bidirectional	Differential pad P.
N	Bidirectional	Differential pad N.

I/O Banks

Elitestek FPGAs have input/output (I/O) banks for general-purpose usage. Each I/O bank has independent power pins. The number and voltages supported vary by FPGA and package.

Some I/O banks are merged at the package level by sharing VCCIO pins, these are called merged banks. Merged banks have underscores (_) between banks in the VCCIO name (e.g., 1B_1C means VCCIO for bank 1B and 1C are connected). Some of the banks in a merged bank may not have available user I/Os in the package. The following table lists banks that have available user I/Os in a package.

Table 23: I/O Banks by Package

Package	I/O Banks	Voltage (V)	Dynamic Voltage Support	DDIO Support	Merged Banks
J361	2B, 2C, 3A, 3B, 4A, 4B, 4C	1.2, 1.35, 1.5, 1.8	–	All	2A_2B, 3B_3C
	BL, TL, TR, BR	1.8, 2.5, 3.0, 3.3	✓	All	–
J484	2B, 3A, 3B, 4A, 4B, 4C	1.2, 1.35, 1.5, 1.8	–	All	2A_2B_2C, 3B_3C
	BL, TL, TR, BR	1.8, 2.5, 3.0, 3.3	✓	All	–
L484	2B, 3A, 3B, 4A, 4B, 4C	1.2, 1.35, 1.5, 1.8	–	All	2A_2B_2C, 3B_3C
	BL, TL, TR, BR	1.8, 2.5, 3.0, 3.3	✓	All	–
G400, G529	2A, 2B, 2C, 3A, 3B, 3C, 4A, 4B, 4C	1.2, 1.35, 1.5, 1.8	–	All	–
	BL, TL, TR, BR	1.8, 2.5, 3.0, 3.3	✓	All	–

Learn more: Refer to the **Ti180 Pinout** for information on the I/O bank assignments.

DDR DRAM Interface

The DDR PHY interface supports LPDDR4/4x memories with x16 or x32 DQ widths and a memory controller hard IP block. The memory controller provides two full-duplex AXI4 buses to communicate with the FPGA core.

Note: The DDR PHY and controller are hard blocks; you cannot bypass the DDR DRAM memory controller to access the PHY directly for non-DDR memory controller applications.

Figure 32: DDR DRAM Block Diagram

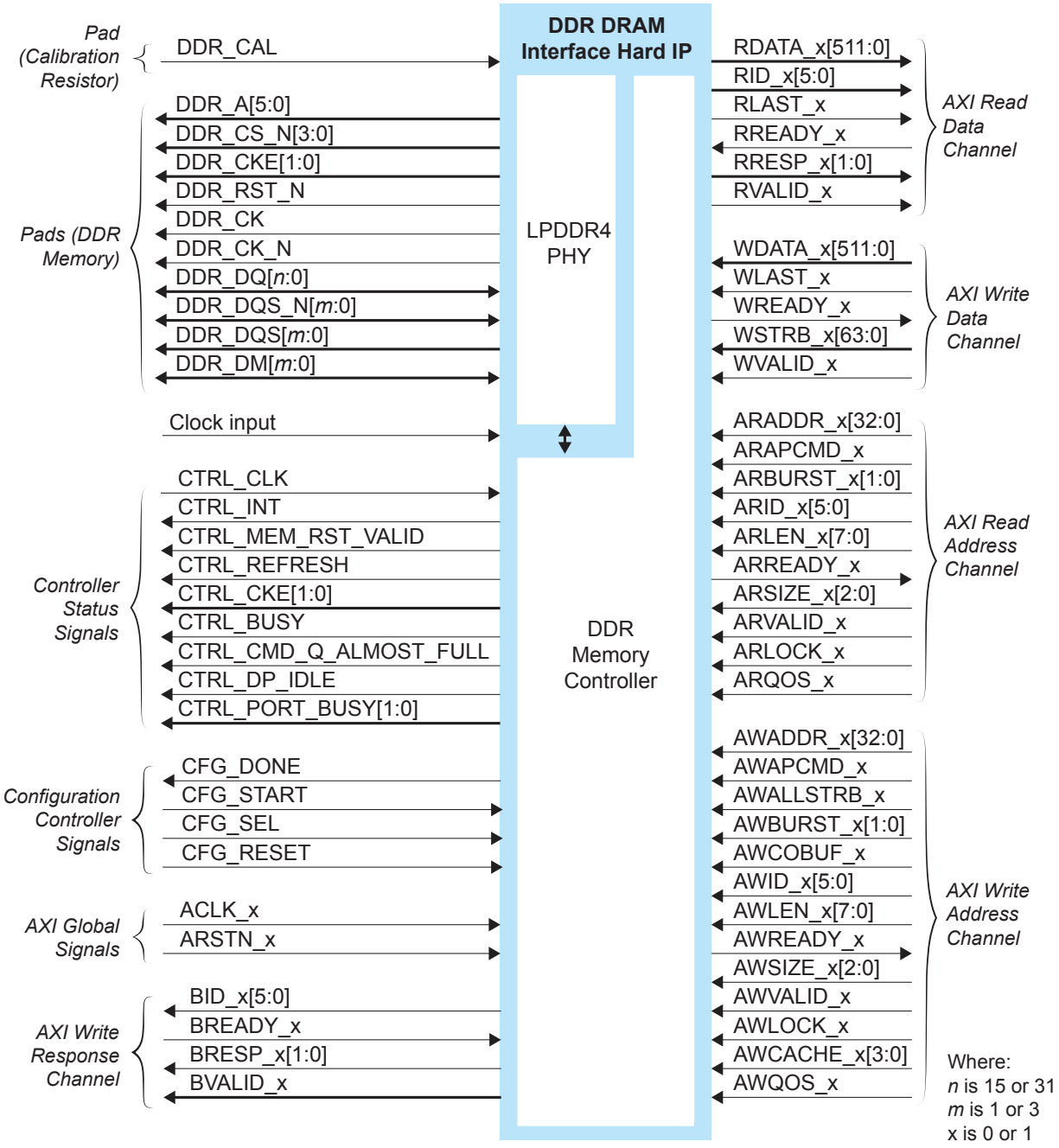
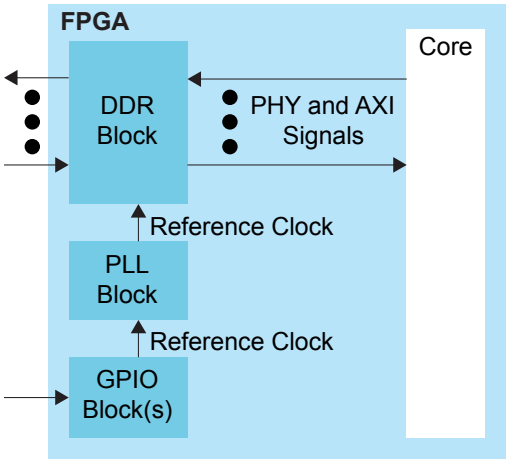


Figure 33: DDR DRAM Interface Block Diagram



Note: The PLL reference clock must be driven by I/O pads. The Efinity software issues a warning if you do not connect the reference clock to an I/O pad. (Using the clock tree may induce additional jitter and degrade the DDR performance.) Refer to **PLL** on page 56 for more information about the PLL block.

Table 24: DDR DRAM Pads

Signal	Direction	Description
DDR_A[5:0]	Output	Address signals to the DRAM.
DDR_CS_N[3:0]	Output	Chip select to the DRAM.
DDR_CKE[1:0]	Output	Active-high clock enable signals to the DRAM.
DDR_RST_N	Output	Active-low reset signal to the DRAM.
DDR_CK	Output	Differential clock signals to the DRAM.
DDR_CK_N	Output	
DDR_DQ[*n*:0]	Bidirectional	Data bus to/from the memories. For writes, the FPGA drives these signals. For reads, the memory drives these signals. These signals are connected to the DQ pins on the memories. *n* is 15 or 31 depending on the Data Width setting. If unused, can be left floating on the board.
DDR_DQS_N[*m*:0]	Bidirectional	Differential data strobes to/from the memories. For writes, the FPGA drives these signals. For reads, the memory drives these signals. These signals are connected to the DQS pins on the memories. *m* is 1or 3 depending on the DQ width. If unused, can be left floating on the board.
DDR_DQS[*m*:0]	Bidirectional	
DDR_DM[*m*:0]	Bidirectional	Signals used as active-high data-mask and data bus inversion indicator. *m* is 1 or 3 depending on the DQ width. If data bus inversion is enabled for a write operation, the DDR controller will drive the signal high if the write data byte is inverted. Similarly, if data bus inversion is enabled for a read operation, the memory device will drive the signal high if the read data byte is inverted. If unused, can be left floating on the board.

Table 25: Calibration Resistor Pad

Signal	Direction	Description
DDR_CAL	Input	Calibration resistor connection. Connect to the ground through a 240 Ω resistor on your board.

Table 26: Controller Status Signals

Signal	Direction	Clock Domain	Description
CTRL_CLK	Input	N/A	Clock for controller status signals.
CTRL_INT	Output	N/A	Controller detects Interrupt.

Signal	Direction	Clock Domain	Description
CTRL_MEM_RST_VALID	Output	N/A	Controller has been reset.
CTRL_REFRESH	Output	CTRL_CLK	Indicate controller is executing refresh command.
CTRL_CKE[1:0]	Output	CTRL_CLK	Delayed 'control_cke' from the controller, indicating that the memory is in self-refresh or power down mode.
CTRL_BUSY	Output	CTRL_CLK	Controller is busy reading data.
CTRL_CMD_Q_ALMOST_FULL	Output	CTRL_CLK	Command queue reached 'q_fullness' parameter.
CTRL_DP_IDLE	Output	CTRL_CLK	Datapath is idle.
CTRL_PORT_BUSY[1:0]	Output	CTRL_CLK	Indicate if port is reading data.

Table 27: Configuration Controller Signals

Signal	Direction	Description
CFG_RESET	Input	Active-high configuration controller reset. Asserting this signal also resets the DDR controller, PHY and the DRAM device.
CFG_START	Input	Start the configuration controller.
CFG_DONE	Output	Indicates the configuration controller is done
CFG_SEL	Input	Tie this input to low to enable the configuration controller.

Table 28: AXI4 Global Signals (Interface to FPGA Core Logic)

Signal	Direction	Clock Domain	Description
ACLK_*x*	Input	N/A	AXI4 clock inputs.
ARSTN_*x*	Input	ACLK_x	Active-low reset signal to the AXI interface.

Table 29: AXI4 Write Response Channel Signals (Interface to FPGA Core Logic)

Signal x is 0 or 1	Direction	Clock Domain	Description
BID_*x*[5:0]	Output	ACLK_x	Response ID tag. This signal is the ID tag of the write response.
BREADY_*x*	Input	ACLK_x	Response ready. This signal indicates that the master can accept a write response.
BRESP_*x*[1:0]	Output	ACLK_x	Read response. This signal indicates the status of the read transfer.
BVALID_*x*	Output	ACLK_x	Write response valid. This signal indicates that the channel is signaling a valid write response.

Table 30: AXI4 Read Data Channel Signals (Interface to FPGA Core Logic)

Signal x is 0 or 1	Direction	Clock Domain	Description
RDATA_*x*[511:0]	Output	ACLK_x	Read data.
RID_*x*[5:0]	Output	ACLK_x	Read ID tag. This signal is the identification tag for the read data group of signals generated by the slave.
RLAST_*x*	Output	ACLK_x	Read last. This signal indicates the last transfer in a read burst.
RREADY_*x*	Input	ACLK_x	Read ready. This signal indicates that the master can accept the read data and response information.
RRESP_*x*[1:0]	Output	ACLK_x	Read response. This signal indicates the status of the read transfer.
RVALID_*x*	Output	ACLK_x	Read valid. This signal indicates that the channel is signaling the required read data.

Table 31: AXI4 Write Data Channel Signals (Interface to FPGA Core Logic)

Signal x is 0 or 1	Direction	Clock Domain	Description
WDATA_*x*[511:0]	Input	ACLK_x	Write data.
WLAST_*x*	Input	ACLK_x	Write last. This signal indicates the last transfer in a write burst.
WREADY_*x*	Output	ACLK_x	Write ready. This signal indicates that the slave can accept the write data.
WSTRB_*x*[63:0]	Input	ACLK_x	Write strobes. This signal indicates which byte lanes hold valid data. There is one write strobe bit for each eight bits of the write data bus.
WVALID_*x*	Input	ACLK_x	Write valid. This signal indicates that valid write data and strobes are available.

Table 32: AXI4 Read Address Signals (Interface to FPGA Core Logic)

Signal x is 0 or 1	Direction	Clock Domain	Description
ARADDR_*x*[32:0]	Input	ACLK_x	Read address. It gives the address of the first transfer in a burst transaction.
ARBURST_*x*[1:0]	Input	ACLK_x	Burst type. The burst type and the size determine how the address for each transfer within the burst is calculated. 'b01 = INCR 'b10 = WRAP
ARID_*x*[5:0]	Input	ACLK_x	Address ID. This signal identifies the group of address signals.
ARLEN_*x*[7:0]	Input	ACLK_x	Burst length. This signal indicates the number of transfers in a burst.
ARREADY_*x*	Output	ACLK_x	Address ready. This signal indicates that the slave is ready to accept an address and associated control signals.
ARSIZE_*x*[2:0]	Input	ACLK_x	Burst size. This signal indicates the size of each transfer in the burst.
ARVALID_*x*	Input	ACLK_x	Address valid. This signal indicates that the channel is signaling valid address and control information.
ARLOCK_*x*	Input	ACLK_x	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
ARAPCMD_*x*	Input	ACLK_x	Read auto-precharge.
ARQOS_*x*	Input	ACLK_x	QoS identifier for read transaction.

Table 33: AXI4 Write Address Signals (Interface to FPGA Core Logic)

Signal x is 0 or 1	Direction	Clock Domain	Description
AWADDR_*x*[32:0]	Input	ACLK_x	Write address. It gives the address of the first transfer in a burst transaction.
AWBURST_*x*[1:0]	Input	ACLK_x	Burst type. The burst type and the size determine how the address for each transfer within the burst is calculated.
AWID_*x*[5:0]	Input	ACLK_x	Address ID. This signal identifies the group of address signals.
AWLEN_*x*[7:0]	Input	ACLK_x	Burst length. This signal indicates the number of transfers in a burst.
AWREADY_*x*	Output	ACLK_x	Address ready. This signal indicates that the slave is ready to accept an address and associated control signals.
AWSIZE_*x*[2:0]	Input	ACLK_x	Burst size. This signal indicates the size of each transfer in the burst.
AWVALID_*x*	Input	ACLK_x	Address valid. This signal indicates that the channel is signaling valid address and control information.
AWLOCK_*x*	Input	ACLK_x	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
AWAPCMD_*x*	Input	ACLK_x	Write auto-precharge.
AWQOS_*x*	Input	ACLK_x	QoS identifier for write transaction.
AWCACHE_*x*[3:0]	Input	ACLK_x	Memory type. This signal indicates how transactions are required to progress through a system.
AWALLSTRB_*x*	Input	ACLK_x	Write all strobes asserted. The DDR controller only supports a maximum of 16 AXI beats for write commands using this signal.
AWCOBUF_*x*	Input	ACLK_x	Write coherent bufferable selection. AWCACHE_*x* must be set to 'b1111 for AWCOBUF_*x* when: • 'b0 = Bvalid Response is returned when both command and data have been received by the port. • 'b1 = Bvalid Response is returned when command is accepted into the controller command queue. When AWCACHE_*x* is set to 'b0000: • Bvalid Response is returned when command is issued to PHY.

DDR DRAM Interface Input Clocks (J361, J484, and G529)

For these packages, you only need one clock to drive the DDR DRAM interface block. To select the PLL as the clock source for the DDR DRAM block, choose **CLKIN 0**, **CLKIN 1**, or **CLKIN 2** as the **Clock Source** in the Interface Designer.

Table 34: Input Clocks

DDR Block	PLL Resource			PLL CLKOUT
	CLKIN 0	CLKIN 1	CLKIN 2	
DDR 0	TL0	TL1	TL2	CLKOUT4

The clock runs at a quarter of the PHY data rate (for example, 2,000 Mbps requires a 500 MHz clock). You only need to instantiate the `CLKOUT4` of the selected PLL resource, enabled with the required frequencies. The Efinity software connects the clocks to the DDR DRAM interface block automatically.

DDR DRAM Interface Input Clocks (M484)

For the M484 package, the PLL_TL2 `CLKOUT3` and `CLKOUT4` are clocks to drive the DDR PHY and controller. The `CLKOUT3` drives the DDR PHY and must run at half of the PHY data rate (for example, 2,000 Mbps requires a 1,000 MHz clock). `CLKOUT4` drives the DDR controller and must run at a quarter of the PHY data rate (for example, 2,000 Mbps requires a 500 MHz clock). You only need to instantiate PLL_TL2 with `CLKOUT3` and `CLKOUT4`, enabled with the required frequencies. The Efinity software connects the clocks to the DDR DRAM interface block automatically.

MIPI D-PHY

In addition to the HSIO, which you can configure as MIPI RX or TX lanes, Ti180 FPGAs have hardened MIPI D-PHY blocks, each with 4 data lanes and 1 clock lane. The MIPI D-PHY RX and MIPI D-PHY TX can operate independently with dedicated I/O banks.

You can use the hardened MIPI D-PHY blocks along with the HSIO configured as MIPI D-PHY lanes to create systems that aggregate data from many cameras or sensors.

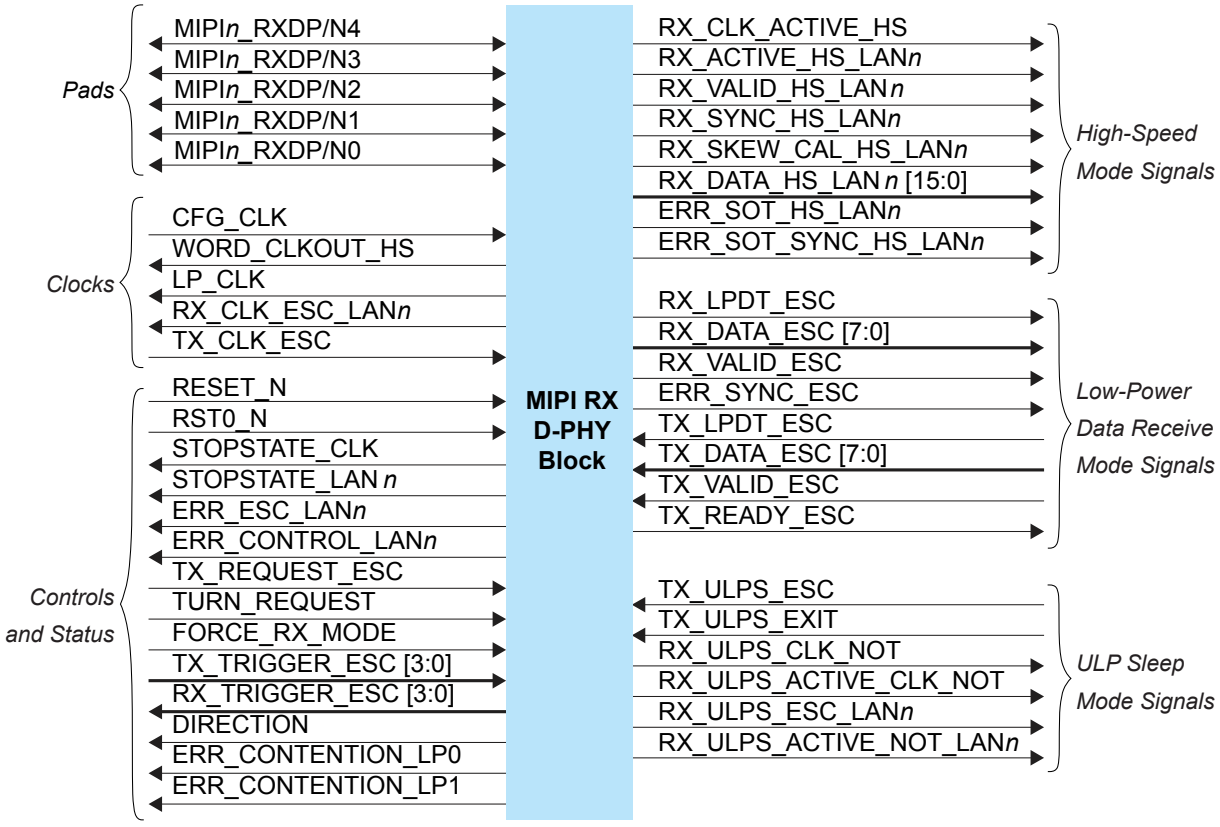
The MIPI TX/RX interface supports the MIPI D-PHY specification v1.1. It has the following features:

- Programmable data lane configuration supporting up to 4 lanes
- High-speed mode supports up to 2.5 Gbps data rates per lane
- Operates in continuous and non-continuous clock modes
- Supports Ultra-Low Power State (ULPS)

MIPI RX D-PHY

The MIPI RX D-PHY is a receiver interface designed to receive data and the control information of MIPI CSI, DSI, or other associated protocols. The MIPI RX D-PHY comprises of one clock lane and up to four data lanes for a single-channel configuration. The MIPI RX D-PHY also interfaces with MIPI-associated protocol controllers via a standard MIPI D-PHY PHY Protocol Interface (PPI) that supports the 8- or 16-bit high-speed receiving data bus.

Figure 34: MIPI RX D-PHY x4 Block Diagram



The status signals provide optional status and error information about the MIPI RX D-PHY interface operation.

Figure 35: MIPI RX D-PHY Interface Block Diagram

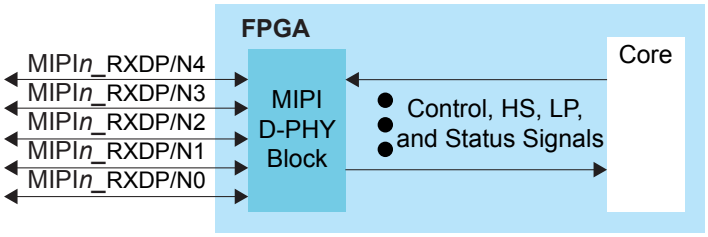


Table 35: MIPI RX D-PHY Clocks Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Notes
CFG_CLK	Input	N/A	Configuration Clock (used for time counter and EQ calibration). The clock must be between 80 MHz to 120 MHz.
WORD_CLKOUT_HS	Output	N/A	HS Receive Byte/Word clock.
LP_CLK	Output	N/A	Low Power State clock.
RX_CLK_ESC_LAN*n*	Output	N/A	Escape Mode Receive clock.
TX_CLK_ESC	Input	N/A	Escape Mode Transmit clock. The clock must be lower than 20 MHz.

Table 36: MIPI RX D-PHY Control and Status Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Notes
RESET_N	Input	N/A	Reset. Disables PHY and reset the digital logic.
RST0_N	Input	N/A	Asynchronous FIFO reset and synchronous out of reset.
STOPSTATE_CLK	Output	N/A	Lane in Stop State.
STOPSTATE_LAN*n*	Output	N/A	Data Lane in Stop State (Lane N).
ERR_ESC_LAN*n*	Output	N/A	Lane *n* Escape Command Error.
ERR_CONTROL_LAN*n*	Output	N/A	Lane *n* Has Line State Error.
TX_REQUEST_ESC	Input	TX_CLK_ESC	Lane 0 Request TX Escape Mode.
TURN_REQUEST	Input	TX_CLK_ESC	Lane 0 Request Turnaround.
FORCE_RX_MODE	Input	N/A	Lane 0 Force Lane into Receive Mode/Wait for Stop State.
TX_TRIGGER_ESC [3:0]	Input	TX_CLK_ESC	Lane 0 Send a Trigger Event.
RX_TRIGGER_ESC [3:0]	Output	RX_CLK_ESC_LAN0	Lane 0 Received a Trigger Event.
DIRECTION	Output	N/A	Lane 0 Transmit/Receive Direction (0 = TX, 1 = RX).
ERR_CONTENTION_LP0	Output	N/A	Lane 0 Contention Error when driving 0.
ERR_CONTENTION_LP1	Output	N/A	Lane 0 Contention Error when driving 1.

Table 37: MIPI RX D-PHY High-Speed Mode Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Notes
RX_CLK_ACTIVE_HS	Output	N/A	HS Clock Lane Active.
RX_ACTIVE_HS_LAN*n*	Output	WORD_CLKOUT_HS	HS Reception Active.
RX_VALID_HS_LAN*n*	Output	WORD_CLKOUT_HS	HS Data Receive Valid.
RX_SYNC_HS_LAN*n*	Output	WORD_CLKOUT_HS	HS Reveiver Sync. Observed.
RX_SKEW_CAL_HS_LAN*n*	Output	WORD_CLKOUT_HS	HS Reveiver DeSkew Burst Received.
RX_DATA_HS_LAN*n* [15:0]	Output	WORD_CLKOUT_HS	HS Receive Data.
ERR_SOT_HS_LAN*n*	Output	WORD_CLKOUT_HS	Start-of-Transmission (SOT) Error.
ERR_SOT_SYNC_HS_LAN*n*	Output	WORD_CLKOUT_HS	SOT Sync. Error.

Table 38: MIPI RX D-PHY Low-Power Data Receive Mode Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Notes
RX_LPDT_ESC	Output	RX_CLK_ESC_LAN0	Lane 0 enter LPDT RX Mode.
RX_DATA_ESC [7:0]	Output	RX_CLK_ESC_LAN0	Lane 0 LPDT RX Data.
RX_VALID_ESC	Output	RX_CLK_ESC_LAN0	Lane 0 LPDT RX Data Valid.
ERR_SYNC_ESC	Output	N/A	Lane 0 LPDT RX Data Sync. Error.
TX_LPDT_ESC	Input	TX_CLK_ESC	Lane 0 Enter LPDT TX Mode.
TX_DATA_ESC [7:0]	Input	TX_CLK_ESC	Lane 0 LPDT TX Data.
TX_VALID_ESC	Input	TX_CLK_ESC	Lane 0 LPDT TX Data Valid.
TX_READY_ESC	Output	TX_CLK_ESC	Lane 0 LDPT TX Data Ready.

Table 39: MIPI RX D-PHY ULP Sleep Mode Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Notes
TX_ULPS_ESC	Input	TX_CLK_ESC	Lane 0 Enter ULPS Mode.
TX_ULPS_EXIT	Input	TX_CLK_ESC	Lane 0 Exit ULPS Mode.
RX_ULPS_CLK_NOT	Output	N/A	CLK0 Enter ULPS Mode.
RX_ULPS_ACTIVE_CLK_NOT	Output	N/A	CLK0 is in ULPS (Active Low).
RX_ULPS_ESC_LAN*n*	Output	RX_CLK_ESC_LAN*n*	Lane *n* Enter ULPS Mode.
RX_ULPS_ACTIVE_NOT_LAN*n*	Output	N/A	Lane *n* is in ULPS (Active Low).

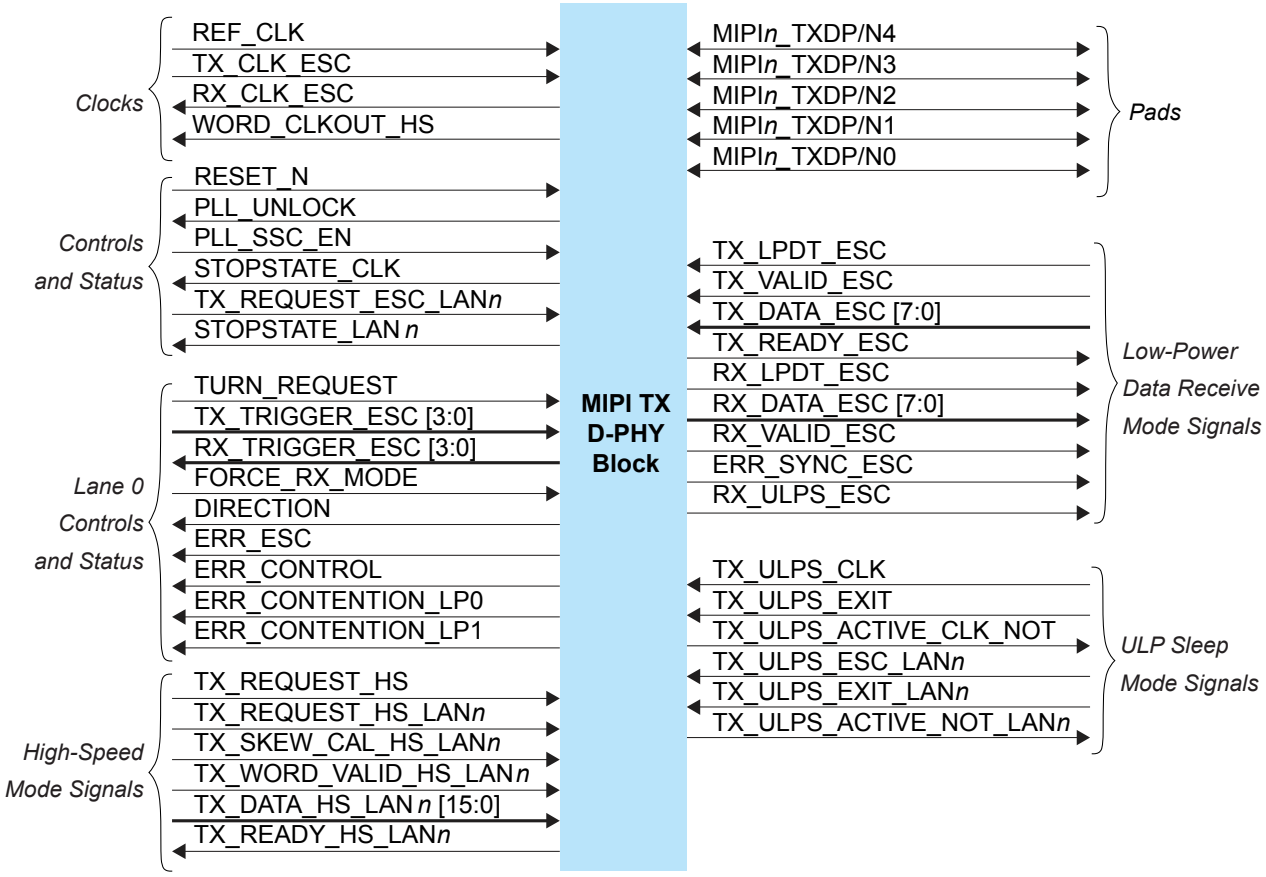
Table 40: MIPI RX D-PHY Pads

Pad	Direction	Description
MIPI*n*_RXDP[4:0]	Bidirectional	MIPI transceiver P pads.
MIPI*n*_RXDN[4:0]	Bidirectional	MIPI transceiver N pads.

MIPI TX D-PHY

The MIPI TX D-PHY is a transmitter interface designed to transmit data and the control information of MIPI CSI, DSI, or other associated protocols. The MIPI TX D-PHY comprises of one clock lane and up to four data lanes for a single-channel configuration. The MIPI TX D-PHY also interfaces with MIPI-associated protocol controllers via a standard MIPI D-PHY PPI that supports the 8- or 16-bit high-speed receiving data bus.

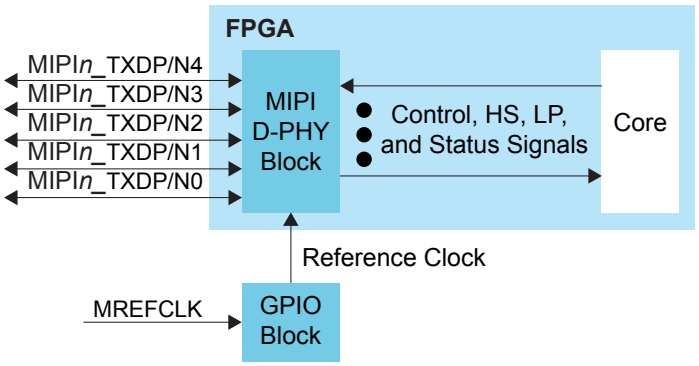
Figure 36: MIPI TX D-PHY x4 Block Diagram



The MIPI TX D-PHY block requires an escape clock (`TX_CLK_ESC`) for use when the MIPI interface is in escape (low-power) mode, which runs up to 20 MHz.

Note: Elitestek recommends that you set the escape clock frequency as close to 20 MHz as possible.

Figure 37: MIPI TX D-PHY Interface Block Diagram



Note: GPIO block is the default reference clock source. However, the PLL and core clock out can also be set as the reference clock source.

Table 41: MIPI TX D-PHY Clocks Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Notes
REF_CLK	Input	N/A	Reference Clock. The clock must be between 12 MHz to 52 MHz.
TX_CLK_ESC	Input	N/A	Escape Mode Transmit Clock, used to generate escape sequence. The clock must be less than 20 MHz.
RX_CLK_ESC	Output	N/A	Escape Mode Receive Clock (lane 0 only)
WORD_CLKOUT_HS	Output	N/A	HS Transmit Byte/Word Clock. This signal must be 1/8 of the bit-rate in normal 8-bit HS-PPI D-PHY mode, or 1/16 of the bit-rate in 16-bit PHY mode.

Table 42: MIPI TX D-PHY Control and Status Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Notes
RESET_N	Input	N/A	Reset. Disables PHY and reset the digital logic.
PLL_UNLOCK	Output	N/A	PLL is in unlock state.
PLL_SSC_EN	Input	N/A	(Optional) PLL SSC Enable: Always enable: 1 Disable: 0 Driven by active signal for dynamic enable
STOPSTATE_CLK	Output	N/A	Clock Lane in Stop State (Clk 0).
TX_REQUEST_ESC_LAN*n*	Input	TX_CLK_ESC	Escape Mode Transmit Request (Lane N).
STOPSTATE_LAN*n*	Output	N/A	Data Lane in Stop State (Lane N).

Table 43: MIPI TX D-PHY Lane 0 Control and Status Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Notes
TURN_REQUEST	Input	TX_CLK_ESC	Lane 0 Turnaround Request.
TX_TRIGGER_ESC [3:0]	Input	TX_CLK_ESC	Lane 0 Send an Escape Mode Trigger Event.
RX_TRIGGER_ESC [3:0]	Output	RX_CLK_ESC	Lane 0 Received an Escape Mode Trigger Event.
FORCE_RX_MODE	Input	N/A	Lane 0 Force into Receive Mode/Wait for Stop.
DIRECTION	Output	N/A	Lane 0 Transmit/Receive Direction: 0: TX, 1: RX
ERR_ESC	Output	N/A	Lane 0 Escape Command Error.
ERR_CONTROL	Output	N/A	Lane 0 Line State Error.
ERR_CONTENTION_LP0	Output	N/A	Lane 0 Line Contention Detected (when driving 0).
ERR_CONTENTION_LP1	Output	N/A	Lane 0 Line Contention Detected (when driving 1).

Table 44: MIPI TX D-PHY High Speed Mode Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Notes
TX_REQUEST_HS	Input	WORD_CLKOUT_HS	HS Clock Request (Clk 0).
TX_REQUEST_HS_LAN*n*	Input	WORD_CLKOUT_HS	HS Transmit Request and Data Valid (Lane 0-3).
TX_SKEW_CAL_HS_LAN*n*	Input	WORD_CLKOUT_HS	HS Skew Calibration (Lane N).
TX_WORD_VALID_HS_LAN*n*	Input	WORD_CLKOUT_HS	HS High Byte Valid (Lane N) for 16-bit mode.
TX_DATA_HS_LAN*n* [15:0]	Input	WORD_CLKOUT_HS	HS Transmit Data (Lane N).
TX_READY_HS_LAN*n*	Output	WORD_CLKOUT_HS	HS Transmit Ready (Lane N).

Table 45: MIPI TX D-PHY Low-Power Data Receive Mode Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Notes
TX_LPDT_ESC	Input	TX_CLK_ESC	Lane 0 Enter LPDT Mode.
TX_VALID_ESC	Input	TX_CLK_ESC	Lane 0 LPDT Data Valid .
TX_DATA_ESC [7:0]	Input	TX_CLK_ESC	Lane 0 LPDT Data Bus.
TX_READY_ESC	Output	TX_CLK_ESC	Lane 0 LPDT Data Ready.
RX_LDPT_ESC	Output	RX_CLK_ESC	Escape LP Data Receive Mode.
RX_DATA _ESC[7:0]	Output	RX_CLK_ESC	Escape Mode Receive Data.
RX_VALID_ESC	Output	RX_CLK_ESC	Escape Mode Receive Data Valid.
ERR_SYNC_ESC	Output	N/A	LPDT Data Sync Error.
RX_ULPS_ESC	Output	RX_CLK_ESC	Lane 0 entered ULPS mode.

Table 46: MIPI TX D-PHY ULP Sleep Mode (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Notes
TX_ULPS_CLK	Input	TX_CLK_ESC	CLK0 to enter Ultra-Low Power State.
TX_ULPS_EXIT	Input	TX_CLK_ESC	CLK0 to exit Ultra-Low Power State.
TX_ULPS_ACTIVE_CLK_NOT	Output	N/A	Clock Lane in ULP State - Active Low (Clk 0).
TX_ULPS_ESC_LAN*n*	Input	TX_CLK_ESC	Lane *n* to enter Ultra-Low Power State.
TX_ULPS_EXIT_LAN*n*	Input	TX_CLK_ESC	Lane *n* to exit Ultra-Low Power State.
TX_ULPS_ACTIVE_NOT_LAN*n*	Output	N/A	Data Lane in ULP State - Active Low (Lane N).

Table 47: MIPI TX D-PHY Pads

Pad	Direction	Description
MIPI*n*_TXDP[4:0]	Bidirectional	MIPI transceiver P pads.
MIPI*n*_TXDN[4:0]	Bidirectional	MIPI transceiver N pads.

Oscillator

The Ti180 has one low-frequency oscillator tailored for low-power operation. The oscillator runs at a nominal frequency of 10, 20, 40, or 80 MHz. You can use the oscillator to perform always-on functions with the lowest power possible. Its output clock is available to the core. You can enable or disable the oscillator to allow power savings when not in use. The oscillator has:

- An output duty cycle of 45% to 55%.
- A ±20% frequency variation from device to device.

PLL

Ti180 FPGAs have 8 PLLs to synthesize clock frequencies. The PLLs are located in the corners of the FPGA. You can use the PLL to compensate for clock skew/delay via external or internal feedback to meet timing requirements in advanced applications. The PLL reference clock has up to four sources. You can dynamically select the PLL reference clock with the `CLKSEL` port. (Hold the PLL in reset when dynamically selecting the reference clock source.)

The PLL consists of a pre-divider counter (N counter), a feedback multiplier counter (M counter), a post-divider counter (O counter), and output dividers (C).

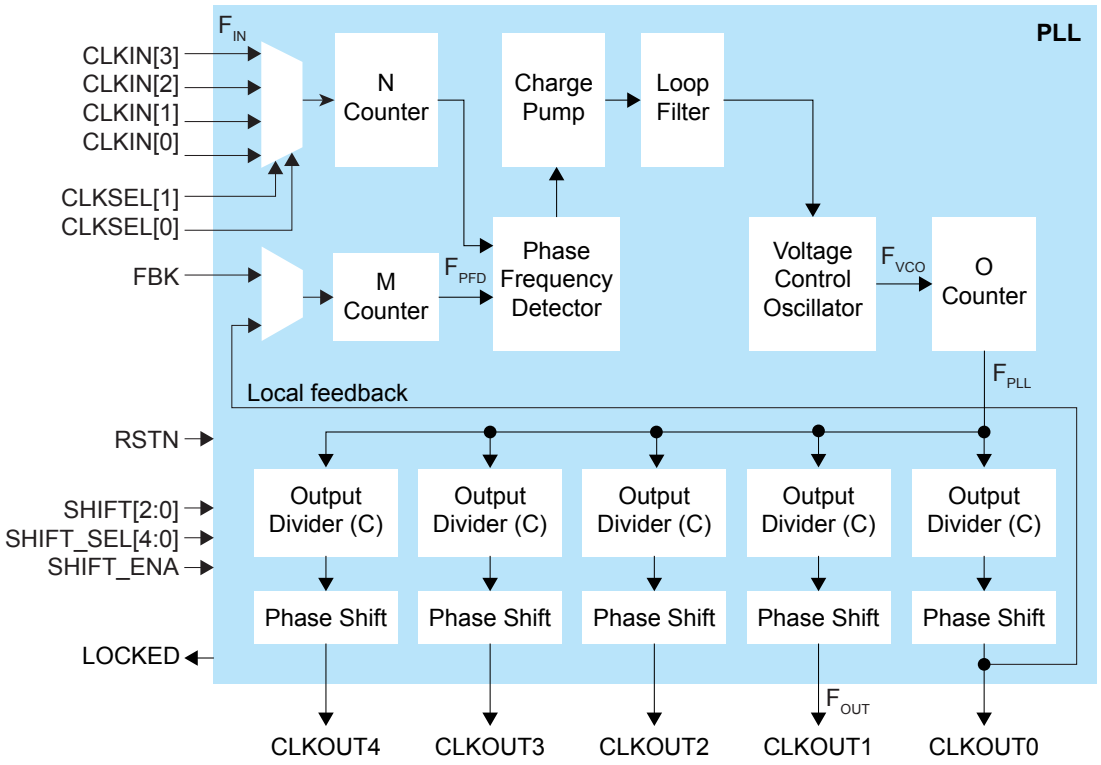
At startup, Elitestek recommends that you hold the PLL in reset until the PLL's reference clock source is stable.

Note: You can cascade PLLs. To avoid the PLL losing lock, Elitestek recommends that you do not cascade more than two PLLs.

At startup, Elitestek recommends resetting all cascaded PLLs. Hold the first PLL in reset until the PLL's reference clock source is stable. Hold the cascaded PLLs in reset until the previous PLL is locked.

Cascaded PLLs do not need a 50% duty cycle on the reference clock. However, the clock needs to meet the PLL minimum pulse width as specified in the data sheet.

Figure 38: PLL Block Diagram



The counter settings define the PLL output frequency:

Local and Core Feedback Mode	Where:
$F_{PFD} = F_{IN} / N$ $F_{VCO} = (F_{PFD} \times M \times O \times C_{FBK})$ [5] $F_{PLL} = F_{VCO} / O$ $F_{OUT} = (F_{IN} \times M \times C_{FBK}) / (N \times C)$	F_{VCO} is the voltage control oscillator frequency F_{PLL} is the post-divider PLL VCO frequency F_{OUT} is the output clock frequency F_{IN} is the reference clock frequency F_{PFD} is the phase frequency detector input frequency O is the post-divider counter C is the output divider

[5] $(M \times O \times C_{FBK})$ must be ≤ 255.

Note: Refer to the **PLL Timing and AC Characteristics** on page 84 for F_{VCO}, F_{OUT}, F_{IN}, F_{PLL}, and F_{PFD} values.

Figure 39: PLL Interface Block Diagram

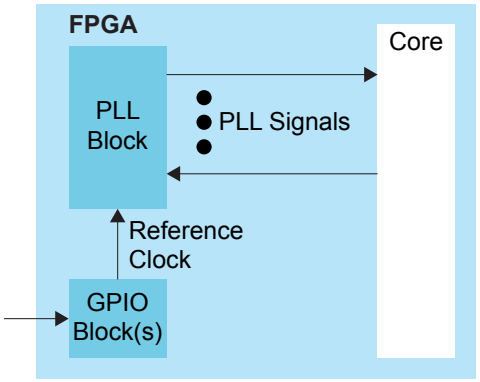


Table 48: PLL Signals (Interface to FPGA Fabric)

Signal	Direction	Description
CLKIN[3:0]	Input	Reference clocks driven by I/O pads or core clock tree.
CLKSEL[1:0]	Input	You can dynamically select the reference clock from one of the clock in pins.
RSTN	Input	Active-low PLL reset signal. When asserted, this signal resets the PLL; when de-asserted, it enables the PLL. De-assert only when the CLKIN signal is stable. Connect this signal in your design to power-up or reset the PLL. Assert the RSTN pin for a minimum pulse of 10 ns to reset the PLL. Assert RSTN when dynamically changing the selected PLL reference clock.
FBK	Input	Connect to a clock out interface pin when the PLL is in when the PLL is not in internal feedback mode.
CLKOUT0 CLKOUT1 CLKOUT2 CLKOUT3 CLKOUT4	Output	PLL output. You can route these signals as input clocks to the core's GCLK network. You can use CLKOUT0 only for clocks with a maximum frequency of 4x (integer) of the reference clock. If all your system clocks do not fall within this range, you should dedicate one unused clock for CLKOUT0.
LOCKED	Output	Goes high when PLL achieves lock; goes low when a loss of lock is detected. Connect this signal in your design to monitor the lock status. This signal is not synchronized to any clock and the minimum high or low pulse width of the lock signal may be smaller than the CLKOUT's period.
SHIFT[2:0]	Input	(Optional) Dynamically change the phase shift of the output selected to the value set with this signal. Possible values from 000 (no phase shift) to 111 (3.5 F_{PLL} cycle delay). Each increment adds 0.5 cycle delay.
SHIFT_SEL[4:0]	Input	(Optional) Choose the output(s) affected by the dynamic phase shift.
SHIFT_ENA	Input	(Optional) When high, changes the phase shift of the selected PLL(s) to the new value.

Table 49: PLL Reference Clock Resource Assignments (J361)

PLL	REFCLK0	REFCLK1	External Feedback I/O
PLL_BL0	Single-ended: GPIOB_P_00_PLLIN0	Single-ended: GPIOL_00_PLLIN1	Single-ended: GPIOB_P_01_EXTFB Differential: GPIOB_P_01_EXTFB, GPIOB_N_01_CCK
PLL_BL1	Single-ended: GPIOB_P_11_PLLIN0 Differential: GPIOB_P_11_PLLIN0, GPIOB_N_11	Unbonded[6]	Single-ended: GPIOB_P_12_EXTFB Differential: GPIOB_P_12_EXTFB, GPIOB_N_12_SSU_N
PLL_BL2	Single-ended: GPIOB_P_23_PLLIN0 Differential: GPIOB_P_23_PLLIN0, GPIOB_N_23_CDI12	Unbonded[6]	Single-ended: GPIOB_P_24_EXTFB Differential: GPIOB_P_24_EXTFB, GPIOB_N_24_CDI13
PLL_TL0	Unbonded[6]	Single-ended: GPIOL_26_PLLIN1	Unbonded[6]
PLL_TL1	Single-ended: GPIOT_P_11_PLLIN0 Differential: GPIOT_P_11_PLLIN0, GPIOT_N_11	Single-ended: GPIOL_36_PLLIN1	Single-ended: GPIOT_P_12_EXTFB Differential: GPIOT_P_12_EXTFB, GPIOT_N_12
PLL_TL2	Single-ended: GPIOT_P_23_PLLIN0 Differential: GPIOT_P_23_PLLIN0, GPIOT_N_23	Single-ended: GPIOL_32_PLLIN1	Single-ended: GPIOT_P_24_EXTFB Differential: GPIOT_P_24_EXTFB, GPIOT_N_24
PLL_TR	Single-ended: GPIOR_P_45_PLLIN0 Differential: GPIOR_P_45_PLLIN0, GPIOR_N_45	Single-ended: GPIOR_P_31_PLLIN1 Differential: GPIOR_P_31_PLLIN1, GPIOR_N_31	Single-ended: GPIOR_P_44_EXTFB Differential: GPIOR_P_44_EXTFB, GPIOR_N_44
PLL_BR	Unbonded[6]	Single-ended: GPIOR_P_16_PLLIN1 Differential: GPIOR_P_16_PLLIN1, GPIOR_N_16	Unbonded[6]

Table 50: PLL Reference Clock Resource Assignments (L484, J484, M484)

PLL	REFCLK0	REFCLK1	External Feedback I/O
PLL_BL0	Single-ended: GPIOB_P_00_PLLIN0	Single-ended: GPIOL_00_PLLIN1	Single-ended: GPIOB_P_01_EXTFB Differential: GPIOB_P_01_EXTFB, GPIOB_N_01_CCK
PLL_BL1	Single-ended: GPIOB_P_11_PLLIN0 Differential: GPIOB_P_11_PLLIN0, GPIOB_N_11	Unbonded[6]	Single-ended: GPIOB_P_12_EXTFB Differential: GPIOB_P_12_EXTFB, GPIOB_N_12_SSU_N
PLL_BL2	Single-ended: GPIOB_P_23_PLLIN0 Differential: GPIOB_P_23_PLLIN0, GPIOB_N_23_CDI12	Unbonded[6]	Single-ended: GPIOB_P_24_EXTFB Differential: GPIOB_P_24_EXTFB, GPIOB_N_24_CDI13
PLL_TL0	Unbonded[6]	Single-ended: GPIOL_26_PLLIN1	Unbonded[6]
PLL_TL1	Single-ended: GPIOT_P_11_PLLIN0 Differential: GPIOT_P_11_PLLIN0, GPIOT_N_11	Single-ended: GPIOL_36_PLLIN1	Single-ended: GPIOT_P_12_EXTFB Differential: GPIOT_P_12_EXTFB, GPIOT_N_12
PLL_TL2	Unbonded[6]	Single-ended: GPIOL_32_PLLIN1	Unbonded[6]
PLL_TR	Single-ended: GPIOR_P_45_PLLIN0 Differential: GPIOR_P_45_PLLIN0, GPIOR_N_45	Single-ended: GPIOR_P_31_PLLIN1 Differential: GPIOR_P_31_PLLIN1, GPIOR_N_31	Single-ended: GPIOR_P_44_EXTFB Differential: GPIOR_P_44_EXTFB, GPIOR_N_44
PLL_BR	Unbonded[6]	Single-ended: GPIOR_P_16_PLLIN1 Differential: GPIOR_P_16_PLLIN1, GPIOR_N_16	Unbonded[6]

[6] There is no dedicated pin assigned to this reference clock.

Table 51: PLL Reference Clock Resource Assignments (G400, G529)

PLL	REFCLK0	REFCLK1	External Feedback I/O
PLL_BL0	Single-ended: GPIOB_P_00_PLLIN0 Differential: GPIOB_P_00_PLLIN0, GPIOB_N_00	Single-ended: GPIOL_00_PLLIN1	Single-ended: GPIOB_P_01_EXTFB Differential: GPIOB_P_01_EXTFB, GPIOB_N_01_CCK
PLL_BL1	Single-ended: GPIOB_P_11_PLLIN0 Differential: GPIOB_P_11_PLLIN0, GPIOB_N_11	Single-ended: GPIOL_10_PLLIN1	Single-ended: GPIOB_P_12_EXTFB Differential: GPIOB_P_12_EXTFB, GPIOB_N_12_SSU_N
PLL_BL2	Single-ended: GPIOB_P_23_PLLIN0 Differential: GPIOB_P_23_PLLIN0, GPIOB_N_23_CDI12	Single-ended: GPIOL_20_PLLIN1	Single-ended: GPIOB_P_24_EXTFB Differential: GPIOB_P_24_EXTFB, GPIOB_N_24_CDI13
PLL_TL0	Single-ended: GPIOT_P_00_PLLIN0 Differential: GPIOT_P_00_PLLIN0, GPIOT_N_00	Single-ended: GPIOL_26_PLLIN1	Single-ended: GPIOT_P_01_EXTFB Differential: GPIOT_P_01_EXTFB, GPIOT_N_01
PLL_TL1	Single-ended: GPIOT_P_11_PLLIN0 Differential: GPIOT_P_11_PLLIN0, GPIOT_N_11	Single-ended: GPIOL_36_PLLIN1	Single-ended: GPIOT_P_12_EXTFB Differential: GPIOT_P_12_EXTFB, GPIOT_N_12
PLL_TL2	Single-ended: GPIOT_P_23_PLLIN0 Differential: GPIOT_P_23_PLLIN0, GPIOT_N_23	Single-ended: GPIOL_32_PLLIN1	Single-ended: GPIOT_P_24_EXTFB Differential: GPIOT_P_24_EXTFB, GPIOT_N_24
PLL_TR	Single-ended: GPIOR_P_45_PLLIN0 Differential: GPIOR_P_45_PLLIN0, GPIOR_N_45	Single-ended: GPIOR_P_31_PLLIN1 Differential: GPIOR_P_31_PLLIN1, GPIOR_N_31	Single-ended: GPIOR_P_44_EXTFB Differential: GPIOR_P_44_EXTFB, GPIOR_N_44
PLL_BR	Single-ended: GPIOR_P_00_PLLIN0 Differential: GPIOR_P_00_PLLIN0, GPIOR_N_00	Single-ended: GPIOR_P_16_PLLIN1 Differential: GPIOR_P_16_PLLIN1, GPIOR_N_16	Single-ended: GPIOR_P_01_EXTFB Differential: GPIOR_P_01_EXTFB, GPIOR_N_01

Dynamic Phase Shift

Ti180 FPGAs support a dynamic phase shift where you can adjust the phase shift of each output dynamically in user mode by up to 3.5 F_{PLL} cycles. For example, to phase shift a 400 MHz clock by 90-degree, configure the PLL to have a F_{PLL} frequency of 800 MHz, set the output counter division to 2, and set `SHIFT[2:0]` to `001`.

Implementing Dynamic Phase Shift

Use these steps to implement the dynamic phase shift:

1. Write the new phase setting into `SHIFT[2:0]`.
2. After one clock cycle of the targeted output clock that you want to shift, assert the `SHIFT_SEL[n]` and `SHIFT_ENA` signals.
3. Hold `SHIFT_ENA` and `SHIFT_SEL[n]` high for a minimum period of four clock cycles of the targeted output clock.
4. De-assert `SHIFT_ENA` and `SHIFT_SEL[n]`. Wait for at least four clock cycles of the targeted output clock before asserting `SHIFT_ENA` and `SHIFT_SEL[n]` again.

Note: *n* in `SHIFT_SEL[n]` represents the output clock that you intend to add phase shift.

The following waveforms describe the signals for a single phase shift and consecutive multiple phase shifts.

Figure 40: Single Dynamic Phase Shift Waveform Example for CLKOUT1

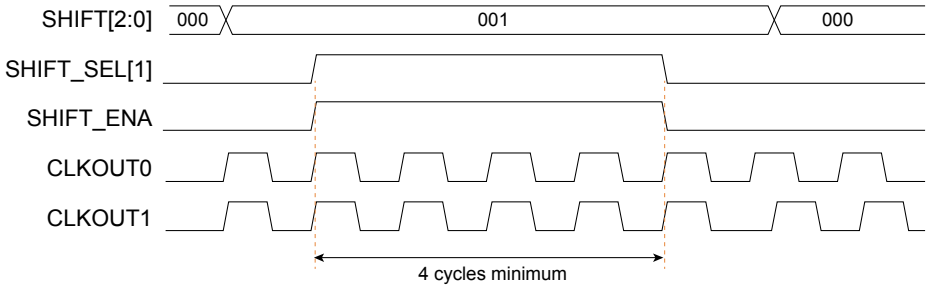
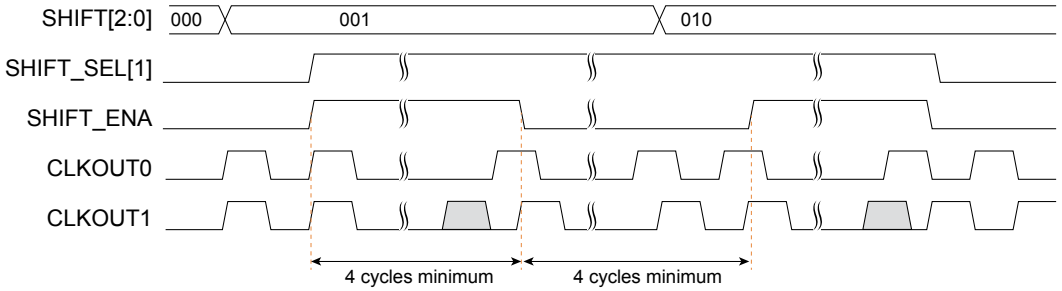


Figure 41: Consecutive Dynamic Phase Shift Waveform Example for CLKOUT1



Spread-Spectrum Clocking PLL

The Ti180 MIPI D-PHY interface includes a spread-spectrum clocking (SSC) PLL that spreads or varies the signal spectrum around the ideal clock frequency. If you are not using the MIPI D-PHY TX interface for MIPI signals, you can use the SSC PLL as another clock source.

The PLL consists of a pre-divider counter (N counter), a feedback multiplier counter (M counter), a post-divider counter (O counter), and output divider (C). You cannot modify the counter settings. Instead, you specify the output frequency you want and the reference clock frequency. If the SSC PLL cannot exactly match the output frequency, it displays (and uses) the frequency that is closest to your setting.

By default, the SSC PLL acts as a regular PLL. You enable the spread-spectrum clocking by turning on the **Enable Spread Spectrum Clock (SSC)** option in the Interface Designer.

Figure 42: SSC PLL Block Diagram

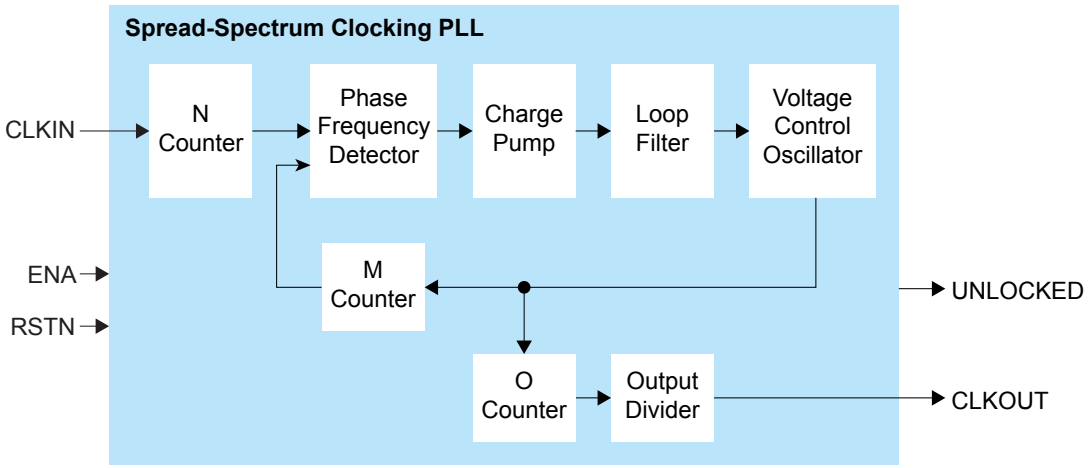


Figure 43: SSC PLL Interface Block Diagram

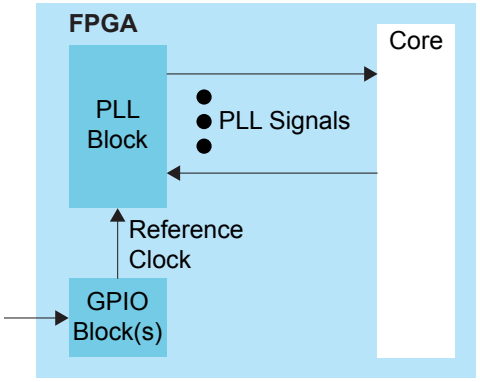


Table 52: SSC PLL Signals (Interface to FPGA Fabric)

Signal	Direction	Description
CLKIN	Input	Reference clocks from core, PLL, or GPIO.
CLKOUT	Output	PLL SSC Clock Out Pin Name.
RSTN	Input	Active-low PLL SSC reset signal.
UNLOCKED	Output	PLL Unlock State Pin Name. Goes high when PLL SSC is in unlock state. Connect this signal in your design to monitor the lock status.
ENA	Input	(Optional) PLL SSC Enable Pin Name: Always enable: 1 Disable: 0 Can be driven by an active signal for dynamic enable.

Single-Event Upset Detection

The Ti180 FPGA has a hard block for detecting single-event upset (SEU). The SEU detection feature has two modes:

- *Auto mode*—The Ti180 control block periodically runs SEU error checks and flags if it detects an error. You can configure the interval time between SEU checks.
- *Manual mode*—The user design runs the check.

In both modes, the user design is responsible for deciding whether to reconfigure the Ti180 when an error is detected.

Learn more: For more information on using the SEU detection feature, refer to the TJ-Series Interfaces User Guide.

Important: For applications that require the SEU feature, you must implement an external system-level primary functional detection mechanism. You should only use the TJ-Series FPGA SEU detection feature as a secondary indicator and it should not take precedence over the primary detection mechanism.

Note: Contact your local Elitestek representative for more system-level design details if your application needs both Over-the-Air and SEU detection.

Internal Reconfiguration Block

The Ti180 FPGAs have built-in hardware that supports an internal reconfiguration feature. The Ti180 can reconfigure itself from a bitstream image stored in flash memory.

Note: Refer to **AN 010: Using the Internal Reconfiguration Feature to Update Efinix FPGAs Remotely** for details regarding reconfiguration.

Security Feature

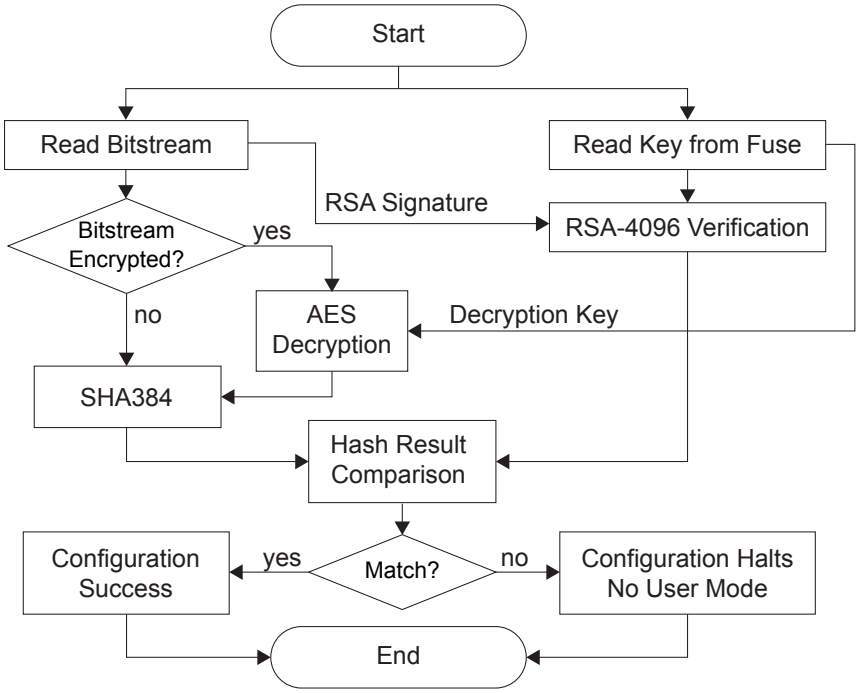
The FPGA security feature includes:

- Intellectual property protection using bitstream encryption with the AES-GCM-256 algorithm
- Anti-tampering support using asymmetric bitstream authentication with the RSA-4096 algorithm

Important: You cannot enable the FPGA security features when using compressed bitstreams.

You can enable encryption, authentication, or both. You enable the security features at the project level.

Figure 44: Security Flow



Download: Refer to the "Securing Bitstreams" section of the "Configuring an FPGA" chapter in the Efinity Software User Guide for instructions on how to enable these features.

Bitstream Encryption

Symmetric bitstream encryption uses a 256-bit key and the AES-GCM-256 algorithm. You create the key and then use it to encrypt the bitstream. You also need to store the key into the FPGA's fuses. During configuration, the built-in AES-GCM-256 engine decrypts the encrypted configuration bitstream using the stored key. Without the correct key, the bitstream decryption process cannot recover the original bitstream.

Bitstream Authentication

For bitstream authentication, you use a public/private key pair and the RSA-4096 algorithm. You create a public/private key pair and sign the bitstream with the private key. Then, you save a hashed version of the public key into fuses in the FPGA. During configuration, the FPGA validates the signature on the bitstream using the public key.

If the signature is valid, the FPGA knows that the bitstream came from a trusted source and has not been altered by a third party. The FPGA continues configuring normally and goes into user mode. If the signature is invalid, the FPGA stops configuration and does not go into user mode.

The private key remains on your computer and is not shared with anyone. The FPGA only has the public key: the bitstream contains the public key data and a signature, while the fuses contain a hashed public key. You can only sign the bitstream with the private key. An attacker cannot re-sign a tampered bitstream without the private key.

Disabling JTAG Access

Ti180 FPGA's support JTAG blocking, which disables JTAG access to the FPGA by blowing a fuse. Once the fuse is blown, you cannot perform any JTAG operation except for reading the FPGA `IDCODE`, reading `DEVICE_STATUS`, using `SAMPLE/PRELOAD`, and enabling `BYPASS` mode. To fully secure the FPGA, you **must** blow the JTAG fuse.

If you still want to use the JTAG interface for debugging, you can use the **DISABLE_EFUSE_ONLY** option, which permanently disables the JTAG efuse instructions only. Other JTAG instructions are not affected, for example, you can still perform debugging. Refer to "Using the Efinity Bitstream Security Key Generator" in the **Efinity Software User Guide** for more information.

Important: Once you disable JTAG by blowing the fuse, however, you cannot use JTAG ever again in that FPGA (except for `IDCODE`, `DEVICE_STATUS`, `SAMPLE/PRELOAD`, and `BYPASS`). So blowing this fuse should be the very last step in your manufacturing process.

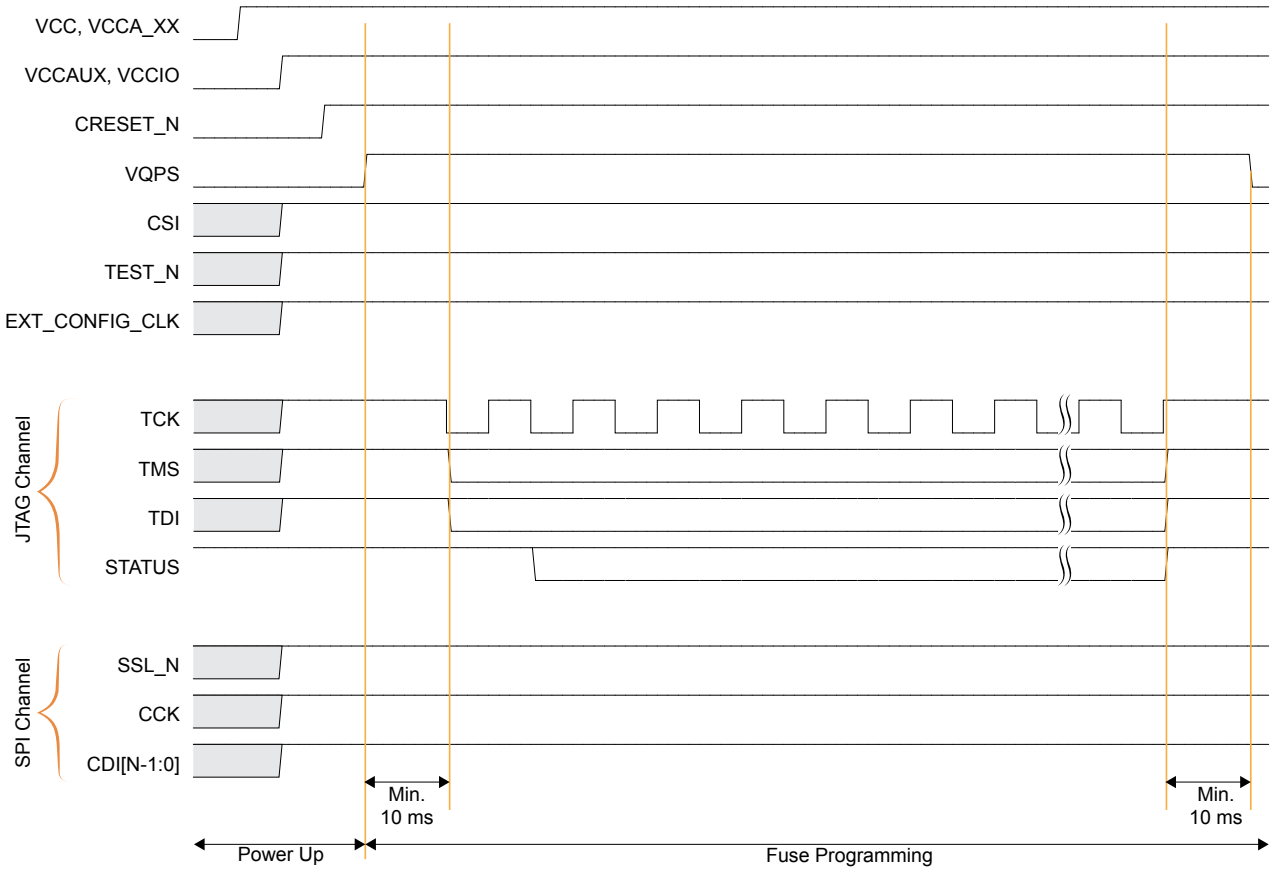
Fuse Programming Requirements

Important: The VQPS supply current requires a minimum of 100 mA.

To program the security fuses in FPGA, follow these requirements:

- During fuse programming, avoid device configuration and other JTAG operations that are not related to fuse programming.
- Ramp up the VQPS pin only after all other power supplies have ramped to their nominal voltages. The VQPS ramp rate follows the requirements shown in **Table 60: Power Supply Ramp Rates** on page 72.
- After powering up the VQPS pin, wait for a minimum of 10 ms before issuing JTAG instructions for fuse programming.
- After completing fuse programming through JTAG, wait for a minimum of 10 ms before powering down the VQPS pin.
- If required, other power supplies can be powered down only after the VQPS pin has been powered down below 25% of its nominal voltage level.

Figure 45: Fuse Programming Waveform



This waveform assumes you are using an SVF file generated with the Efinity Bitstream Security Key Generator.

Important: The SPI bus must be inactive during fuse programming.
The EXT_CONFIG_CLK pin must be inactive during fuse programming.

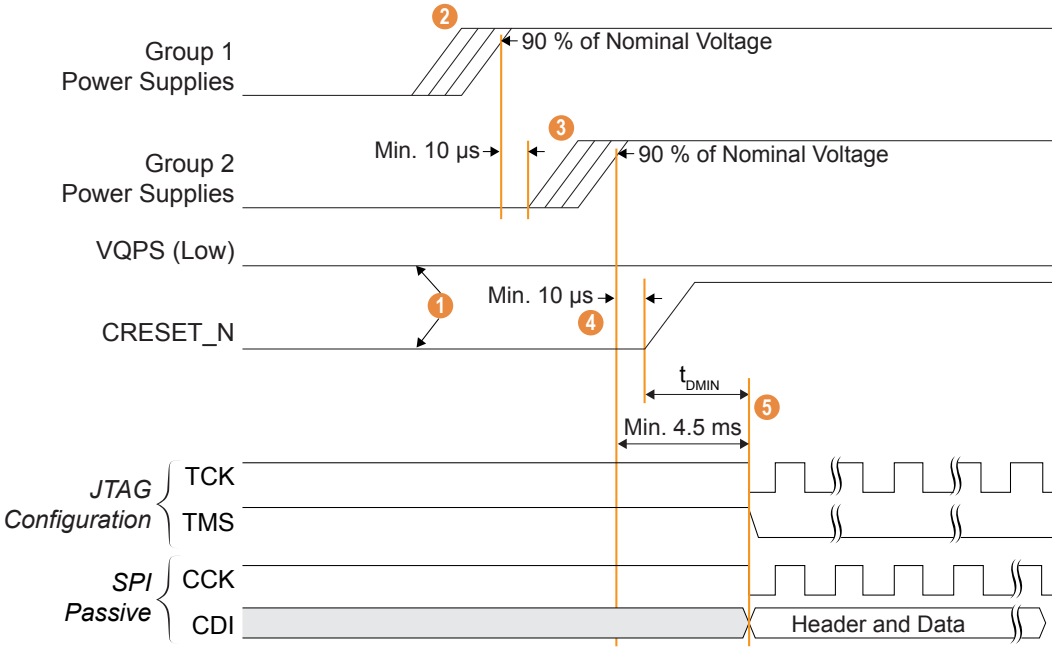
Learn more: Refer to the "Securing Bitstreams" section in the Efinity Programmer User Guide.
Refer to AN 057: Controlling VQPS with the Efinity SVF Player for more details about fuse programming.

Power Sequence

Important: You **must** follow the power-up and power-down sequence when powering TJ-Series FPGAs.

Power-Up Sequence

Figure 46: Power-Up Sequence



Important: You can only use one configuration channel at a time. Using SPI passive and JTAG at the same time can result in configuration failure.

1. The `CRESET_N` input must stay **low** until all power supplies are powered up. Additionally, `VQPS` must **always** stay **low** unless you are blowing the Ti180 security fuses.

   Note: Refer to **Fuse Programming Requirements** on page 65 if you need to blow the security fuses for the Ti180 FPGA on your board.

2. Power up supplies in group 1 first. You can power up these supplies in any sequence.

   Important: Ensure the power ramp rate is within the values shown in **Table 60: Power Supply Ramp Rates** on page 72.

3. Power up the group 2 supplies in any sequence at a minimum delay of 10 µs after group 1 supplies have reached 90% of their nominal voltage levels.
4. Release the `CRESET_N` input to high at a minimum delay of 10 µs after all FPGA supplies have reached 90% of their nominal voltage levels.
5. FPGA configuration can begin after there has been:
   - A 4.5 ms minimum delay after all supplies have reached at least 90% of their nominal voltage.
   - A t_{DMIN} minimum delay after `CRESET_N` goes high (see **SPI Passive Mode** on page 88 and **JTAG Mode** on page 86 for the delay specification).

   Note: With the configuration bitstream stored in the SPI flash device and the SPI active hardware connection properly established, the SPI active configuration automatically starts after the `CRESET_N` signal transitions from low to high.

Table 53: Power-Up Groups

If you are blowing the security fuses, refer to **Fuse Programming Requirements** on page 65.

Power-Up Sequence	
Group 1	**Group 2**
VCC VCCA	VCCAUX VCCIO VCCIO33
MIPI D-PHY	
–	VCC18A_MIPI_TX VCC18A_MIPI_RX
DDR DRAM controller	
VDD_PHY VDDPLL_MCB_TOP_PHY	VDDQ_PHY VDDQX_PHY VDDQ_CK_PHY



Note: Some DDR DRAM devices have a specific power-up sequence requirement. Ensure this requirement is met when the FPGA and memory share a power supply.

Power-Down Sequence

There is no specific power-down sequence for Ti180 FPGAs. However, the VQPS power supply **must** follow the specifications in **Fuse Programming Requirements** on page 65.

Power Supply Current Transient

You may observe an inrush current on the dedicated power rail during power-up. You must ensure that the power supplies selected in your board meets the current requirement during power-up and the estimated current during user mode. Use the Power Estimator to calculate the estimated current during user mode.

Table 54: Minimum Power Supply Current Transient

Power Supply	Minimum Power Supply Current Transient	Unit
VCC	1,500	mA

Unused Resources and Features

Table 55: Connection Requirements for Unused Resources and Features

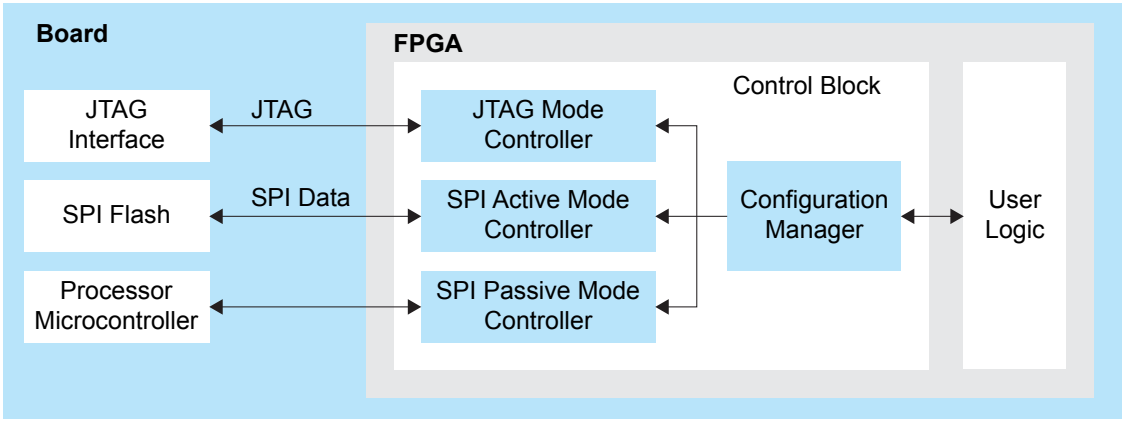
Unused Resource/Feature	Pin	Note
PLL	VCCA	Connect to VCC.
HSIO Bank	VCCIO	Connect to either 1.2 V, 1.35 V, 1.5 V, or 1.8 V.
HVIO Bank	VCCIO33	Connect to either 1.8 V, 2.5 V, 3.0 V, or 3.3 V.
MIPI	VCC18A_MIPI_TX VCC18A_MIPI_RX	Connect to VCC.
DDR	VDD_PHY	Leave unconnected.
	VDDPLL_MCB_TOP_PHY	Leave unconnected.
	VDDQ_PHY	Leave unconnected.
	VDDQX_PHY	Leave unconnected.
	VDDQ_CK_PHY	Leave unconnected.
Security (Fuse Blowing)	VQPS	Connect to GND.

Learn more: For more information, refer to the **Elitestek website**.

Configuration

The Ti180 FPGA contains volatile Configuration RAM (CRAM). The user must configure the CRAM for the desired logic function upon power-up and before the FPGA enters normal operation. The FPGA's control block manages the configuration process and uses a bitstream to program the CRAM. The Efinity® software generates the bitstream, which is design dependent. You can configure the Ti180 FPGA(s) in SPI active, SPI passive, or JTAG mode.

Figure 47: High-Level Configuration Options



In active mode, the FPGA controls the configuration process. The configuration clock can either be provided by an oscillator circuit within the FPGA or an external clock connected to the `EXT_CONFIG_CLK` pin. The bitstream is typically stored in an external serial flash device, which provides the bitstream when the FPGA requests it.

The control block sends out the instruction and address to read the configuration data. First, it issues a release from power-down instruction to wake up the external SPI flash. Then, it waits for at least 30 µs before issuing a fast read command to read the content of SPI flash from address 24h’000000 for 3-byte addressing mode or 32'h00000000 for 4-byte addressing mode.

In passive mode, the FPGA is the slave and relies on an external master to provide the control, bitstream, and clock for configuration. Typically the master is a microcontroller or another FPGA in active mode. The controller must wait for at least 32 µs after `CRESET` is de-asserted before it can send the bitstream.

In JTAG mode, you configure the FPGA via the JTAG interface.

Supported Configuration Modes

Table 56: Ti180 Configuration Modes by Package

Configuration Mode	Width	All Packages
Active	×1	✓
	×2	✓
	×4	✓
	×8	✓
Passive	×1	✓
	×2	✓
	×4	✓
	×8	✓
	×16	✓(7)
	×32	✓(7)
JTAG	×1	✓

Learn more: Refer to **AN 033: Configuring TJ-Series FPGAs** for more information.

(7) Not supported when security mode is enabled.

Characteristics and Timing

The following table shows the specification status for Ti180 packages.

Table 57: Package Status

Package	Status
All other packages	Final

DC and Switching Characteristics

Table 58: Absolute Maximum Ratings[8]

Conditions beyond those listed may cause permanent damage to the device. Device operation at the absolute maximum ratings for extended periods of time has adverse effects on the device.

Symbol	Description	Min	Max	Units
VCC	Core power supply.	-0.5	1.05	V
VCCA	PLL analog power supply.	-0.5	1.05	V
VCCAUX	1.8 V auxiliary power supply.	-0.5	1.98	V
VQPS	1.8 V security fuse supply.	-0.5	1.98	V
VCCIO	HSIO bank power supply.	-0.5	1.98	V
VCCIO33	HVIO bank power supply.	-0.5	3.63	V
VCC18A_MIPI_TX	1.8 V TX analog power supply for MIPI TX.	-0.5	1.98	V
VCC18A_MIPI_RX	1.8 V TX analog power supply for MIPI RX.	-0.5	1.98	V
VDD_PHY	LPDDR4/4x digital power supply.	-0.5	1.05	V
VDDPLL_MCB_TOP_PHY	LPDDR4/4x PLL power supply.	-0.5	1.05	V
VDDQ_PHY	LPDDR4/4x I/O power supply.	-0.5	1.21	V
VDDQX_PHY	LPDDR4/4x I/O pre-driver power supply.	-0.5	1.21	V
VDDQ_CK_PHY	LPDDR4/4x I/O power supply for clock.	-0.5	1.21	V
I_{IN}	Maximum current allowed through any I/O pin when the device is not turned on or during power-up/down with forward biasing of the clamp diode.[9]	–	10	mA
V_{IN}	HVIO input voltage.	-0.5	3.63	V
	HSIO input voltage.	-0.5	1.98	V
T_J	Operating junction temperature.	-40	125	°C
T_{STG}	Storage temperature, ambient.	-55	150	°C

[8] Supply voltage specification applied to the voltage taken at the device pins with respect to ground, not at the power supply.
[9] Should not exceed a total of 100 mA per bank

Table 59: Recommended Operating Conditions [8]

Symbol	Description	Min	Typ	Max	Units
VCC	C3L, C4L, I3L, I4L speed grade core power supply.	0.82	0.85	0.88	V
	C3, C4, I3, I4, Q3 speed grade core power supply.	0.92	0.95	0.98	V
VCCA	C3L, C4L, I3L, I4L speed grade PLL analog power supply.	0.82	0.85	0.88	V
	C3, C4, I3, I4, Q3 speed grade PLL analog power supply.	0.92	0.95	0.98	V
VCCAUX	1.8 V auxiliary power supply.	1.75	1.8	1.85	V
VQPS	1.8 V security fuse supply.	1.71	1.8	1.89	V
VCCIO	1.2 V HSIO bank power supply.	1.14	1.2	1.26	V
	1.35 V HSIO bank power supply	1.283	1.35	1.417	V
	1.5 V HSIO bank power supply.	1.425	1.5	1.575	V
	1.8 V HSIO bank power supply.	1.71	1.8	1.89	V
VCCIO33	1.8 V HVIO bank power supply.	1.71	1.8	1.89	V
	2.5 V HVIO bank power supply.	2.375	2.5	2.625	V
	3.0 V HVIO bank power supply.	2.85	3.0	3.15	V
	3.3 V HVIO bank power supply.	3.135	3.3	3.465	V
VCC18A_MIPI_TX	1.8 V analog power supply for MIPI TX.	1.71	1.8	1.89	V
VCC18A_MIPI_RX	1.8 V analog power supply for MIPI RX.	1.71	1.8	1.89	V
VDD_PHY	LPDDR4/4x digital power supply.	0.82	0.85	0.88	V
VDDPLL_MCB_TOP_PHY	LPDDR4/4x PLL power supply.	0.82	0.85	0.88	V
VDDQ_PHY	LPDDR4 I/O power supply.	1.06	1.1	1.17	V
	LPDDR4x I/O power supply.	0.57	0.6	0.65	V
VDDQX_PHY	LPDDR4 I/O pre-driver power supply.	1.06	1.1	1.17	V
	LPDDR4x I/O pre-driver power supply.	1.06	1.1	1.17	V
VDDQ_CK_PHY	LPDDR4 I/O power supply for clock.	1.06	1.1	1.17	V
	LPDDR4x I/O power supply for clock.	0.57	0.6	0.65	V
T_{JCOM}	Operating junction temperature, commercial.	0	–	85	°C
T_{JIND}	Operating junction temperature, industrial.	-40	–	100	°C
T_{JAUTO}	Operating junction temperature, automotive.	-40	–	125	°C

Table 60: Power Supply Ramp Rates

Symbol	Description	Min	Max	Units
t_{RAMP}	Power supply ramp rate for all supplies.	0.1 * V_{supply}	10	V/ms

Table 61: HVIO DC Electrical Characteristics

I/O Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)
	Min	Max	Min	Max	Max	Min
3.3 V LVCMOS	-0.3	0.8	2.1	3.465	0.2	VCCIO33 - 0.2
3.0 V LVCMOS	-0.3	0.8	2.1	3.15	0.2	VCCIO33 - 0.2
3.3 V LVTTL	-0.3	0.8	2.1	3.465	0.4	2.4
3.0 V LVTTL	-0.3	0.8	2.1	3.15	0.4	2.4
2.5 V LVCMOS	-0.3	0.45	1.7	2.625	0.4	2.0
1.8 V LVCMOS	-0.3	0.58	1.27	1.89	0.45	VCCIO33 - 0.45
1.8 V LVCMOS (JTAG)[10]	-0.3	0.28	1.27	1.89	0.45	VCCIO33 - 0.45

Table 62: HVIO DC Electrical Characteristics

Voltage (V)	Typical Hysteresis (mV)[11]	Input Leakage Current (µA)	Tristate Output Leakage Current (µA)
3.3	250	±25	±10
2.5	250	±25	±10
1.8	200	±25	±10

Table 63: HSIO Pins Configured as Single-Ended I/O DC Electrical Characteristics

I/O Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)
	Min	Max	Min	Max	Max	Min
1.8 V LVCMOS	-0.3	0.58	1.27	1.89	0.45	VCCIO - 0.45
1.5 V LVCMOS	-0.3	0.35 * VCCIO	0.65 * VCCIO	1.575	0.25 * VCCIO	0.75 * VCCIO
1.2 V LVCMOS	-0.3	0.35 * VCCIO	0.65 * VCCIO	1.26	0.25 * VCCIO	0.75 * VCCIO
1.8 V HSTL	–	VREF - 0.1	VREF + 0.1	–	0.4	VCCIO - 0.4
1.5 V HSTL	–	VREF - 0.1	VREF + 0.1	–	0.4	VCCIO - 0.4
1.2 V HSTL	-0.15	VREF - 0.08	VREF + 0.08	VREF + 0.15	0.25 * VCCIO	0.75 * VCCIO
1.8 V SSTL	-0.3	VREF - 0.125	VREF + 0.125	VCCIO + 0.3	VTT - 0.603	VTT + 0.603
1.5 V SSTL	–	VREF - 0.1	VREF + 0.1	–	0.2 * VCCIO	0.8 * VCCIO
1.35 V SSTL	–	VREF - 0.1	VREF + 0.1	–	0.2 * VCCIO	0.8 * VCCIO
1.2 V SSTL	–	VREF - 0.1	VREF + 0.1	–	0.2 * VCCIO	0.8 * VCCIO

Table 64: HSIO Pins Configured as Single-Ended I/O DC Electrical Characteristics

I/O Standard	VREF (V)			Vtt (V)		
	Min	Typ	Max	Min	Typ	Max
1.8 V HSTL	0.85	0.9	0.95	–	0.5 * VCCIO	–
1.5 V HSTL	0.68	0.75	0.9	–	0.5 * VCCIO	–
1.2 V HSTL	0.47 * VCCIO	0.5 * VCCIO	0.53 * VCCIO	–	0.5 * VCCIO	–
1.8 V SSTL	0.833	0.9	0.969	VREF - 0.04	VREF	VREF + 0.04
1.5 V SSTL	0.49 * VCCIO	0.5 * VCCIO	0.51 * VCCIO	0.49 * VCCIO	0.5 * VCCIO	0.51 * VCCIO
1.35 V SSTL	0.49 * VCCIO	0.5 * VCCIO	0.51 * VCCIO	0.49 * VCCIO	0.5 * VCCIO	0.51 * VCCIO
1.2 V SSTL	0.49 * VCCIO	0.5 * VCCIO	0.51 * VCCIO	0.49 * VCCIO	0.5 * VCCIO	0.51 * VCCIO

(10) For JTAG configuration mode
(11) For input pins with Schmitt Trigger enabled

Table 65: HSIO Pins Configured as Differential SSTL I/O Electrical Characteristics

I/O Standard	$V_{SWING\ (DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING\ (AC)}$ (V)	
	Min	Max	Min	Typ	Max	Min	Max
1.8 V SSTL	0.25	VCCIO + 0.6	VCCIO/2 – 0.175	–	VCCIO/2 + 0.175	0.5	VCCIO + 0.6
1.5 V SSTL	0.2	–	VCCIO/2 – 0.15	–	VCCIO/2 + 0.15	0.35	–
1.35 V SSTL	0.2	–	VCCIO/2 – 0.15	–	VCCIO/2 + 0.15	0.35	–
1.2 V SSTL	0.18	–	VREF– 0.15	VCCIO /2	VREF + 0.15	-0.3	0.3

Table 66: HSIO Pins Configured as Differential HSTL I/O Electrical Characteristics

I/O Standard	$V_{DIF\ (DC)}$ (V)		$V_{X\ (AC)}$ (V)			$V_{CM\ (DC)}$ (V)			$V_{DIF\ (AC)}$ (V)	
	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
1.8 V HSTL	0.2	–	0.78	–	1.12	0.78	–	1.12	0.4	–
1.5 V HSTL	0.2	–	0.68	–	0.9	0.68	–	0.9	0.4	–
1.2 V HSTL	0.16	VCCIO + 0.3	–	0.5 * VCCIO	–	0.4 * VCCIO	0.5 * VCCIO	0.6 * VCCIO	0.3	VCCIO + 0.48

Table 67: HSIO Pins Configured as Single-Ended I/O DC Electrical Characteristics

Voltage (V)	Typical Hysteresis (mV)[12]	Input Leakage Current (µA)	Tristate Output Leakage Current (µA)
1.8	200	±25	±10
1.5	160	±25	±10
1.35	–	±25	±10
1.2	140	±25	±10

Table 68: Supported HVIO Drive Strength

I/O Standard	Drive Strength	Units
3.3 V LVTTL	4, 8, 12, 16	mA
3.3 V LVCMOS	2, 4, 6, 8	mA
3.0 V LVTTL	4, 8, 12, 16	mA
3.0 V LVCMOS	2, 4, 6, 8	mA
2.5 V LVCMOS	4, 8, 12, 16	mA
1.8 V LVCMOS	4, 8, 12, 16	mA

[12] For LVCMOS input pins with Schmitt Trigger enabled

Table 69: Supported HSIO Drive Strength

I/O Standard	Drive Strength	Units
1.8 V LVCMOS	4, 8, 12, 16	mA
1.5 V LVCMOS	4, 8, 12, 16	mA
1.2 V LVCMOS	2, 4, 8, 12	mA
1.8 V SSTL	4, 8, 10, 12	mA
1.5 V SSTL	4, 8, 10, 12	mA
1.35 V SSTL	4, 8, 10, 12	mA
1.2 V SSTL	4, 8, 10, 12	mA
1.8 V HSTL	4, 8, 10, 12	mA
1.5 V HSTL	4, 8, 10, 12	mA
1.2 V HSTL	4, 8, 10, 12	mA

Table 70: Maximum Toggle Rate

I/O	I/O Standard	Speed Grade	Serialization Mode	Max Toggle Rate (Mbps)[13][14]
HVIO	3.0 V, 3.3 V LVTTL 3.0 V, 3.3 V LVCMOS	All	–	200
HVIO	2.5 V LVCMOS	All	–	100
HVIO	1.8 V LVCMOS	All	–	400
HSIO	1.8 V, 1.5 V, 1.2 V LVCMOS	All	–	400
HSIO	1.8 V, 1.5 V, 1.35 V, 1.2 V SSTL 1.8 V, 1.5 V, 1.2 V HSTL	All	–	800
HSIO	LVDS	C4, I3, I4, Q3	Full-rate	1,000
			Half-rate	1,500
		C3	Full-rate	1,000
			Half-rate	1,300
		C4L, I3L, I4L	Full-rate	800
			Half-rate	1,250
		C3L	Full-rate	800
			Half-rate	1,100
HSIO	Sub-LVDS	C3, C4, I3, I4, Q3	Full-rate	1,000
			Half-rate	1,250
		C3L, C4L, I3L, I4L	Full-rate	800
			Half-rate	1,250
HSIO	MIPI lane	C4, I3, I4, Q3	–	1,500
		C3	–	1,300
		I3L, C4L, I4L	–	1,250
		C3L	–	1,100

Table 71: HVIO Internal Weak Pull-Up and Pull-Down Resistance

I/O Standard	Internal Pull-Up			Internal Pull-Down			Units
	Min	Typ	Max	Min	Typ	Max	
3.3 V LVTTL/LVCMOS	25	42	67	24	29	33	kΩ
3.0 V LVTTL/LVCMOS	25	42	67	24	29	33	kΩ
2.5 V LVCMOS	25	42	67	24	29	33	kΩ
1.8 V LVCMOS	25	35	45	24	29	33	kΩ

[13] The maximum toggle rate is dependent on the drive strength and external load conditions. Perform IBIS simulation to determine the optimal drive strength setting to achieve the targeted toggle rate.

[14] All I/O standards are characterized with 5 pF load, except for LVTTL and LVCMOS standards which are characterized with 15 pF load.

Table 72: HSIO Internal Weak Pull-Up and Pull-Down Resistance

CDONE and CRESET_N also have an internal weak pull-up with these values.

I/O Standard	Speed Grade	Internal Pull-Up			Internal Pull-Down			Units
		Min	Typ	Max	Min	Typ	Max	
1.8 V LVCMOS, HSTL, SSTL	C3, C4, I3, C3L, C4L, I3L	18	27	47	18	27	47	kΩ
	Q3	15	27	47	15	27	47	kΩ
1.5 V LVCMOS, HSTL, SSTL	C3, C4, I3, C3L, C4L, I3L	22	38	65	22	38	65	kΩ
	Q3	20	38	65	20	38	65	kΩ
1.35 V SSTL	C3, C4, I3, C3L, C4L, I3L	30	52	100	30	52	100	kΩ
	Q3	22	52	100	22	52	100	kΩ
1.2 V LVCMOS, HSTL, SSTL	C3, C4, I3, C3L, C4L, I3L	40	66	135	40	66	135	kΩ
	Q3	25	66	135	25	66	135	kΩ

Table 73: Single-Ended I/O Programmable Delay Chain Step Size: Static

Speed Grade	Delay per Step			Units
	Min	Typ	Max	
C3, C4, I3, I4, Q3	35	55	75	ps
C3L, C4L, I3L, I4L	50	68	89	ps

Table 74: Single-Ended I/O Programmable Delay Chain Step Size: Dynamic

Speed Grade	Delay per Step			Units
	Min	Typ	Max	
C3, C4, I3, I4	12	18	24	ps
Q3	12	18	26	ps
C3L, C4L, I3L, I4L	15	22	28	ps

Table 75: Differential I/O Programmable Delay Chain Step Size: Static and Dynamic

Speed Grade	Delay per Step			Units
	Min	Typ	Max	
C3, C4, I3, I4	12	18	24	ps
Q3	12	18	26	ps
C3L, C4L, I3L, I4L	15	22	28	ps

Table 76: Block RAM, DSP Block, Gobal Clock Buffer, and DPA Performance

Description	Speed Grade			Units
	C3, C4, I3, I4	Q3	C3L, C4L, I3L, I4L	
Block RAM maximum frequency.	1,000	900	800	MHz
DSP block maximum frequency.	1,000	900	800	MHz
Global clock buffer block maximum frequency.	1,000	1,000	800	MHz
DPA maximum data rate.	1,000	1,000	800	Mbps

Table 77: MIPI D-PHY Interface Performance

Description	Packages	FPGA Speed Grade				Units
		C4, I3	C3, I4	C3L, C4L, I3L, I4L	Q3	
MIPI D-PHY block maximum data rate.	J361, L484	2.5	2.5	2.0	–	Gbps
	J484	2.5	2.5	2.0	2.0	Gbps

Table 78: LPDDR4/4x Interface Performance

Description	Packages	FPGA Speed Grade					Units
		C4	I4, C4L, I4L	I3	C3, C3L, I3L	Q3	
LPDDR4/4x DRAM interface maximum data rate.	J361	3.0	3.0	2.5	2.5	–	Gbps
	J484	3.0	3.0	2.5	2.5	2.5	Gbps
	G529	3.3	3.3	2.8	2.8	–	Gbps

Table 79: V_{IH}, V_{IL}, V_{OL}, and V_{OH} Specifications for LPDDR4/4x

Description	V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)
	Min	Max	Min	Max	Max	Min
LPDDR4	–	(V_{DDQ_PHY} / 6) - 0.075	(V_{DDQ_PHY} / 6) + 0.075	–	V_{DDQ_PHY} * 0.1	V_{DDQ_PHY} * 0.5
LPDDR4x	–	(V_{DDQ_PHY} / 4) - 0.075	(V_{DDQ_PHY} / 4) + 0.075	–	V_{DDQ_PHY} * 0.1	V_{DDQ_PHY} * 0.5

HSIO Electrical and Timing Specifications

The HSIO pins comply with the LVDS EIA/TIA-644 electrical specifications.

HSIO as LVDS, Sub-LVDS, Bus-LVDS, RSDS, Mini LVDS, and SLVS

Table 80: HSIO Electrical Specifications when Configured as LVDS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
LVDS TX						
V_{CCIO}	LVDS transmitter voltage supply	–	1.71	1.8	1.89	V
V_{OD}	Output differential voltage	RL = 100 Ω	200	350	450	mV
Δ V_{OD}	Change in V_{OD}	–	–	–	50	mV
V_{OCM}	Output common mode voltage	–	1.125	1.2	1.375	V
Δ V_{OCM}	Change in V_{OCM}	–	–	–	50	mV
LVDS RX						
V_{ID}	Input differential voltage	–	100	–	600	mV
V_{ICM}	Input common mode voltage (fmax <= 1000 Mbps)	–	100	–	1,600	mV
	Input common mode voltage (fmax > 1000 Mbps)	–	700	–	1,400	mV
V_i	Input voltage valid range	–	0	–	1.89	V

Table 81: HSIO Timing Specifications when Configured as LVDS

Parameter	Description	Min	Typ	Max	Unit
t_{LVDS_CPA}	LVDS TX reference clock output phase accuracy	-5	–	+5	%
t_{LVDS_skew}	LVDS TX lane-to-lane skew	–	200	–	ps

Table 82: HSIO Electrical Specifications when Configured as Sub-LVDS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
Sub-LVDS TX						
VCCIO	Sub-LVDS transmitter voltage supply	–	1.71	1.8	1.89	V
V_{OD}	Output differential voltage	RL = 100 Ω	100	150	200	mV
ΔV_{OD}	Change in V_{OD}	–	–	–	50	mV
V_{OCM}	Output common mode voltage	–	0.8	0.9	1.0	V
ΔV_{OCM}	Change in V_{OCM}	–	–	–	50	mV
Sub-LVDS RX						
V_{ID}	Input differential voltage	–	100	–	600	mV
V_{ICM}	Input common mode voltage	–	100	–	1600	mV
V_i	Input voltage valid range	–	0	–	1.89	V

Table 83: HSIO Electrical Specifications when Configured as Bus-LVDS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
Bus-LVDS TX						
VCCIO	Voltage supply for LVDS transmitter	–	1.71	1.8	1.89	V
V_{OD}	Differential output voltage	RL = 27 Ω	200	250	300	mV
ΔV_{OD}	Static difference of VOD (between 0 and 1)	–	–	–	50	mV
V_{OC}	Output common mode voltage	–	1.125	1.2	1.375	V
ΔV_{OC}	Output common mode voltage offset	–	–	–	50	mV
Bus-LVDS RX						
V_{ID}	Differential input voltage	–	100	–	600	mV
V_{IC}	Differential input common mode	–	100	–	1600	mV
V_i	Valid input voltage range	–	0	–	1.89	V

Table 84: HSIO Electrical Specifications when Configured as RSDS, Mini LVDS and SLVS

IO standard	V_{ID} (mV)		V_{ICM} (mV)		V_{OD} (mV)			V_{OCM} (mV)		
	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
RSDS	100	-	300	1400	100	200	600	500	1200	1400
Mini LVDS	200	600	400	1325	250	-	600	1000	1200	1400
SLVS	100	400	100	300	150	200	250	140	200	270

HSIO as High–Speed and Low-Power MIPI Lane

The MIPI transmitter and receiver lanes are compliant to the MIPI Alliance Specification for D-PHY Revision 1.1.

Table 85: HSIO DC Specifications when Configured as High–Speed MIPI TX Lane

Parameter	Description	Min	Typ	Max	Unit
VCCIO	High–speed transmitter voltage supply.	1.14	1.2	1.26	V
V_{CMTX}	High–speed transmit static common–mode voltage.	150	200	250	mV
$\|\Delta V_{CMTX}\|$	V_{CMTX} mismatch when output is Differential–1 or Differential–0.	–	–	5	mV
$\|V_{OD}\|$	High–speed transmit differential voltage.	140	200	270	mV
$\|\Delta V_{OD}\|$	V_{OD} mismatch when output is Differential–1 or Differential–0.	–	–	14	mV
V_{OHHS}	High–speed output high voltage.	–	–	360	mV
V_{CMRX}	Common mode voltage for high-speed receive mode.	70	–	330	mV

Table 86: HSIO DC Specifications when Configured as Low–Power MIPI TX Lane

Parameter	Description	Min	Typ	Max	Unit
V_{OH}	Thevenin output high level.	1.1	1.2	1.3	V
V_{OL}	Thevenin output low level.	-50	–	50	mV
Z_{OLP}	Output impedance of low-power transmitter.	110	–	–	Ω

Table 87: HSIO DC Specifications when Configured as High–Speed MIPI RX Lane

Parameter	Description	Min	Typ	Max	Unit
$V_{CMRX(DC)}$	Common mode voltage high–speed receiver mode .	70	–	330	mV
V_{IDTH}	Differential input high threshold.	–	–	70	mV
V_{IDTL}	Differential input low threshold.	-70	–	–	mV
V_{IHHS}	Single-ended input high voltage.		–	460	mV
V_{ILHS}	Single-ended input low voltage.	-40	–	–	mV

Table 88: HSIO DC Specifications when Configured as Low–Power MIPI RX Lane

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	Logic 1 input voltage.	880	–	–	mV
V_{IL}	Logic 0 input voltage, not in ULP state.	–	–	550	mV
$V_{IL-ULPS}$	Logic 0 input voltage, ULPS state.	–	–	300	mV
V_{HYST}	Input hysteresis.	25	–	–	mV

MIPI Electrical Specifications and Timing

The MIPI D-PHY transmitter and receiver are compliant to the MIPI Alliance Specification for D-PHY Revision 1.1.

Table 89: High–Speed MIPI D–PHY Transmitter (TX) DC Specifications

Parameter	Description	Min	Typ	Max	Unit
V_{CMTX}	High–speed transmit static common–mode voltage.	150	200	250	mV
$\|\Delta V_{CMTX(1,0)}\|$	V_{CMTX} mismatch when output is Differential–1 or Differential–0.	–	–	5	mV
$\|V_{OD}\|$	High–speed transmit differential voltage.	140	200	270	mV
$\|\Delta V_{OD}\|$	VOD mismatch when output is Differential–1 or Differential–0.	–	–	14	mV
V_{OHHS}	High–speed output high voltage.	–	–	360	mV
Z_{OS}	Single ended output impedance.	40	50	60	Ω
ΔZ_{OS}	Single ended output impedance mismatch.	–	–	20	%

Table 90: High–Speed MIPI D–PHY Transmitter (TX) AC Specifications

Parameter	Description	Min	Typ	Max	Unit
$\Delta V_{CMTX(HF)}$	Common-level variations above 450 MHz.	–	–	15	mV_{RMS}
$\Delta V_{CMTX(LF)}$	Common-level variations between 50 to 450 MHz.	–	–	25	mV_{PEAK}
t_R and t_F	Rise and fall time < 1.0 Gbps.	–	–	0.3	UI
	Rise and fall time > 1.0 Gbps.	–	–	0.35	UI
	Rise and fall time > 1.5 Gbps.	–	–	0.4	UI

Table 91: Low–Power MIPI D–PHY Transmitter (TX) DC Specifications

Parameter	Description	Min	Typ	Max	Unit
V_{OH}	Thevenin output high level.	0.95	1.2	1.3	V
V_{OL}	Thevenin output low level.	–50	–	50	mV
Z_{OLP}	Output impedance of low–power transmitter.	110	–	–	Ω

Table 92: Low-Power MIPI D–PHY Transmitter (TX) AC Specifications

Parameter	Description	Min	Typ	Max	Unit
T_{RLP}/T_{FLP}	15%-85% rise time and fall time.	–	–	25	ns
T_{REOT}	30%-85% rise time and fall time.	–	–	35	ns
$T_{LP\text{-}PULSE\text{-}TX}$	Pulse width of first LP exclusive-OR clock pulse after Stop state or last pulse before Stop state.	40	–	–	ns
	Pulse width of all other pulses.	–	20	–	ns
$T_{LP\text{-}PER\text{-}TX}$	Period of the LP exclusive-OR clock.	90	–	–	ns
$\delta V/\delta t_{SR}$	Slew rate at C_{LOAD} = 50 pF < 1.5 Gbps.	30	–	150	mV/ns
	Slew rate at C_{LOAD} = 50 pF > 1.5 Gbps.	25	–	150	mV/ns

Table 93: High–Speed MIPI D–PHY Receiver (RX) DC Specifications

Parameter	Description	Min	Typ	Max	Unit
$V_{CMRX(DC)}$	Common mode voltage high–speed receive mode.	70	–	330	mV
Z_{ID}	Differential input impedance.	80	100	120	Ω

Table 94: High–Speed MIPI D–PHY Receiver (RX) AC Specifications

Parameter	Description	Min	Typ	Max	Unit
$\Delta V_{CMRX(HF)}$	Common-point interference above 450 MHz.	–	–	50	mV
$\Delta_{VCMRX(LF)}$	Common-point interference between 50 MHz to 450 MHz.	–	–	25	mV
V_{IDTH}	Differential input high threshold.	–	–	40	mV
V_{IDTL}	Differential input low threshold.	–40	–	–	mV
V_{IHHS}	Single–ended input high voltage.	–	–	460	mV
V_{ILHS}	Single–ended input low voltage.	–40	–	–	mV
$V_{TERM–EN}$	Single–ended threshold for high–speed termination enable.	–	–	450	mV
CCP	Common-point termination.	–	–	60	pF

Table 95: Low–Power MIPI D–PHY Receiver (RX) DC Specifications

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	Logic 1 input voltage.	740	–	–	mV
V_{IL}	Logic 0 input voltage, not in ULP state.	–	–	550	mV
$V_{IL–ULPS}$	Logic 0 input voltage, ULP state.	–	–	300	mV
V_{HYST}	Input hysteresis.	25	–	–	mV

Table 96: Low-Power MIPI D–PHY Receiver (RX) AC Specifications

Parameter	Description	Min	Typ	Max	Unit
T_{MIN-RX}	Minimum pulse width response.	20	–	–	ns
V_{INT}	Peak interference amplitude.	–	–	200	mV
f_{INT}	Interference frequency.	450	–	–	MHz

MIPI Reset Timing

The MIPI RX and TX interfaces have two reset signals (`RESET` and `RST0_N`) to reset the D-PHY controller logic. These signals are active low, and you should use them together to reset the MIPI interface.

The following waveform illustrates the minimum time required to reset the MIPI interface.

Figure 48: RESET and RST0_N Timing Diagram

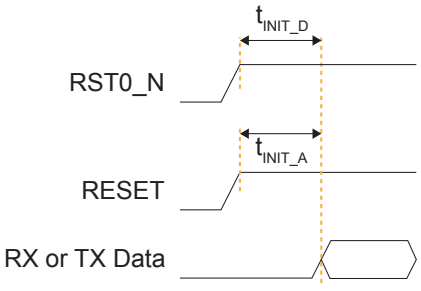


Table 97: MIPI Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{INIT_A}	Minimum time between the rising edge of RESET and the start of MIPI RX or TX data.	350	–	–	µs
t_{INIT_D}	Minimum time between the rising edge of RST0_N and the start of MIPI RX or TX data.	1	–	–	clk

PLL Timing and AC Characteristics

The following tables describe the PLL timing and AC characteristics.

Table 98: PLL Timing

Symbol	Parameter	Min	Typ	Max	Units
F_{IN}	Input clock frequency.	16	–	800	MHz
F_{OUT}	Output clock frequency.	0.1342	–	1,000	MHz
F_{VCO}	PLL VCO frequency.	2,200	–	5,500	MHz
F_{PLL}	Post-divider PLL VCO frequency.	–	–	4,000	MHz
F_{PFD}	Phase frequency detector input frequency.	16	–	800	MHz

Table 99: PLL AC Characteristics

Test conditions at nominal voltage and room temperature.

Symbol	Parameter	Min	Typ	Max	Units
t_{DT}	Output clock duty cycle.	45	50	55	%
t_{OPJIT}	Output clock period jitter (PK-PK). This specification applies when an input jitter of 20 ps is applied.	–	–	200	ps
t_{OPJITN}	Output clock period jitter (PK-PK) with noisy input. This specification applies for a maximum allowed input jitter of 800 ps. The period jitter is measured over 10,000 sample size with minimal core and I/O activity.	–	–	400	ps
t_{ILJIT}	Input clock long-term jitter (PK-PK).	–	–	800	ps
t_{PLL_HLW}	PLL input clock high/low pulse width.	0.56	–	–	ns
t_{LOCK}	PLL lock-in time.	–	300	500	PFD[15]

[15] The PFD cycle is equal to the reference clock divider divided by the reference clock frequency.

Configuration Timing

The Ti180 FPGA has the following configuration timing specifications.

Note: Refer to **AN 033: Configuring TJ-Series FPGAs** for detailed configuration information.

Timing Parameters Applicable to All Modes

Table 100: All Modes

Symbol	Parameter	Min	Typ	Max	Units
t_{CRESET_N}	Minimum CRESET_N low pulse width required to trigger re-configuration.	0.32	–	–	µs
t_{USER}	Minimum configuration duration after CDONE goes high before entering user mode. Test condition at 10 kΩ pull-up resistance and 10 pF output loading on CDONE pin.	25	–	–	µs

Note: The FPGA may go into user mode before t_{USER} has elapsed. However, Elitestek recommends that you keep the system interface to the FPGA in reset until t_{USER} has elapsed.

For JTAG programming, the min t_{USER} configuration time is required after `CDONE` goes high and the FPGA receives the ENTERUSER instruction from the JTAG host (TAP controller in UPDATE_IR state).

JTAG Mode

Figure 49: JTAG Timing Waveform

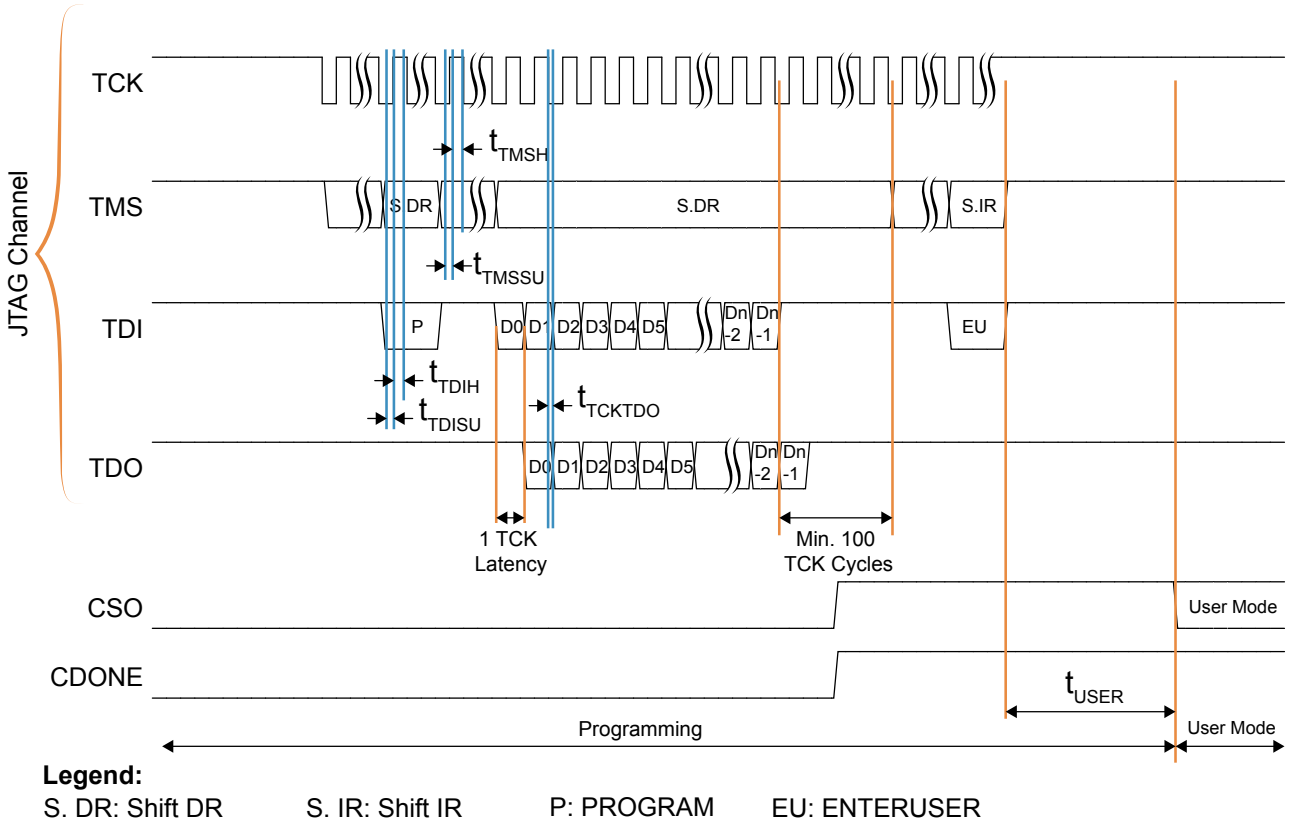


Table 101: JTAG Mode Timing

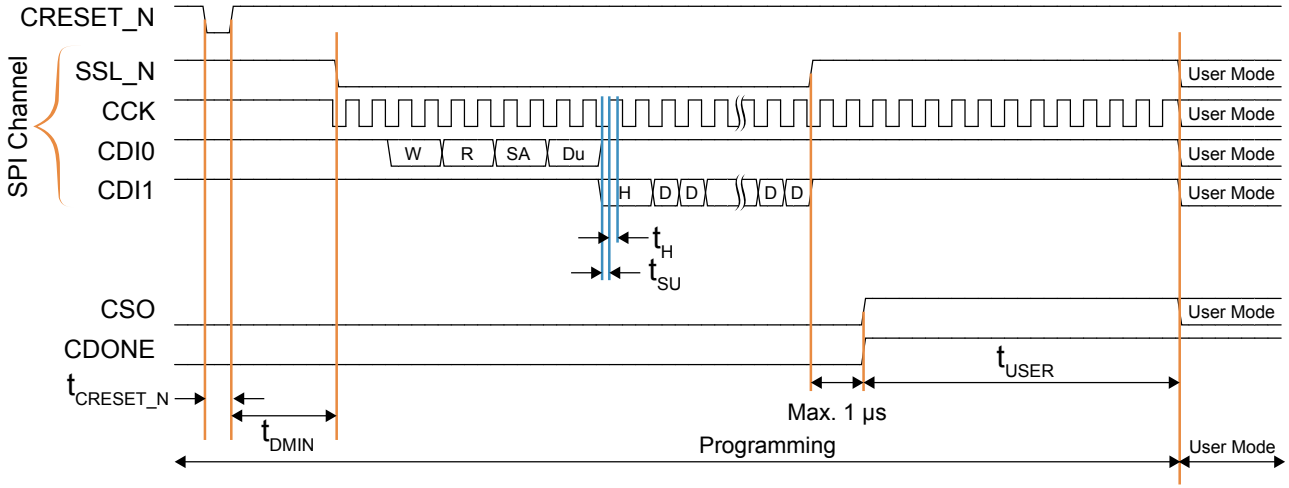
Symbol	Parameter	Min	Typ	Max	Units
f_{TCK}	TCK frequency.	–	–	10	MHz
	TCK frequency (1.8 V).	–	–	3	MHz
t_{TDISU}	TDI setup time.(16)	15	–	–	ns
t_{TDIH}	TDI hold time.(16)	2.5	–	–	ns
t_{TMSSU}	TMS setup time.(16)	15	–	–	ns
t_{TMSH}	TMS hold time.(16)	2.5	–	–	ns
t_{TCKTDO}	TCK falling edge to TDO output.(16)	–	–	30	ns
t_{DMIN}	Minimum time between deassertion of CRESET_N to the start of JTAG configuration.	32	–	–	µs

Important: The SPI bus must be inactive during JTAG configuration.
The `EXT_CONFIG_CLK` pin must be inactive during JTAG configuration.

(16) Applicable for all voltage ranges.

SPI Active Mode

Figure 50: SPI Active (x1) Timing Sequence



Legend:

W: Wake Up R: Read SA: Start Address
Du: Dummy H: Header D: Data

The waveform shows the perspective from the control block without any optional external pull-up or pull-down resistors connected.

Table 102: Active Mode Timing

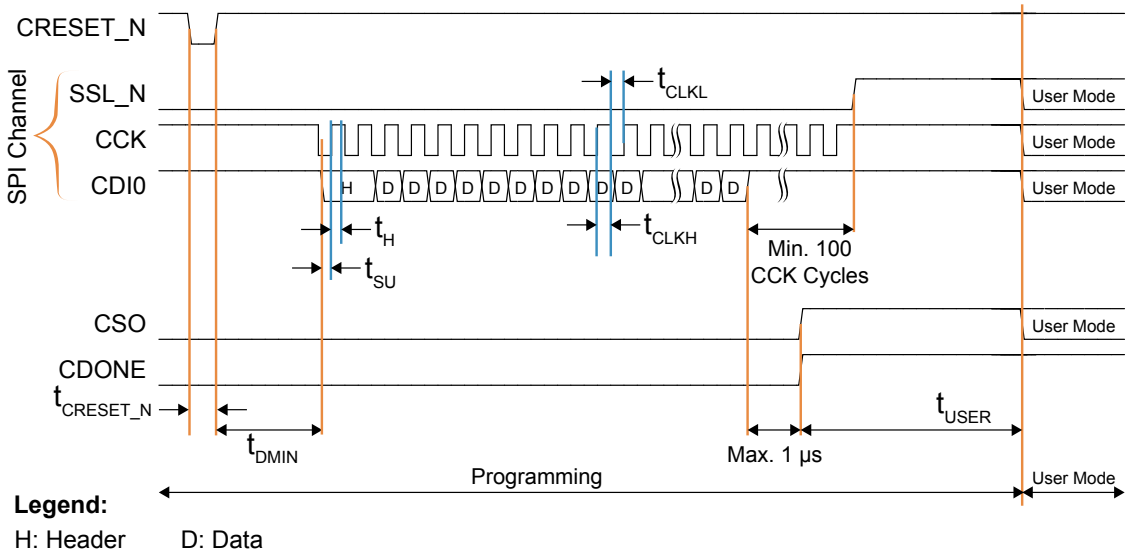
Symbol	Parameter	Frequency	Min	Typ	Max	Units
f_{MAX_M}	Active mode internal configuration clock frequency.	DIV1	52	80	100	MHz
		DIV2	26	40	52	MHz
		DIV4	13	20	26	MHz
		DIV8	6.5	10	13	MHz
$f_{MAX_M_EXTCLK}$	Active mode external configuration clock frequency.	–	–	–	100	MHz
t_{SU}	Setup time. Test condition at 1.8 V I/O standard and 0 pF output loading.	–	3	–	–	ns
t_H	Hold time. Test condition at 1.8 V I/O standard and 0 pF output loading.	–	0	–	–	ns
t_{DMIN}	Minimum time between deassertion of CRESET_N to first valid configuration data.	–	32	–	–	µs

Important: The JTAG pins must be inactive during SPI active configuration.

The `EXT_CONFIG_CLK` pin must be inactive during SPI active configuration if the internal oscillator is selected as the configuration clock source (default).

SPI Passive Mode

Figure 51: SPI Passive Mode (x1, Mode 3) Timing Sequence



Note:

- The waveform shows the perspective from the control block without any optional external pull-up or pull-down resistors connected.
- CDI input data is clocked by `CCK`. To prevent configuration failure, `CCK` must stop toggling if the bitstream data becomes invalid. You must resume with the next bitstream data before stopping to continue the configuration.
- `CSI` must stay high during configuration.
- `SSL_N` must stay low during configuration.
- Elitestek does not recommend connecting multiple slaves on the same SPI bus.

Important: To ensure successful configuration, the microprocessor must continue to supply the configuration clock to the TJ-Series FPGA for at least 100 cycles after sending the last configuration data.

Table 103: Passive Mode Timing

Symbol	Parameter	Min	Typ	Max	Units
f_{MAX_S}	Passive mode configuration clock frequency.	–	–	100	MHz
t_{CLKH}	Configuration clock pulse width high.	4.8	–	–	ns
t_{CLKL}	Configuration clock pulse width low.	4.8	–	–	ns
t_{SU}	Setup time.	2	–	–	ns
t_H	Hold time.	1	–	–	ns
t_{DMIN}	Minimum time between deassertion of CRESET_N to first valid configuration data.	32	–	–	µs

Important: The JTAG pins must be inactive during SPI passive configuration.
The `EXT_CONFIG_CLK` pin must be inactive during SPI passive configuration.

Pinout Description

The following tables describe the pinouts for power, ground, configuration, and interfaces.

Table 104: Power and Ground Pinouts

xx indicates the bank location.

Function	Description
VCC	Core power supply.
VCCA_*xx*	PLL analog power supply.
VCCAUX	1.8 V auxiliary power supply.
VCCIO33_*xx*	HVIO bank power supply.
VCCIO*xx*	HSIO bank power supply.
VCCIO*xx_yy_zz*	Power for HSIO banks that are shorted together. *xx*, *yy*, and *zz* are the bank locations. For example: VCCIO1B_1C shorts banks 1B and 1C
VQPS	1.8 V supply for security fuse. During configuration and normal operation, keep this pin at 0 V. When you want to blow the security fuses, power this pin up to 1.8 V.
GND	Ground.

Table 105: GPIO Pinouts

x indicates the location (T, B, L, or R); *xx* indicates the bank location; *n* indicates the number; *yyyy* indicates the function.

Function	Direction	Description
GPIO*x_n*	I/O	HVIO for user function. User I/O pins are single-ended.
GPIO*x_n_yyyy*	I/O	HVIO or multi-function pin.
GPIO*x*_N_*n* GPIO*x*_P_*n*	I/O	HSIO transmitter, receiver, or both.
GPIO*x*_N_*n_yyyy* GPIO*x*_P_*n_yyyy*	I/O	HSIO transmitter, receiver, both, or multi-function.
REF_RES_*xx*	–	REF_RES is a reference resistor to generate constant current for the related circuits. Connect the following REF_RES pins to ground through a 10 kΩ resistor with a tolerance of ±1% : • REF_RES_ 2A, REF_RES_2C, REF_RES_4A, and REF_RES_4C pins must be connected. • REF_RES pin of the particular bank, if pins in the bank are used as LVDS TX or MIPI TX lane. • REF_RES_3A pin, if the internal oscillator is used. • REF_RES_3A pin, if blowing of fuses for FPGA security is required. You can leave the REF_RES pins floating if none of the above are applicable.

Table 106: Alternate Function Pinouts

n is the number.

Function	Direction	Description
CLK*n*	Input	Single ended input for global clock and control network resource. The number of inputs is package dependent.
CLK*n*_P/N	Input	Differential input pair for global clock and control network resource. P pins can access to global clock and control network resource if it is in single-ended configuration.
EXTFB	Input	PLL external feedback CLKIN.
PLLIN*n*	Input	PLL reference clock resource. The number of reference clock resources is package dependent.

Configuration Pins

Table 107: Dedicated Configuration Pins

These pins cannot be used as general-purpose I/O after configuration.

All the pins are in internal weak pull-up during configuration mode except for `TCK` and `TDO`.

Calculate the resistor value as described in "Resistors in Configuration Circuitry" in AN 033: Configuring TJ-Series FPGAs.

Pins	Direction	Description	External Weak Pull Up/ Pull Down Requirement
CDONE	I/O	Configuration done status pin. CDONE is an open drain output; connect it to an external pull-up resistor to VCCIO. When CDONE = 1, the configuration is complete and the FPGA enters user mode. You can hold CDONE low and release it to synchronize the FPGAs entering user mode.	Pull up
CRESET_N	Input	Active-low FPGA reset and re-configuration trigger. Pulse CRESET_N low for a duration of t_{creset_N} before releasing CRESET_N from low to high to initiate FPGA re-configuration. This pin does not perform a system reset.	Pull up
TCK	Input	JTAG test clock input (TCK). The rising edge loads signals applied at the TAP input pins (TMS and TDI). The falling edge clocks out signals through the TAP TDO pin.	Pull up
TMS	Input	JTAG test mode select input (TMS). The I/O sequence on this input controls the test logic operation . The signal value typically changes on the falling edge of TCK. TMS is typically a weak pull-up; when it is not driven by an external source, the test logic perceives a logic 1.	Pull up
TDI	Input	JTAG test data input (TDI). Data applied at this serial input is fed into the instruction register or into a test data register depending on the sequence previously applied at TMS. Typically, the signal applied at TDI changes state following the falling edge of TCK while the registers shift in the value received on the rising edge. Like TMS, TDI is typically a weak pull-up; when it is not driven from an external source, the test logic perceives a logic 1.	Pull up
TDO	Output	JTAG test data output (TDO). This serial output from the test logic is fed from the instruction register or a test data register depending on the sequence previously applied at TMS. The shift out content is based on the issued instruction. The signal driven through TDO changes state following the falling edge of TCK. When data is not being shifted through the device, TDO is set to an inactive drive state (e.g., high-impedance).	Pull up

(17) CDONE has a drive strength of 12 mA at 1.8 V.

Table 108: Dual-Purpose Configuration Pins

In user mode (after configuration), you can use these dual-purpose pins as general I/O.
Calculate the resistor value as described in "Resistors in Configuration Circuitry" in AN 033: Configuring TJ-Series FPGAs.

Configuration Functions	Direction	Description	External Weak Pull Up/Pull Down Requirement
CBSEL[1:0]	Input	Multi-image configuration selection pin. This function is not applicable to single-image bitstream configuration or internal reconfiguration (remote update). Connect CBSEL[1:0] to the external resistors for the image you want to use: 00 for image 1 01 for image 2 10 for image 3 11 for image 4 0: Connect to an external weak pull down. 1: Connect to an external weak pull up.	Pull up or pull down
CCK	I/O	Passive SPI input configuration clock or active SPI output configuration clock.	Optional pull up if required by external load
CDI*n*	I/O	Data input for SPI configuration. *n* is a number from 0 to 31 depending on the SPI configuration data width. CDI0 is an output in x1 active configuration mode and is a bidirectional pin in all other active configuration modes. CDI4 is a bidirectional pin in x8 active configuration mode. In a multi-bit daisy chain connection, CDI[31:0] connects to the data bus in parallel.	Optional pull up if required by external load
CSI	Input	Chip select. 0: The FPGA is not selected or enabled and will not be configured. 1: Select the FPGA for configuration modes. CSI must remain high throughout configuration.	Pull up
CSO	Output	Chip select output. Asserted after configuration is complete. Connect this pin to the chip select pin of the next FPGA for daisy chain configuration.	–
NSTATUS	Output	Indicates a configuration error. When the FPGA drives this pin low, it indicates either a device mismatch or a failed bitstream CRC check. Refer to **Table 1**.	–
SSL_N	I/O	SPI configuration mode select. The FPGA senses the value of SSL_N when it comes out of reset (i.e., CRESET_N transitions from low to high). 0: Passive mode; connect to external weak pull down. 1: Active mode; connect to external weak pull up. In active configuration mode, SSL_N is an active-low chip select to the flash device (CDI0 - CDI3).	Pull up or pull down
SSU_N	Output	Active-low chip select to the upper flash device (CDI4 - CDI17) in active x8 configuration mode (dual quad mode).	Optional pull up if required by external load
EXT_CONFIG_CLK	Input	Alternative clock in active configuration mode.	Optional pull up if required by external load
TEST_N	Input	Active-low test mode enable signal. Set to 1 to disable test mode. During all configuration modes, rely on the external weak pull-up or drive this pin high.	Pull up

Note: Refer to the column Configuration Functions in the pinout file.

Dedicated DDR Pinout

Table 109: Dedicated DDR Pinout

n indicates the number.

Function	Direction	Description
DDR_A[*n*]	Output	Address signals to the memories.
DDR_CKE	Output	Active-high clock enable signals to the memories.
DDR_CK DDR_CK_N	Output	Differential clock output pins to the memories.
DDR_CS_N	Output	Active-low chip select signals to the memories.
DDR_DQ[*n*]	I/O	Data bus to/from the memories.
DDR_DM[*n*]	I/O	Active-high data-mask signals to the memories.
DDR_DQS[*n*] DDR_DQS_N[*n*]	I/O	Differential data strobes to/from the memories.
DDR_RST_N	Output	Active-low reset signals to the memories.
DDR_CAL	Input	240 Ω to ground reference resistor port.
VDD_PHY	–	DDR digital power supply.
VDDQ_PHY	–	DDR I/O power supply.
VDDQX_PHY	–	DDR I/O pre-driver power supply.
VDDPLL_MCB_TOP_PHY	–	DDR PLL power supply.
VDDQ_CK_PHY	–	DDR I/O power supply for clock.

Dedicated MIPI D-PHY Pinout

Table 110: Dedicated MIPI D-PHY Pinout

m and *n* indicates the number. *L* indicates the lane

Function	Direction	Description
VCC18A_MIPI*m*_*n*_TX	–	Power supply for the MIPI D-PHY TX block. *m* and *n* are the MIPI channel numbers. For example: VCC18A_MIPI0_1_TX displays the power of MIPI D-PHY TX channel 0 and channel 1 being shorted together.
VCC18A_MIPI*m*_*n*_RX	–	Power supply for the MIPI D-PHY RX block. *m* and *n* are the MIPI interface numbers. For example: VCC18A_MIPI0_1_RX displays the power of MIPI D-PHY RX channel 0 and channel 1 being shorted together.
MIPI*n*_TXDP*L* MIPI*n*_TXDN*L*	I/O	MIPI differential transmit data lane.
MIPI*n*_RXDP*L* MIPI*n*_RXDN*L*	I/O	MIPI differential receive data lane.

Pin States

HVIO pins have an internal pullup/down (see **Figure 18: HVIO Interface Block** on page 27); HSIO configured as GPIO have an internal pull up/down (see **Figure 20: I/O Interface Block** on page 29). The following table shows the pin state during reset, configuration, and when unused in user mode.

Note: For the DDR pin states, refer to the TJ-Series DDR DRAM Block User Guide.

Table 111: I/O Pin States

Pin Type	During Reset (CRESET_N Low)	During Configuration (CRESET_N High, CDONE Low)	When Unused in User Mode (Default)
User Pins			
HSIO	Input tri-state with weak pull up.	Input tri-state with weak pull up.	Input tri-state with weak pull up.[18]
HVIO	Input tri-state with weak pull up.	Input tri-state with weak pull up.	Input tri-state with weak pull up.[18]
Dual-Purpose Configuration Pins			
CSO	0	0[19]	Input tri-state with weak pull up.
NSTATUS	0	1[20]	Input tri-state with weak pull up.
CCK	Input tri-state with weak pull up.	SPI active output clock. SPI passive input with weak pull up.	Input tri-state with weak pull up.
CDI0	Input tri-state with weak pull up.	SPI active output. SPI passive input with weak pull up.	Input tri-state with weak pull up.

As shown in **Power-Up Sequence** on page 66, `CRESET_N` must be kept low during power up.

Note: Refer to the following tables for details:
Table 71: HVIO Internal Weak Pull-Up and Pull-Down Resistance on page 76
Table 72: HSIO Internal Weak Pull-Up and Pull-Down Resistance on page 77

[18] You can change the default mode to weak pull-down in the Interface Designer.
[19] CSO is driven to 1 when the bitstream is done transmitting.
[20] NSTATUS set to 1 if valid bit stream detected. Remains at 0 if bit stream is authenticated or encrypted.

The following table shows the states for the MIPI D-PHY pins.

Table 112: MIPI D-PHY Pin States

Pin Type	During Reset (CRESET_N Low)	During Configuration (CRESET_N High, CDONE Low)	When Unused in User Mode (Default)
MIPI 2.5G D-PHY TX	Input tri-state, no pull up or pull down.	Input tri-state, no pull up or pull down.	Input tri-state, no pull up or pull down.
MIPI 2.5G D-PHY RX	Input.	Input.	Input.

Ti180 Interface Floorplan

Note: The numbers in the floorplan figures indicate the HVIO and HSIO number ranges. Some packages may not have all HVIO or HSIO pins in the range bonded out. Refer to the Ti180 pinout file for information on which pins are available in each package.

Figure 52: Floorplan Diagram for J361 Packages

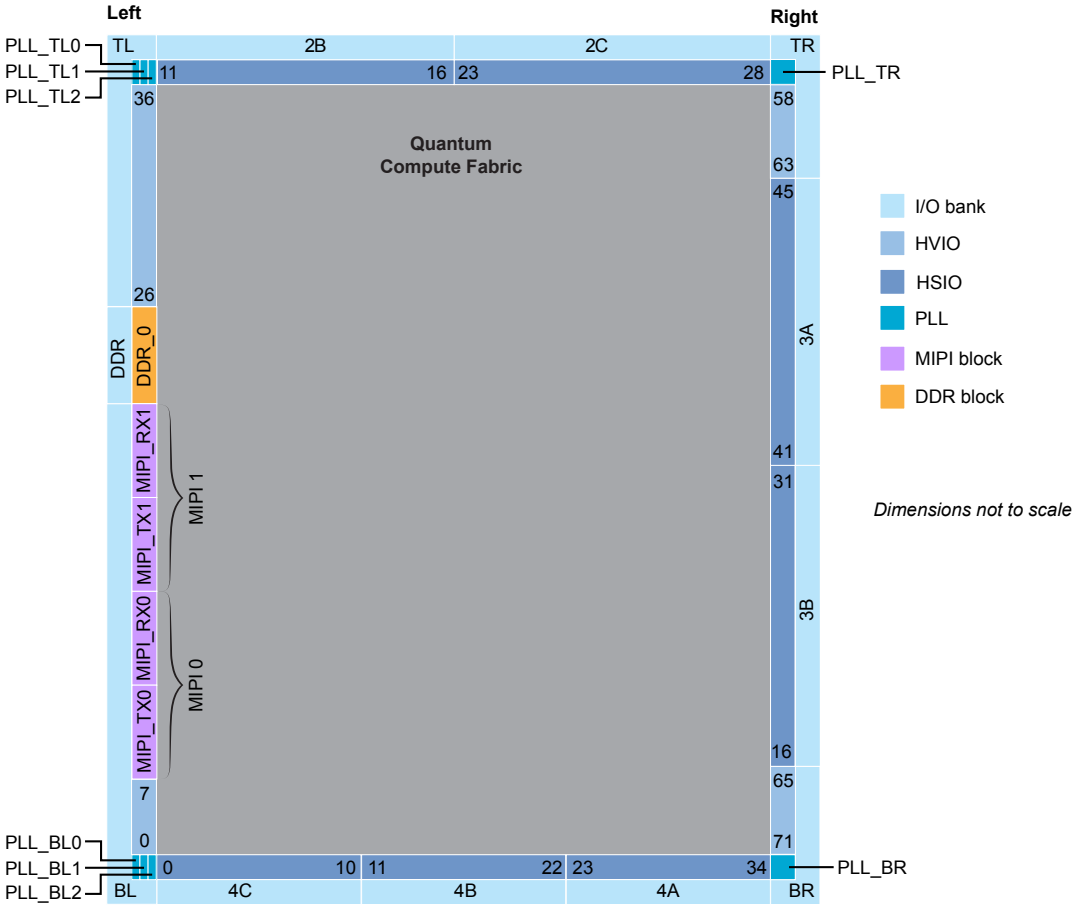


Figure 53: Floorplan Diagram for G400 Packages

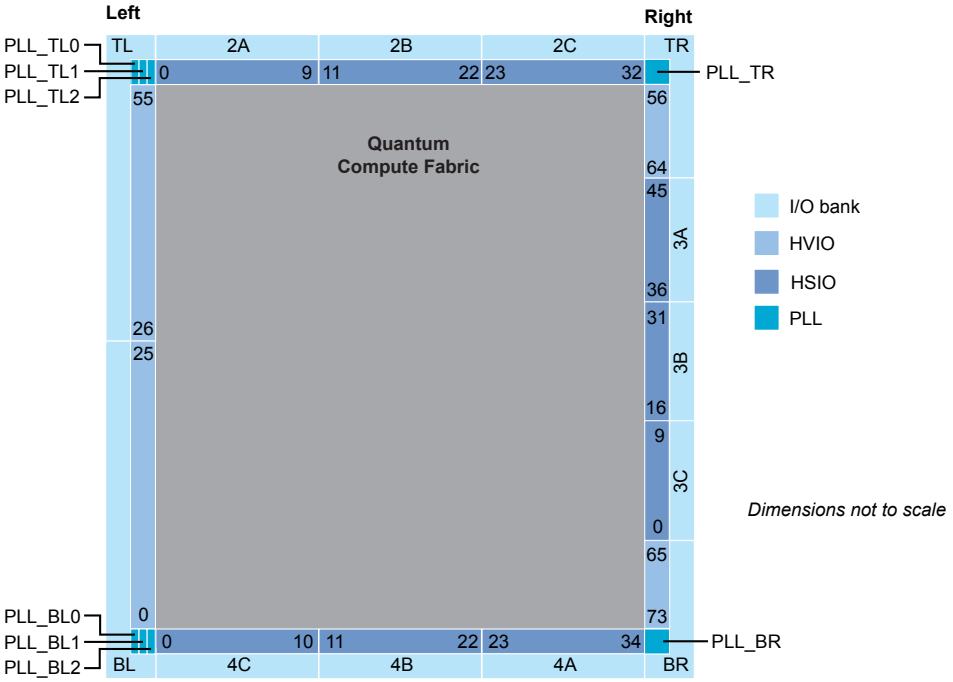


Figure 54: Floorplan Diagram for L484 Packages

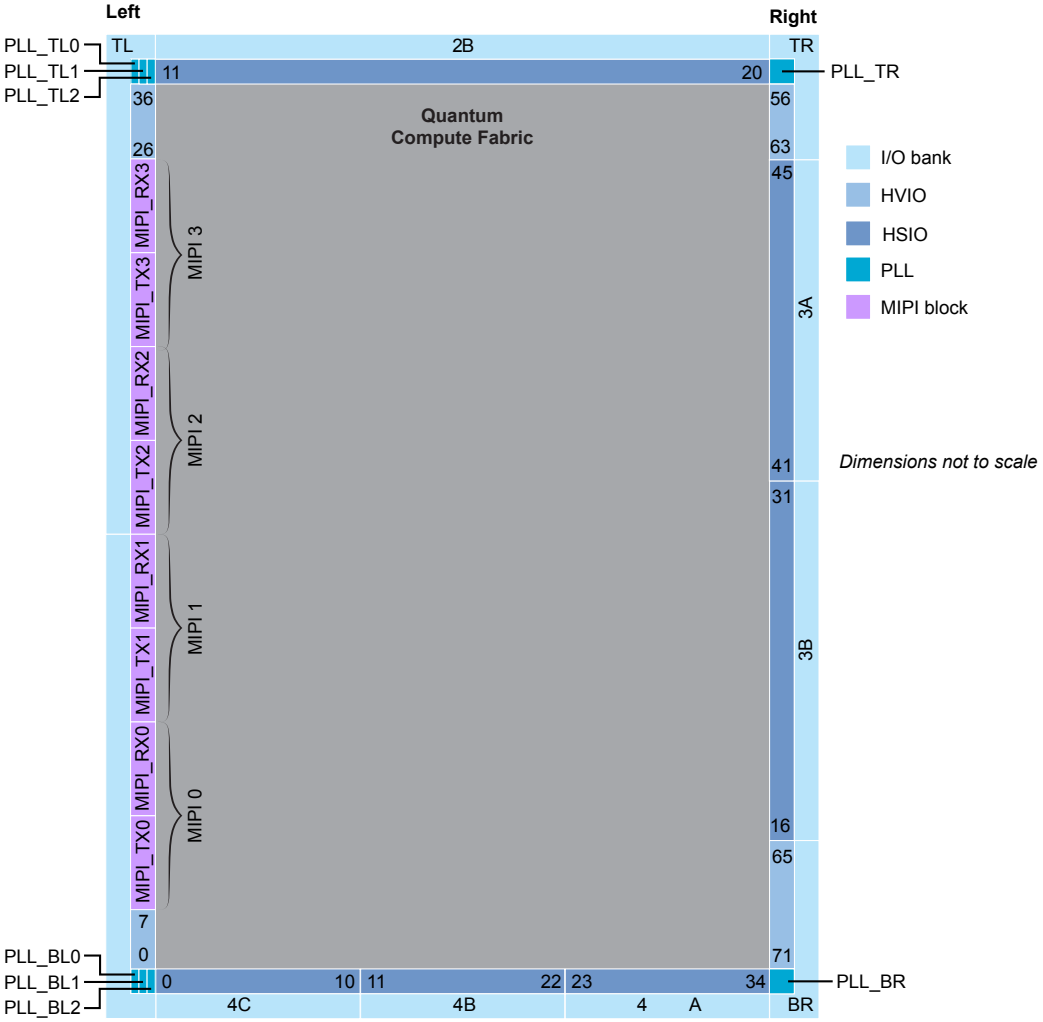


Figure 55: Floorplan Diagram for J484 and M484 Packages

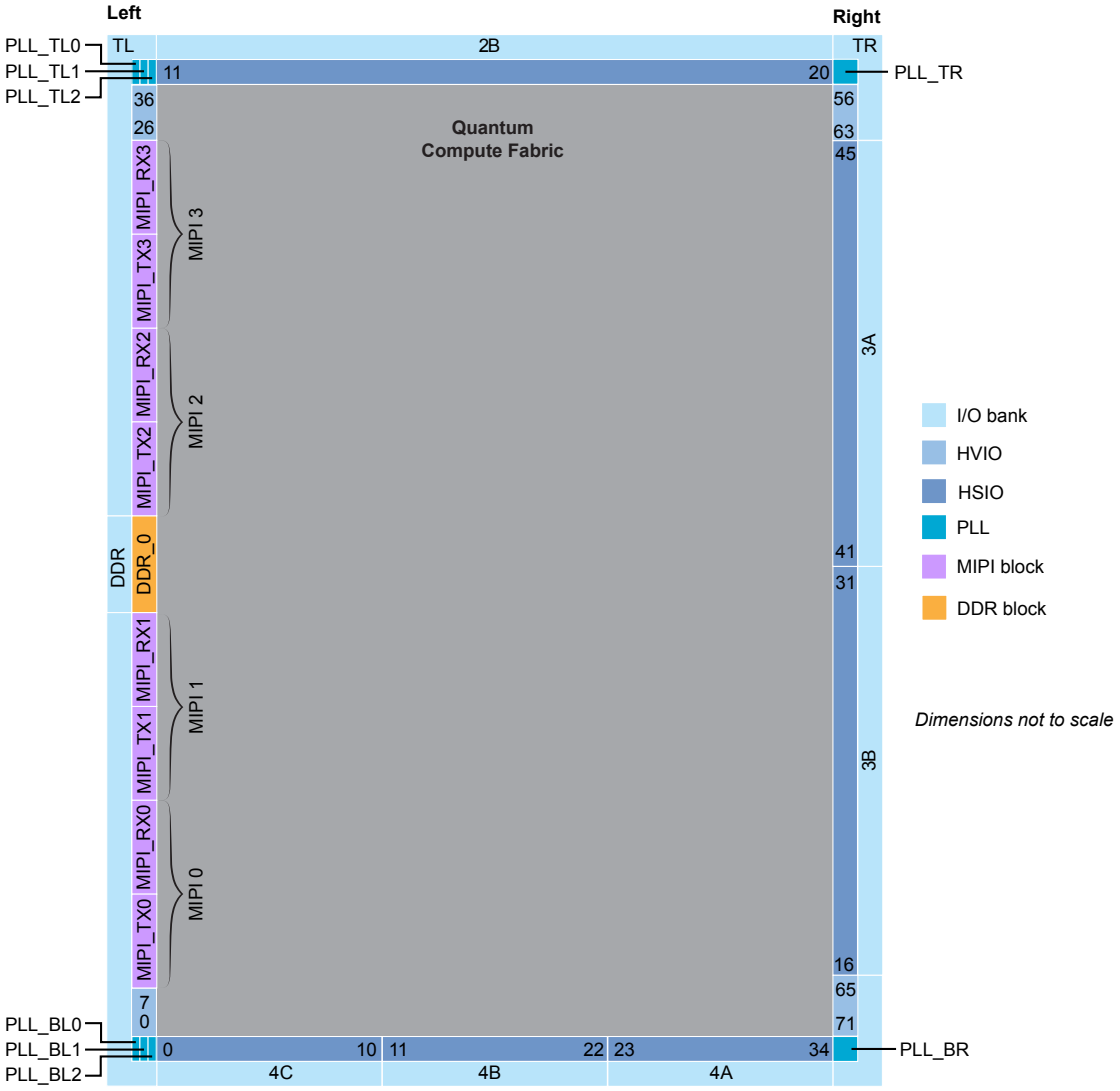
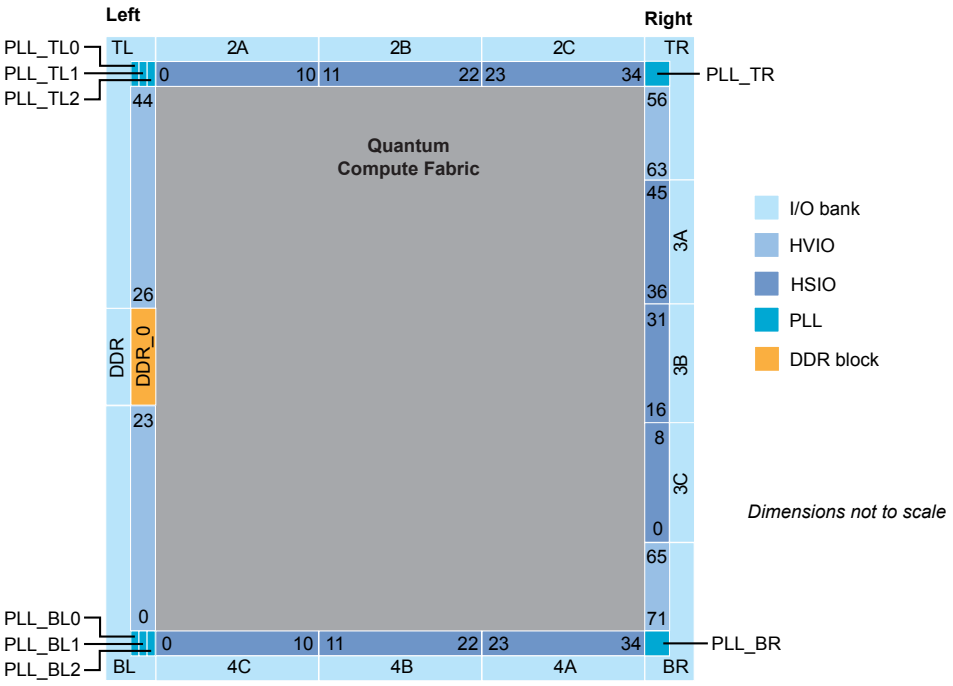


Figure 56: Floorplan Diagram for G529 Packages



Efinity Software Support

The Efinity® software provides a complete tool flow from RTL design to bitstream generation, including synthesis, place-and-route, and timing analysis. The software has a graphical user interface (GUI) that provides a visual way to set up projects, run the tool flow, and view results. The software also has a command-line flow and Tcl command console. The Efinity® software supports simulation flows using the ModelSim, NCSim, or free iVerilog simulators. An integrated hardware Debugger with Logic Analyzer and Virtual I/O debug cores helps you probe signals in your design. The software-generated bitstream file configures the Ti180 FPGA. The software supports the Verilog HDL, SystemVerilog, and VHDL languages.

Ordering Codes

Refer to the **TJ-Series Selector Guide** for the full listing of Ti180 ordering codes.

Revision History

Table 113: Revision History

Date	Version	Description
March 2026	3.7	Updated **DSP block diagram**; W register moved to after adder. (DOC-2592) Updated **Table 6: HSIO Supported I/O Standards** on page 22. Corrected definition for MIPI D-PHY signal ERR_SOT_HS_LAN*n*; SOT is start of transmission. (DOC-2755) Updated the presentation of the LPDDR4/4x resource information in **#unique_3/unique_3_Connect_42_table_tnz_rbm_hyb** to be consistent with other data sheets. (DOC-2814) The Efinity software issues a warning (not error) if you do not leave enough separation between GPIO and LVDS or MIPI lane pins (**see note**). (DOC-2833) Added pull-down resistor to HVIO figure **Figure 18: HVIO Interface Block** on page 27. (DOC-2884) Corrected **Figure 24: LVDS RX Interface Block Diagram** on page 33 and **Figure 28: LVDS Bidirectional Interface Block Diagram** on page 36; they incorrectly showed two PLLs. (DOC-2932)
October 2025	3.6	Updated **Figure 19: HSIO Buffer Block Diagram** on page 28 and **Figure 23: I/O Buffer Path for Differential HSTL and SSTL** on page 32; some N signals were incorrectly labeled as P. (DOC-2676) Updated **Table 22: MIPI Lane Pads** on page 42; updated signal direction. Updated AWCOBUF_*x* in **Table 33: AXI4 Write Address Signals (Interface to FPGA Core Logic)** on page 48. Added notes for **Single-Event Upset Detection** on page 62. (DOC-2602) Updated NSTATUS description in **Table 108: Dual-Purpose Configuration Pins** on page 92. Updated NSTATUS pin state during reset and configuration in **Table 111: I/O Pin States** on page 95. (DOC-2727)
June 2025	3.5	Minor fixes.
March 2025	3.4	Updated configuration timing and fuse programming waveforms. (DOC-2272) Moved table describing connection requirements for unused resources and features to the **Unused Resources and Features** on page 68 topic. In **Table 6: HSIO Supported I/O Standards** on page 22, updated "When Configured As" column for Sub-LVDS and SLVS. (DOC-2314)
November 2024	3.3	Added DLYCLK GPIO signal. (DOC-2159) Updated GPIO and LVDS interface pin names (IN to I and OUT to O) to align with primitives. (DOC-2086) Removed PLL IOFBK interface pin. The SAMPLE/PRELOAD instruction is available after JTAG fuses have been blown. (DOC-2225)
October 2024	3.2	Added notes to the configuration timing and security feature topics about not using SPI and JTAG at the same time. (DOC-2047) Updated configuration timing and fuse programming waveforns. (DOC-2156) Clarified HVIO and HSIO pin states during configuration and when unused in user mode. (DOC-2041)

Date	Version	Description
September 2024	3.1	Corrected MIPI D-PHY interface performance specification. (DOC-2064) Fixed typo in **Table 108: Dual-Purpose Configuration Pins** on page 92. (DOC-2038) Changed column name from Pins to Configuration Functions in **Table 108: Dual-Purpose Configuration Pins** on page 92. (DOC-2038) Added note after **Table 108: Dual-Purpose Configuration Pins** on page 92 directing the reader to the device pinout file. (DOC-2038) Updated **Fuse Programming Requirements** on page 65 with details of VQPS current. (DOC-1999) Removed duplicate specification for F_{OUT} in PLL Timing and AC Characteristics topic. (DOC-1947) Clarified which signals are available when LVDS settings are enabled. (DOC-1908) Added reset recommendations for PLLs and cascaded PLLs. (DOC-1900) Removed duplicate paragraph about the XLR cell.
June 2024	3.0	Split specification for VCC18A_MIPI into VCC18A_MIPI_TX and VCC18A_MIPI_RX. (DOC-1894) Updated LPDDR4/4x and MIPI D-PHY performance specifications for Q3 speed grade. Added automotive speed grade to features.
March 2024	2.9	Specifications are no longer preliminary. Added Q3 (automotive) specifications. Added EXTFB to table of alternate pin functions. Added LPDDR4 DRAM controller power pins to the Absolute Maximum Ratings table. Combined tables of Recommended Operating Conditions into one for ease of use. Added pipeline mode for DDIO. (DOC-1571) Updated power ramp-up details in **Power-Up Sequence** on page 66. (DOC-1683) Added note to **Power-Up Sequence** on page 66 about DDR DRAM power supply requirements. (DOC-1573) Removed t_{MIPI_Power} (MIPI power-up details provided in **Power-Up Sequence** on page 66). (DOC-1609) Updated Power-Up Groups table. Moved dedicated DDR and MIPI D-PHY pinouts into separate sections. Corrected OUTCLK connection in **Figure 20: I/O Interface Block** on page 29. (DOC-1630) Rearranged **Configuration Timing** on page 85 to keep waveforms together with tables. Updated the configuration timing waveforms for SPI active and SPI passive. For the PLL equation $F_{VCO} = (F_{PFD} \times M \times O \times C_{FBK})$, removed the restriction that $(M \times O \times C_{FBK})$ must be ≤ 255. Updated **Configuration Pins** on page 91. Removed MIPI Power-Up Timing topic. This content is moved to **Power-Up Sequence** on page 66 Updated oscillator specification. (DOC-1663) Updated description for HSIO block DLY_INC signal. (DOC-1697) Removed M361 and F529 packages. (DOC-1731) MIPI D-PHY specification is v1.1. (DOC-1610)

Date	Version	Description
November 2023	2.8	Added table V_{IH}, V_{IL}, V_{OL}, V_{OH} Specifications for LPDDR4/LPDDR4x. (DOC-1316) Updated MIPI RCLKs in image of Clock Sources that Drive the Regional Network. (DOC-1362) Removed table Single-Ended I/O and Dedicated Configuration Pins Schmitt Trigger Buffer Characteristic. Added 3.3 V and 2.5 V in table HSIO Pins Configured as Single-Ended I/O DC Electrical Characteristics. Added table Supported HVIO Drive Strength and Supported HSIO Drive Strength. (DOC-1377) Updated min ramp time in table Power Supply Ramp Rates. (DOC-1407) Updated MIPI D-PHY in table title and pinout description in table Dedicated MIPI D-PHY Pinouts. Previously table was MIPI Pinout (Dedicated). (DOC-1409) Updated input leakage limit in table HVIO DC Electrical Characteristics, and HSIO Pins Configured as Single-Ended I/O DC Electrical Characteristics. (DOC-1411) Added important note to highlight the CRESET_N requirement during power-up sequence. (DOC-1443) Updated image Power-Up Sequence. Removed VQPS from Group 2 in table Power-Up Groups by Package Variation and combined Group 2 and 3 together. Changed to GND from 1.8 V for Security (Fuse Blowing) in table Connection Requirements for Unused Resources and Features. Added section Fuse Programming Requirements in Security Features. (DOC-1467) Corrected typo for VCCIO33 max supply in Absolute Maximum Ratings table. (DOC-1483) Added max. value of f_{TCK} at 3 MHz at an operating voltage of 1.8 V to in JTAG Mode table. Added max. value of V_{IL} at 0.28 V for 1.8 V JTAG Configuration in HVIO DC Electrical Characteristics. (DOC-1510) Corrected typo in HSIO Pins Configured as Differential SSTL I/O Electrical Characteristics table. (DOC-1514) Added Power-Down Sequence topic. Updated value of power supply current transient to 1500 mA in table Minimum Power Supply Current Transient. Updated initial CCK waveform of figure SPI Passive Mode (x1) Timing Sequence.
August 2023	2.7	Updated Programmable Delay Chains section, and added static and dynamic delay step size specs. (DOC-1342) Added G400 package. (DOC-1384) Added note about keeping both the current and the next clocks toggling during dynamic clock switching. (DOC-1405)
June 2023	2.6	Added note about 7 x 6 Quad mode output is truncated to 12-bit (DOC-1295) Added slvs option for HSIO configured as LVDS blocks. (DOC-1190) Added Spread-Spectrum Clocking PLL block. (DOC-1178) Updated DDR_DM signal description. (DOC-1322)
May 2023	2.5	Improved MIPI RX function description and added missing MIPI RX signal descriptions. (DOC-1173) Updated 2.5 V LVCMOS max toggle rate. (DOC-1251) Updated LPDDR4 interface maximum data rate for J361, J484, and G529 packages. (DOC-1249) Replaced t_{LVDS_DT} and t_{INDT} specs with t_{PLL_HLW} and t_{LVDS_CPA}. (DOC-1189) Updated PLL LOCKED signal description. (DOC-1208)
April 2023	2.4	Added LVDS RX DBG signals. (DOC-1124) Added note about using LVDS blocks from the same side of the FPGA to minimize skew. (DOC-1150) Updated DDR DRAM interface input clock to include description for J361, J484, and G529 packages. (DOC-1209) Updated PLL RSTN signal description about de-asserting only when CLKIN is stable. (DOC-1226)

Date	Version	Description
February 2023	2.3	Updated LPDDR4 interface maximum data rate for M361, M484, and F529 packages. (DOC-1107) Corrected PLL_SSC_EN MIPI TX D-PHY signal notes. (DOC-1101) Corrected VDDQ_CK_PHY pin name and standardized VCCA pin names. (DOC_1114) Added note about achieving maximum toggle rate. (DOC-1099) Added link in Power Up Sequence pointing to the Web Interactive Hardware Design Checklist and Guidelines. (DOC-1123) Updated REF_RES_3A pin connection requirement in the Pinout Description topic. Updated VQPS power-down sequence note. Added connection requirement when unused for VQPS.
December 2022	2.2	Added VQPS in power up sequence requirement. (DOC-951) Updated for J361, J484, and G529 package support. (DOC-1041) Updated M361, M484, and F529 LPDDR4/4x to only support x16 DQ width. Updated M361, M484, and F529 LPDDR4/4x maximum data rate. Added floorplan diagrams. (DOC-1016) Updated Clock Sources that Drive the Regional Network diagram. (DOC-969) Updated configuration pins external weak pull-up requirements. (DOC-1035) Updated DDR signal name from ARST_x to ARSTN_x. (DOC-1025) Added DPA specs and updated DPA description to support full-rate serialization mode only. (DOC-1078) Updated LVDS and sub-LVDS specs to include half-rate and full-rate serialization. (DOC-1078) Updated JTAG configuration timing specs. (DOC-1083)
October 2022	2.1	Updated DDR DRAM interface signals. (DOC-942) Updated REF_RES_*xx* pins connection requirement. (DOC-943)
September 2022	2.0	Removed GCTRL and RCTRL. (DOC-895) Corrected AWID_x, AWREADY_x, ARADDR_x, and AWADDR_x DDR signals directions and widths. (DOC-907) Updated DDR DRAM Performance specs. (DOC-900) Added note recommending up to only 2 cascading PLLs. (DOC-931) Updated description about differential receivers are powered by VCCAUX. (DOC-929)
August 2022	1.9	Added LPDDR4 and LPDDR4X maximum data rates for C3, C4, I3, and I4 packages. Updated t_{CRESET_N} spec. (DOC-876) Updated DDR DRAM block CLKIN resource. (DOC-881) Corrected MIPI RX Lane Block Diagram. (DOC-878)
July 2022	1.8	Added PLL Reference Clock Resource Assignments. Added MIPI D-PHY maximum data rate specs.
July 2022	1.7	Updated note about pins separation when using HSIO as GPIO, LVDS, or MIPI lanes. (DOC-769) Removed footnote in Minimum Power Supply Current Transient table. (DOC-818) Updated MIPI D-PHY port names. (DOC-782) Updated DDR power supplies to match pinout and Efinity software. (DOC-795) Added L484 package specs and features. (DOC-821) Updated and improved clock and control network content and figures. (DOC-668) Updated the power up sequence topics. Updated package-dependent resources table. Added I4 and I4L packages. Updated DDR and MIPI DPHY block pad names. Removed SPI and JTAG Pins in Secure Mode topic.
April 2022	1.6	Updated test condition load to maximum load in Maximum Toggle Rate Table. (DOC-781) Corrected description for differential TX static programmable delay. (DOC-786) Added PLL period jitter spec with noisy input clock specs and updated test condition note. (DOC-771)

Date	Version	Description
April 2022	1.5	Updated figure title for Connections for Clock and RX Data Lane in the Same MIPI RX Group. (DOC-739) Updated LVDS/RSDS/mini-LVDS RX supported VCCIO. (DOC-740) Added Power Supply Current Transient. (DOC-761) Corrected RD and RST signal directions in MIPI RX Lane Block Diagram.
March 2022	1.4	Updated power supply ramp rate and power up sequence diagram. (DOC-631) Updated external pull-up requirement for dual-purpose configuration pins. (DOC-734)
February 2022	1.3	Corrected t_H and t_{SU} parameter label in SPI Passive Mode (x1) Timing Sequence figure. Updated active and passive configuration timing specs. (DOC-708) Updated 2.5 V LVCMOS V_{IH} and V_{IL} specs. (DOC-718) Added I_{IN} and V_{IN} specs. (DOC-652) Updated MIPI and LVDS maximum toggle rate. Updated available package options. Added note about the block RAM content is random and undefined if it is not initialized. (DOC-729) Added MIPI and DDR pins in pinout description. (DOC-712) Updated M361 package available resources.
January 2022	1.2	Merged MIPI and LVDS data rate specs into Maximum Toggle Rate table.
January 2022	1.1	I/O banks for HVIO pins support dynamic voltage shifting. (DOC-444) Added Schmitt Trigger input buffer specs. (DOC-606) Added PLL reference clock input duty cycle specs. (DOC-661) Updated HVIO maximum toggle rate specs. (DOC-689) Removed I4 and I4L speed grades. (DOC-681) Updated global clock buffer, DSP, BRAM, HSIO as LVDS, and HSIO as MIPI lane specs. (DOC-693) Added internal weak pull-up resistor and drive strength specs for CDONE and CRESET_N. (DOC-635) Added ambient storage temperature spec. (DOC-678)
December 2021	1.0	Initial release.