TJ-Series FPGAs

You only have a few square millimeters to spare, and you need to pack in as much computing power as you can. Elitestek's next-generation TJ-Series FPGAs can help. TJ-Series FPGAs are fabricated on a 16 nm process, delivering high performance with the lowest possible power and a small physical size. They feature the innovative Quantum® compute fabric that, with its enhanced compute capability, makes TJ-Series FPGAs ideal for embedded hardware acceleration applications. With a wide range of logic element (LE) densities from 35K to 1M, and compatibility with the Elitestek RISC-V SoCs, they can help you turn a tiny chip into an accelerated embedded compute system.
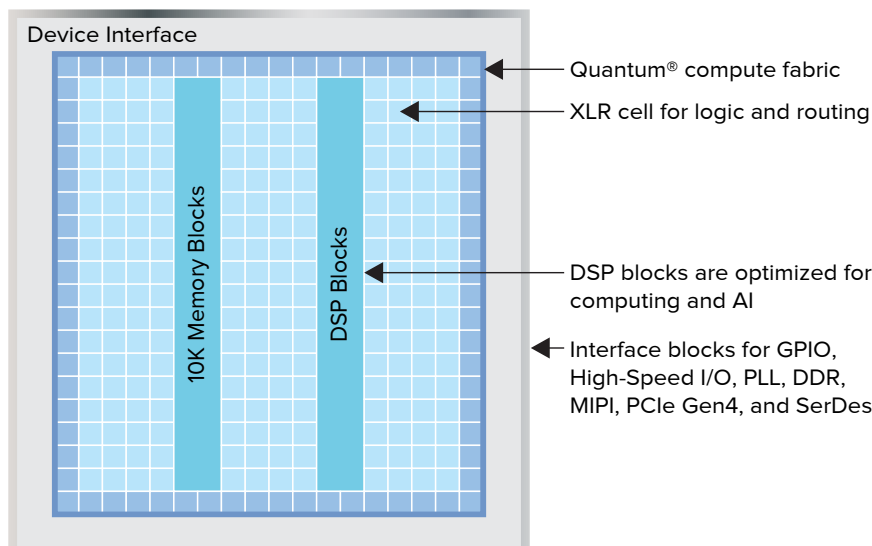
Quantum® Compute Fabric

The Quantum compute fabric is made up of configurable tiles, the eXchangeable logic and routing (XLR) cell, that optimizes routing efficiency and speed while achieving high utilization ratios. The fabric also has highly configurable, 10K embedded memory blocks along with dedicated, high-speed, DSP blocks. Together, these features deliver optimum performance for a wide array of applications from edge compute to industrial automation and video processing.

The 16 nm process node gives TJ-Series FPGAs a small footprint with low power consumption, making them ideal for highly integrated applications.

Figure 1 TJ-Series FPGA Block Diagram

- **16 nm process**
- **Low power**
- **High performance**
- **Small size**
- **Quantum® compute fabric**

Table 1 Resources and Interfaces

Feature	Ti35	Ti60	TJ85	Ti90	Ti120	TJ135	Ti180	TJ180	TJ240	TJ375	TJ550	TJ750	TJ1000
Logic Elements (LEs)	36,176	62,016	83,232	92,534	123,379	132,192	176,256	176,256	236,888	370,137	550,000	750,000	1,000,004
10K RAM blocks (Mb)	1.53	2.62	6.18	6.88	9.18	9.83	13.11	13.11	17.62	27.53	40.92	55.8	74.4
DSP blocks	93	160	300	336	448	480	640	640	860	1,344	2,006	2,736	3,648
PLLs	4	4	9	8	8	9	8	8	12	12	12	12	12
High-voltage I/O	27	27	84	74	74	84	74	54	103	103	200	200	200
High-speed I/O	142	142	139	210	210	139	210	190	234	234	320	320	320
LPDDR4/4x	—	—	x32	x32	x32	x32	x32	x16	2 x32	2 x32	2 x72	2 x72	2 x72
MIPI D-PHY 2.5 Gbps	—	—	2 TX 2 RX	4 TX 4 RX	4 TX 4 RX	2 TX 2 RX	4 TX 4 RX	2 TX 2 RX	3 TX 3 RX	3 TX 3 RX	3 TX 3 RX	3 TX 3 RX	3 TX 3 RX
Transceivers	—	—	2 x4	—	—	2 x4	—	—	4 x4	4 x4	6 x4	6 x4	6 x4
25.8G Transceivers	—	—	—	—	—	—	—	—	—	—	x8	x8	x8
Hardened RISC-V block	—	—	Quad Core	—	—	Quad Core	—	—	Quad Core	Quad Core	Quad Core	Quad Core	Quad Core
PCIe® Gen4 (16G)	—	—	1 x4	—	—	1 x4	—	—	2 x4	2 x4	2 x8	2 x8	2 x8

Refer to the FPGA data sheet or TJ-Series Selector Guide for details on which resources are available in each package.

Table 2 Package Options

Package	Pitch (mm)	Size (mm)	Ti35	Ti60	TJ85	Ti90	Ti120	TJ135	Ti180	TJ180	TJ240	TJ375	TJ550	TJ750	TJ1000
64-ball WLCSP	0.4	3.5x3.4		✓											
100-ball FBGA (1)	0.5	5.5x5.5	✓	✓											
225-ball FBGA	0.65	10x10	✓	✓											
256-ball FBGA	0.8	13x13	✓	✓											
361-ball FBGA	0.65	13x13				✓	✓		✓						
400-ball FBGA	0.8	16x16				✓	✓		✓						
441-ball FBGA	0.5	11x11			✓			✓							
484-ball FBGA (2)	0.65	15x15							✓	✓					
484-ball FBGA	0.8	18x18			✓	✓	✓	✓	✓		✓	✓			
529-ball FBGA	0.8	19x19				✓	✓		✓		✓	✓			
576-ball FBGA	0.65	16x16			✓			✓							
676-ball FBGA	0.65	18x18									✓	✓			
676-ball FBGA	0.8	22x22			✓			✓							
900-ball FBGA	0.8	25x25									✓	✓			
1156-ball FBGA	1.0	35x35									✓	✓	✓	✓	✓

1. The 100 pin package is available as a regular package as well as a SIP that incorporates SPI flash and HyperRAM in addition to the FPGA.
2. The 484 pin package is a SIP that incorporates LPDDR DRAM in addition to the FPGA.

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